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Inventors: SORRELLS et al.
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FIG. 1

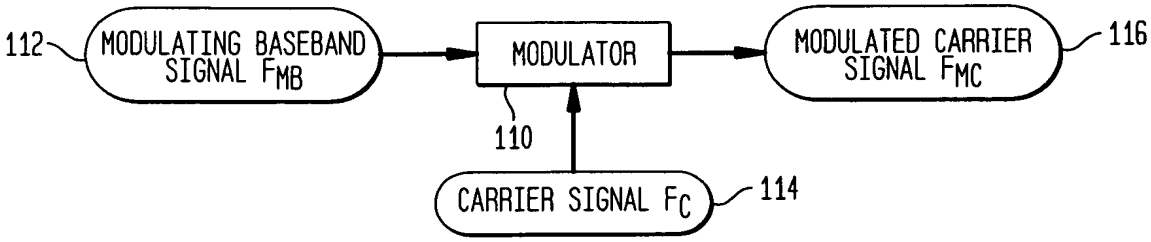



FIG. 2

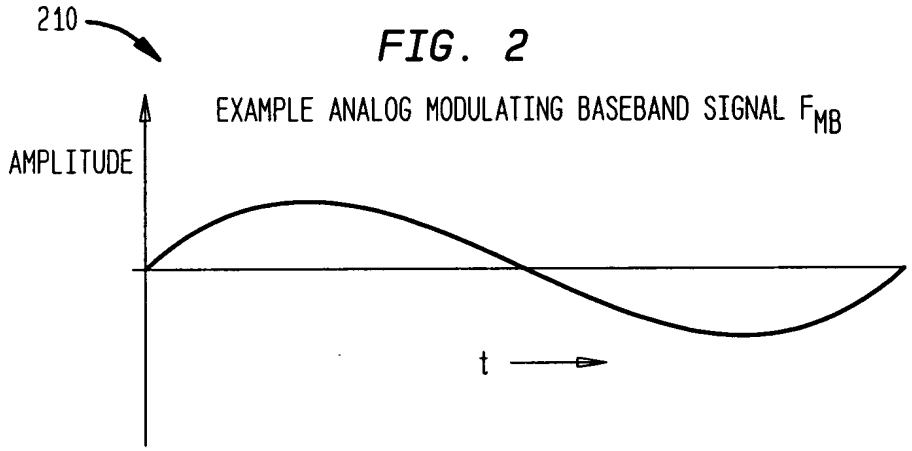



FIG. 3

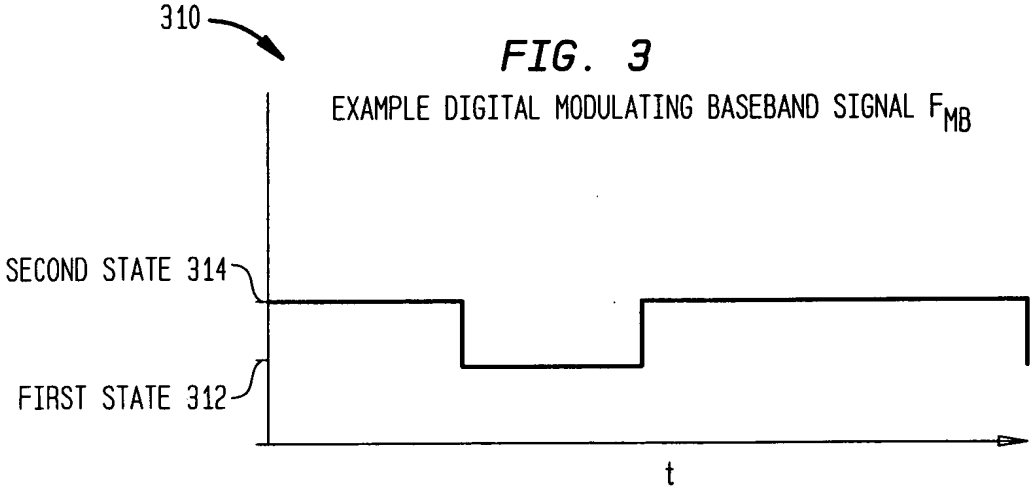
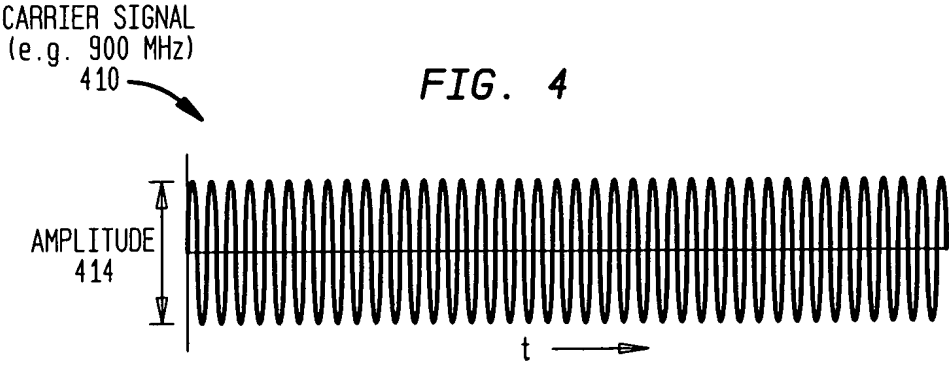



FIG. 4



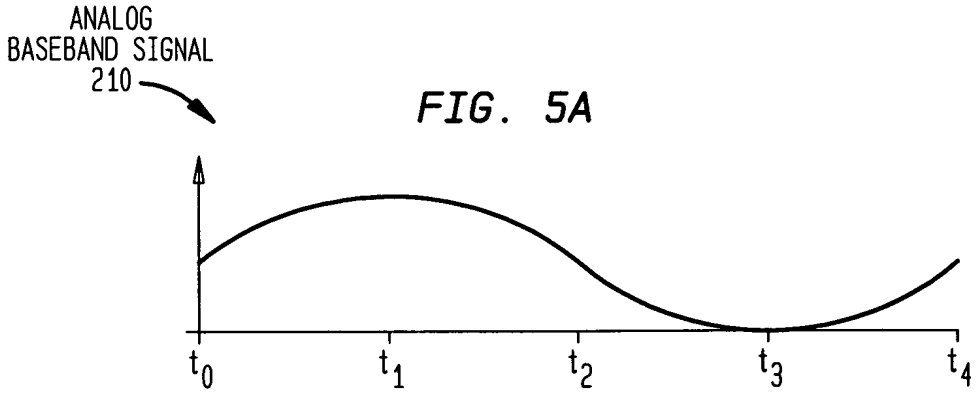



FIG. 5A

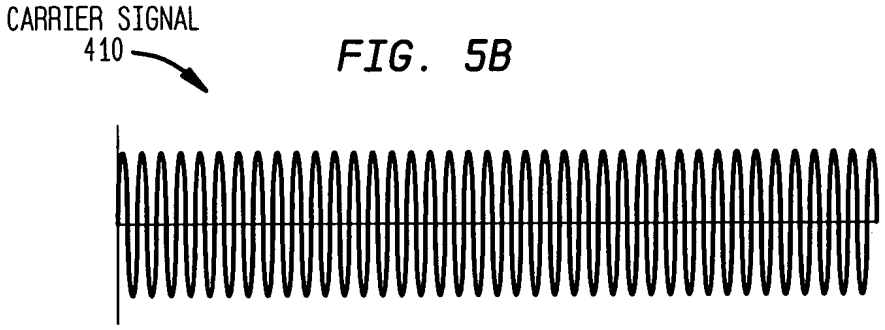



FIG. 5B

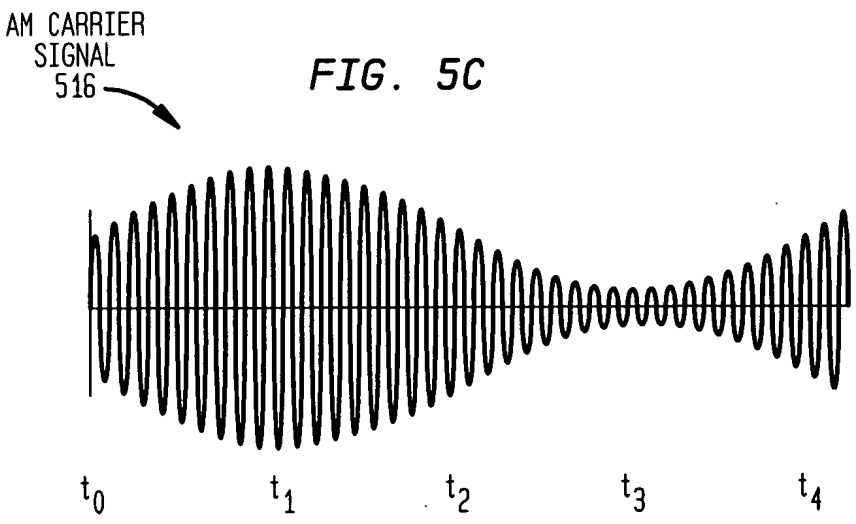



FIG. 5C

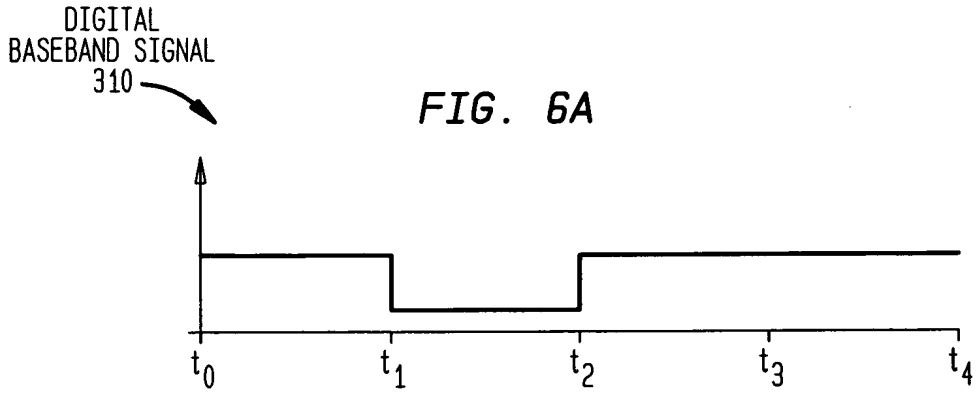



FIG. 6A

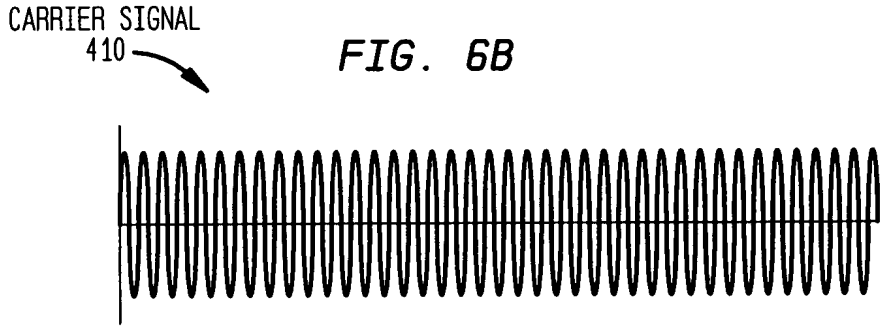



FIG. 6B

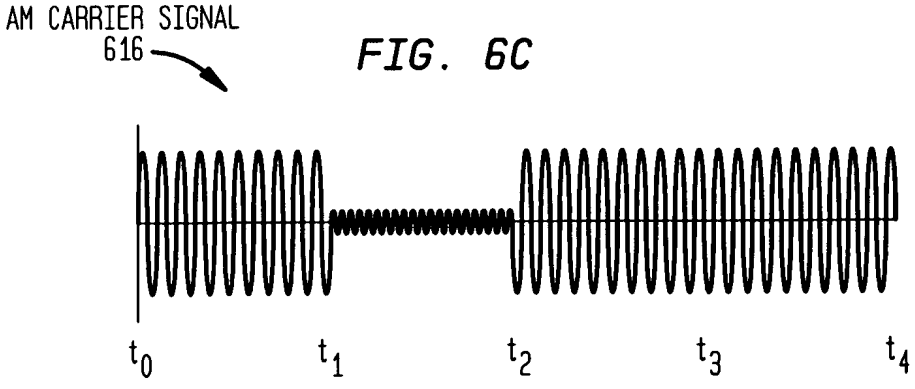



FIG. 6C

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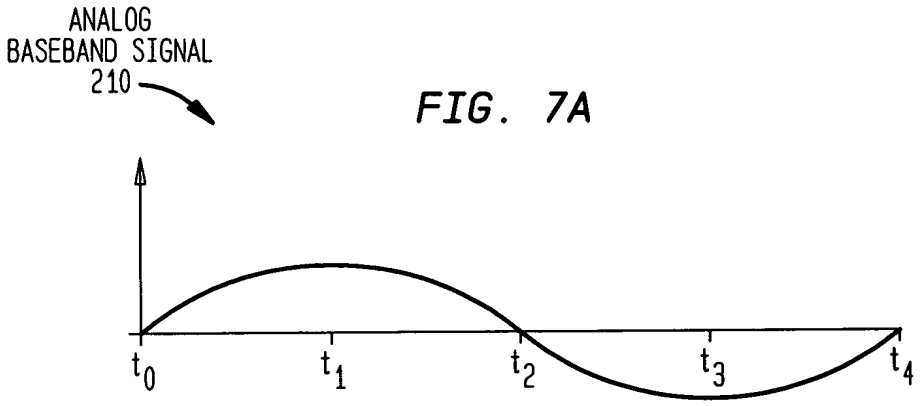


FIG. 7A

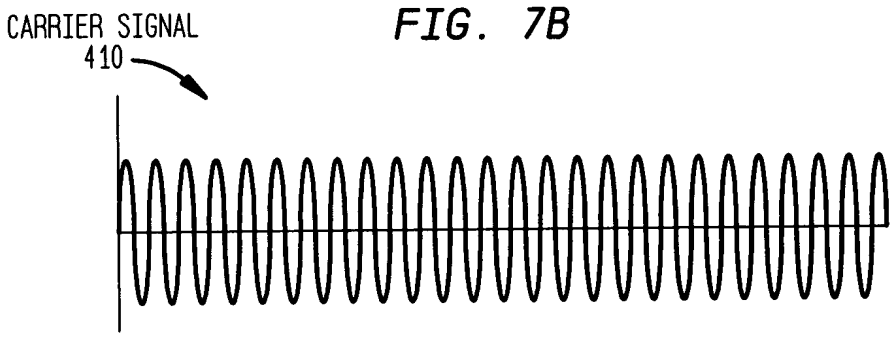


FIG. 7B

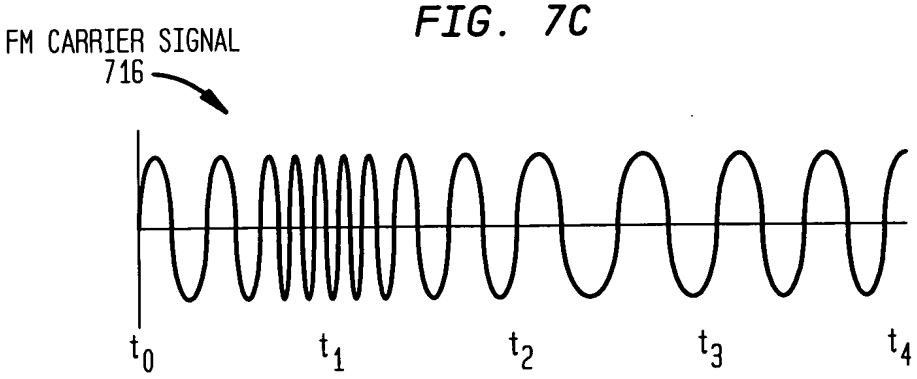


FIG. 7C

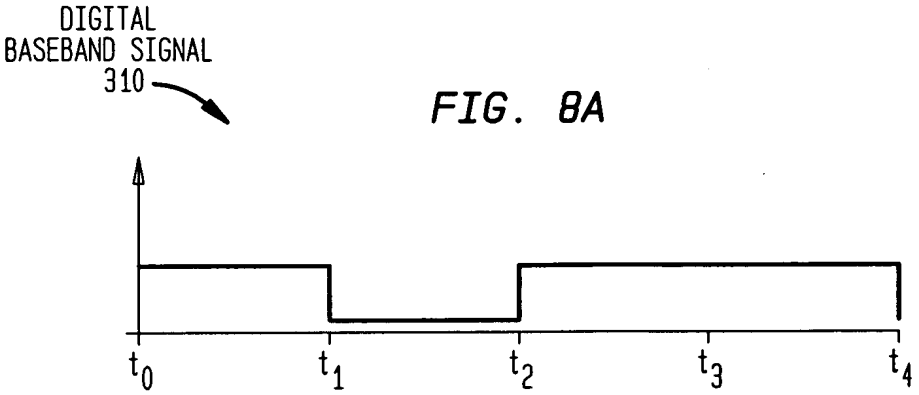


FIG. 8A

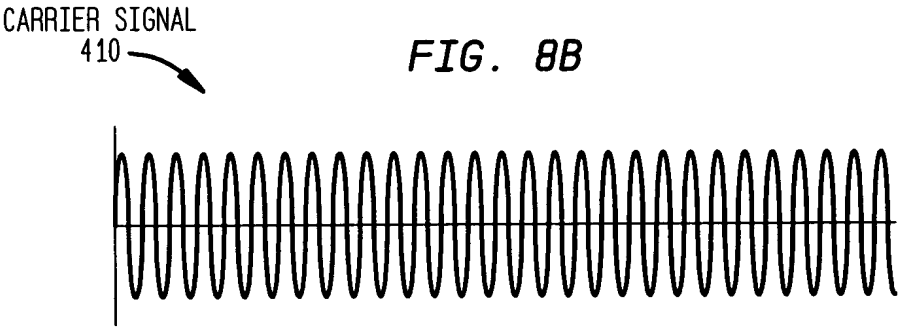


FIG. 8B

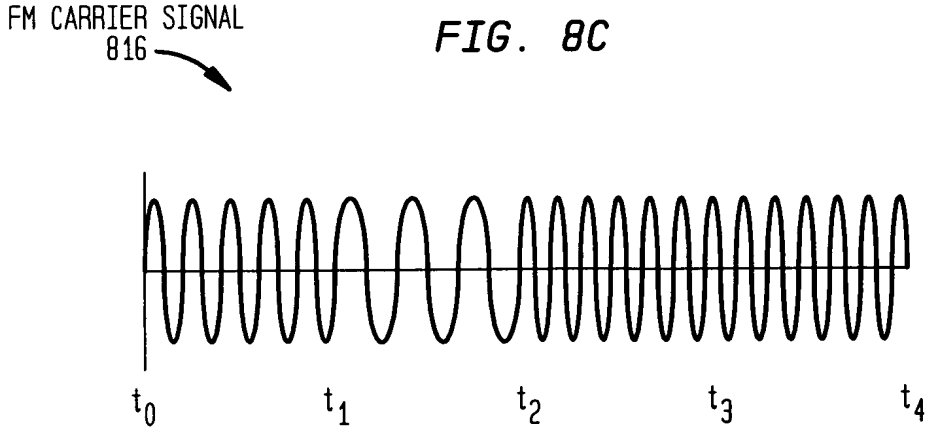


FIG. 8C

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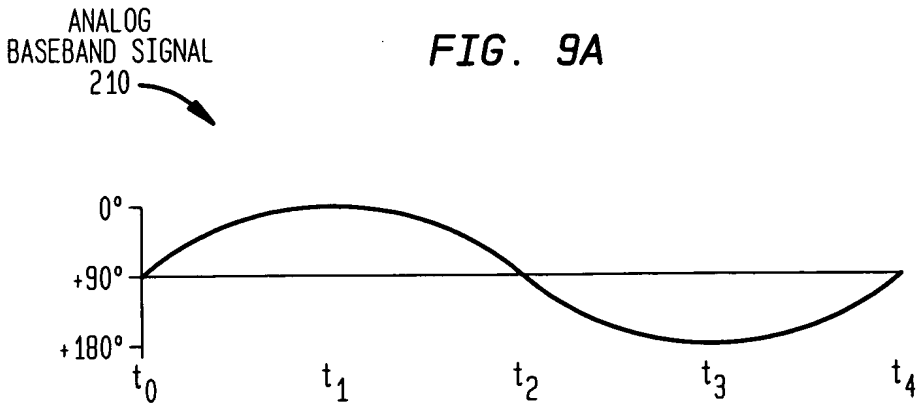


FIG. 9A

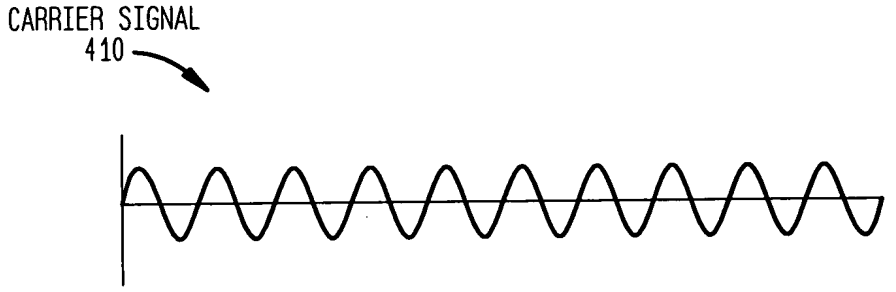


FIG. 9B

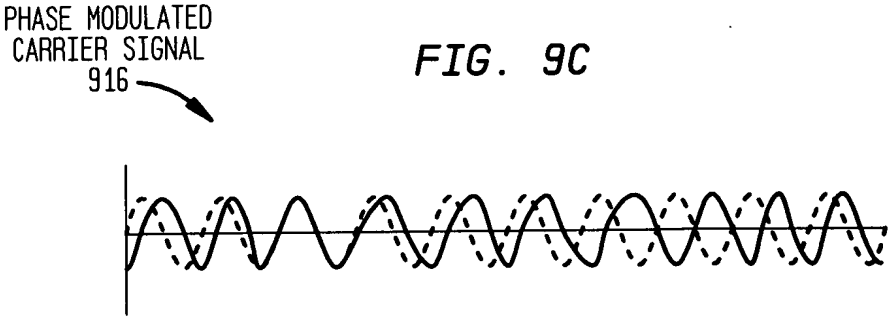


FIG. 9C

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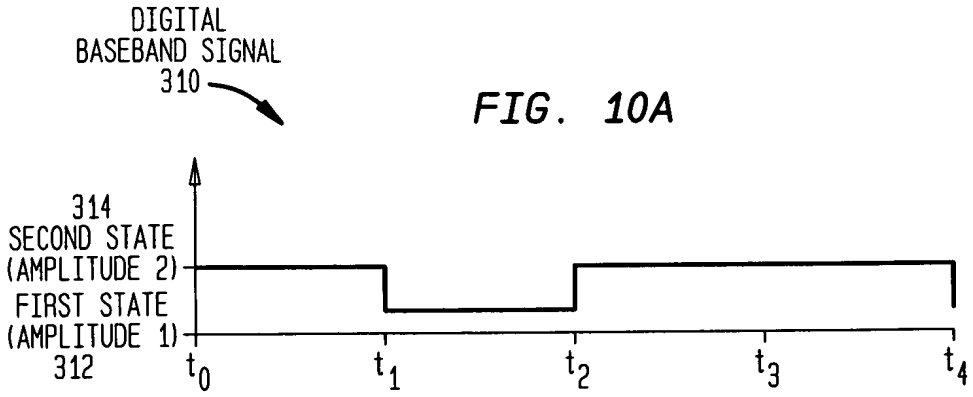


FIG. 10A

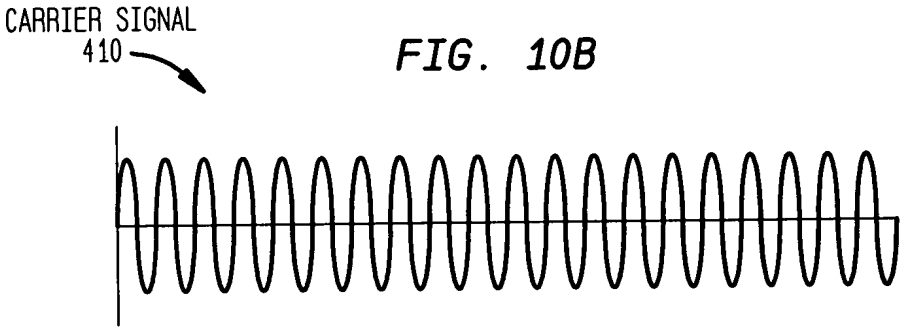


FIG. 10B

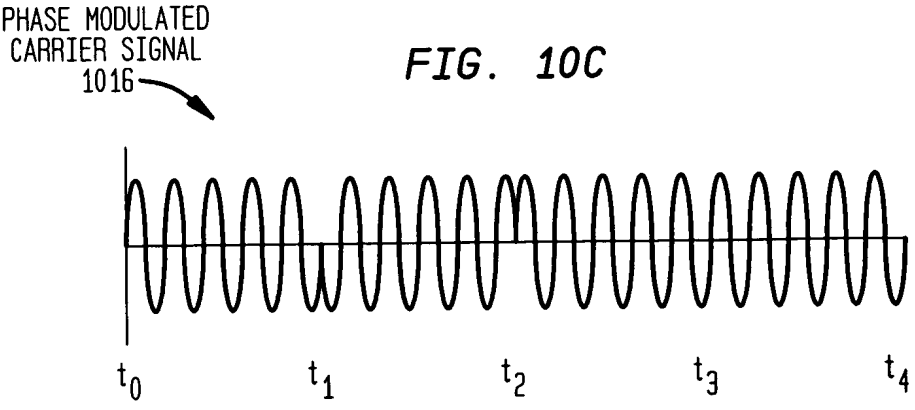


FIG. 10C

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FIG. 11

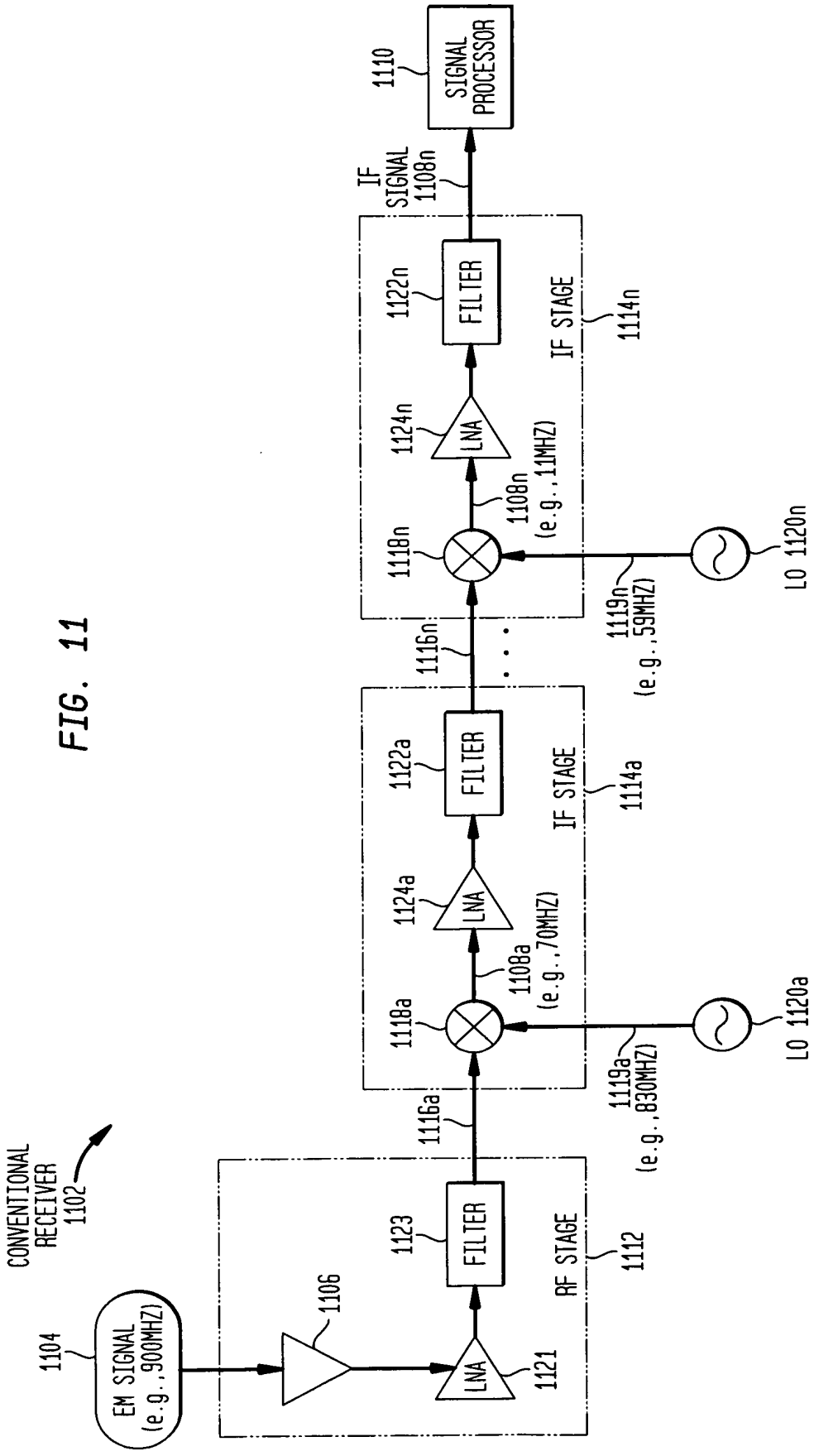

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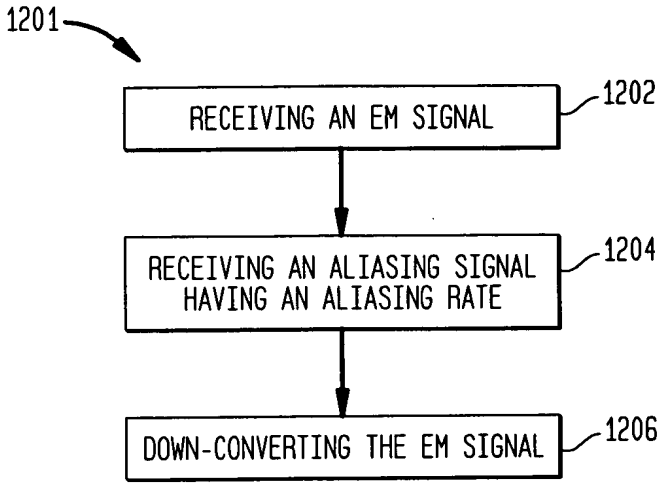
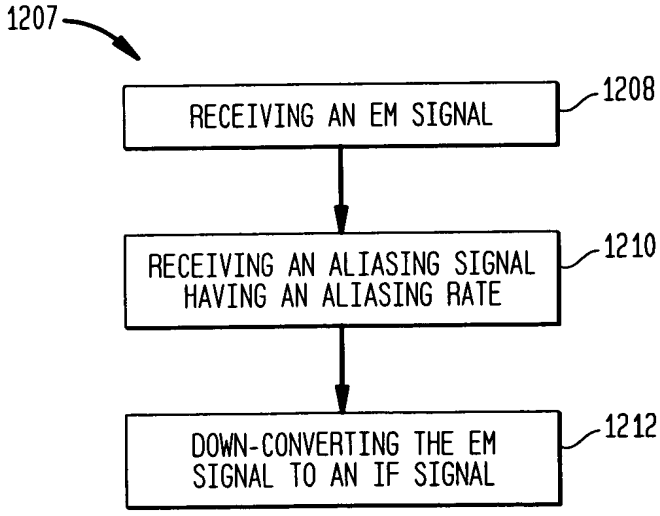
FIG. 12A




GENERIC DOWN-CONVERTING FLOWCHART

FIG. 12B




DOWN-CONVERTING AN EM SIGNAL TO AN IF SIGNAL

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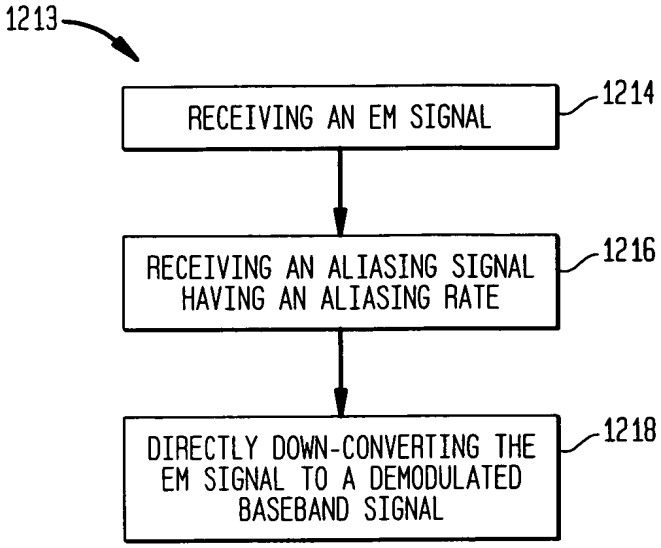
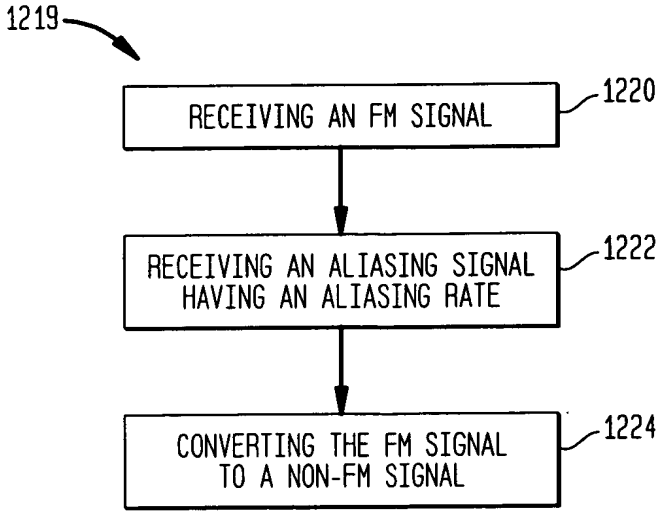
FIG. 12C




DIRECTLY DOWN-CONVERTING AN EM SIGNAL TO A DEMODULATED BASEBAND SIGNAL

FIG. 12D




MODULATION CONVERSION

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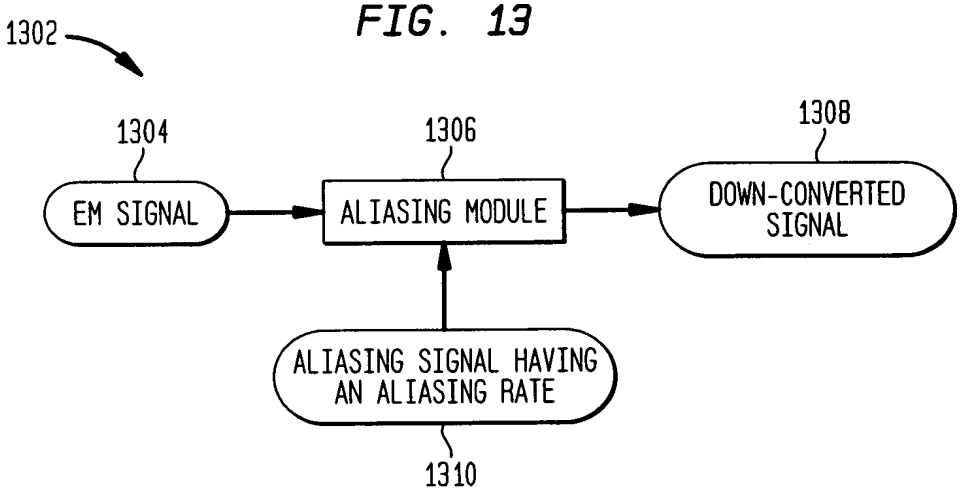
FIG. 13




GENERIC DOWN-CONVERTING SYSTEM

FIG. 14A

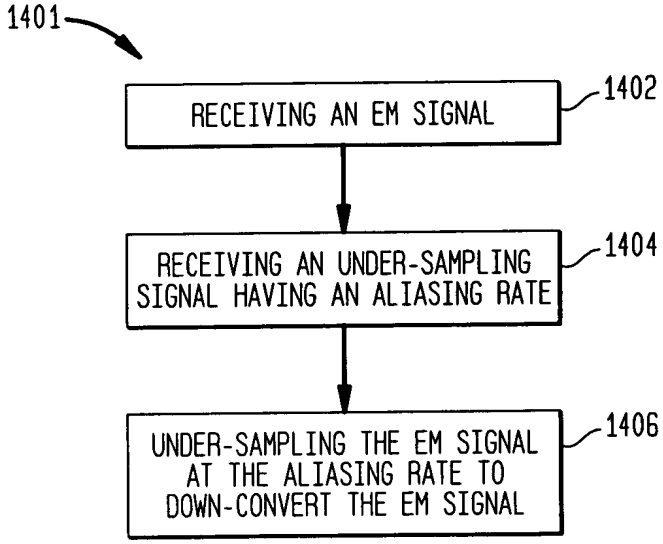


FIG. 14B

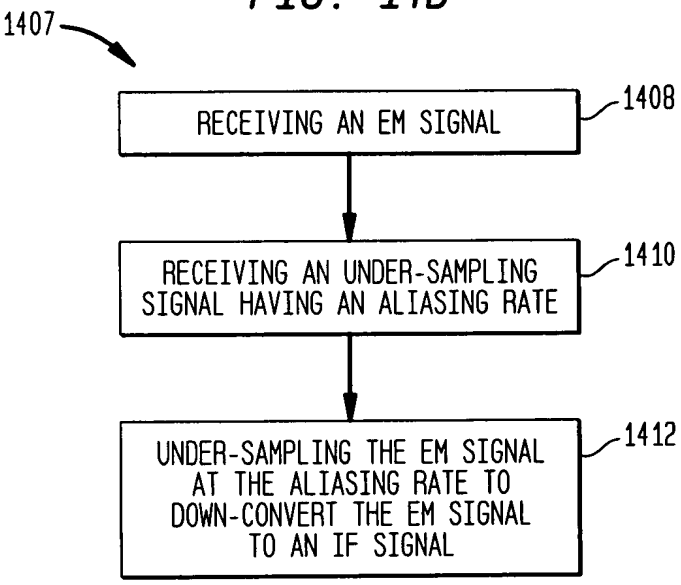



FIG. 14C

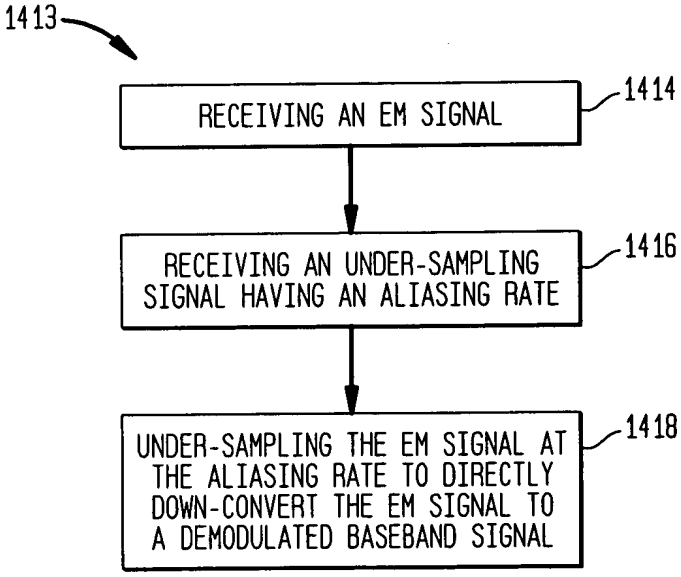


FIG. 14D

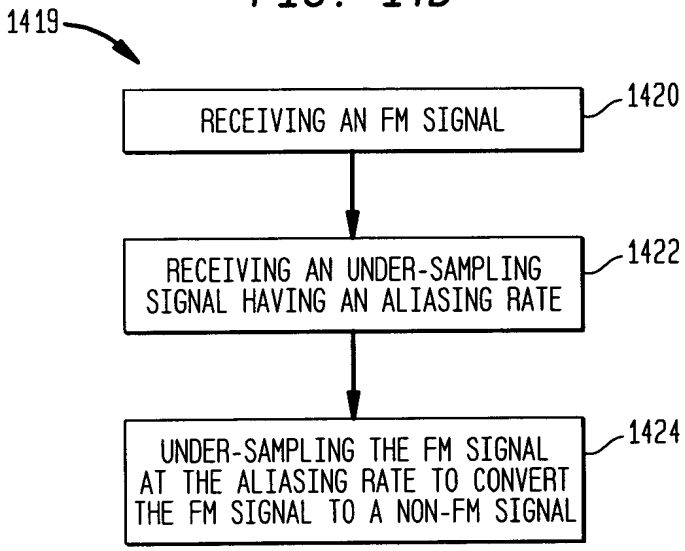

1419
RECEIVING AN FM SIGNAL
1420
RECEIVING AN UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
1422
UNDER-SAMPLING THE FM SIGNAL AT THE ALIASING RATE TO CONVERT THE FM SIGNAL TO A NON-FM SIGNAL
1424

FIG. 15E

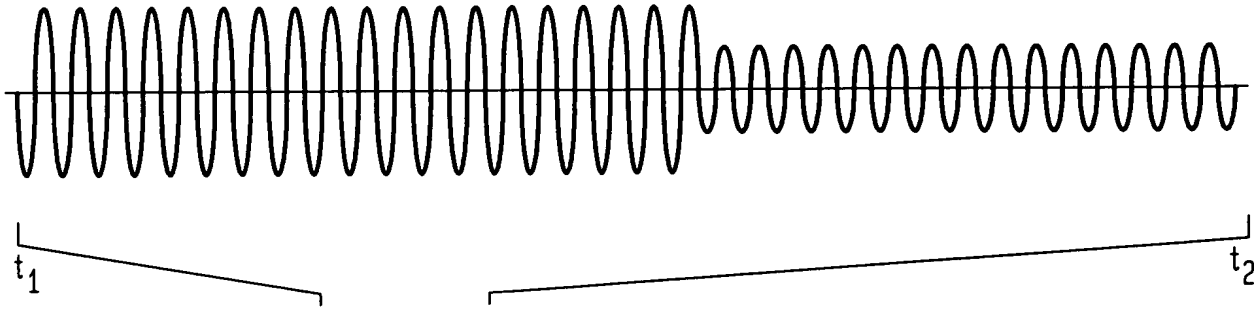



FIG. 15A

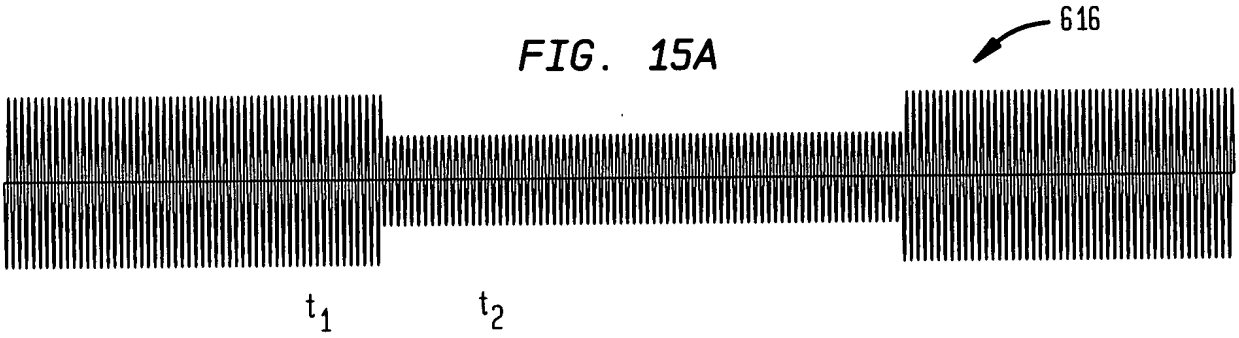



FIG. 15B

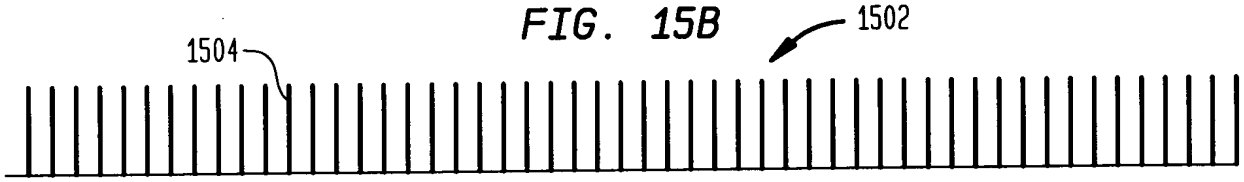



FIG. 15C

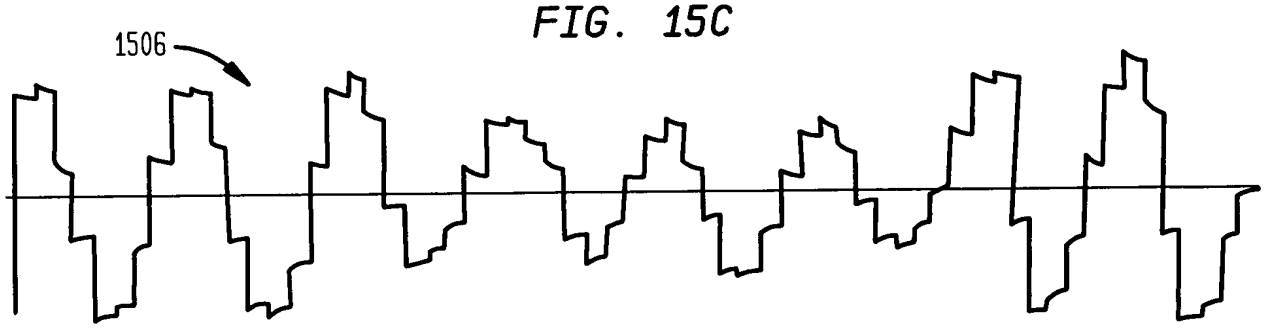



FIG. 15D

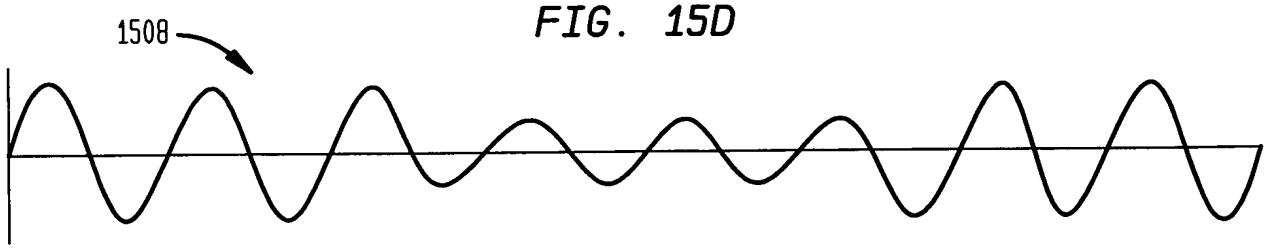


FIG. 16

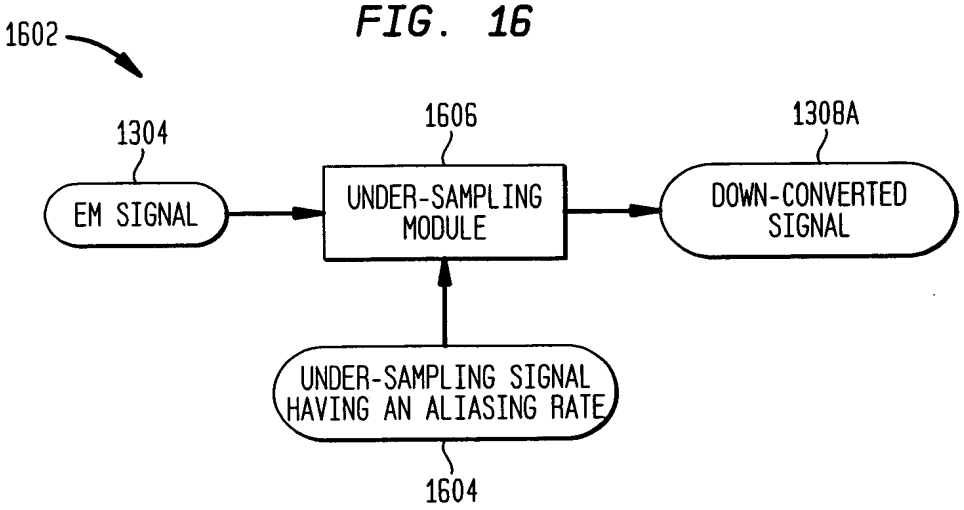

1602
1304
EM SIGNAL
1606
UNDER-SAMPLING MODULE
1308A
DOWN-CONVERTED SIGNAL
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
1604

FIG. 17

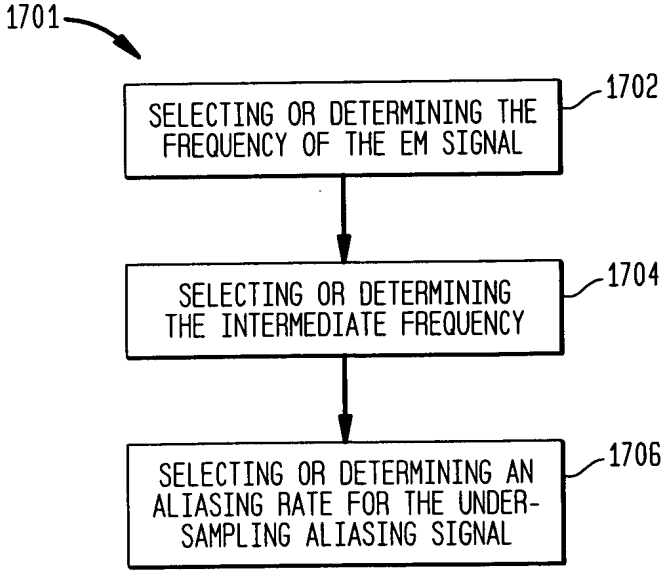

1701
SELECTING OR DETERMINING THE FREQUENCY OF THE EM SIGNAL
1702
SELECTING OR DETERMINING THE INTERMEDIATE FREQUENCY
1704
SELECTING OR DETERMINING AN ALIASING RATE FOR THE UNDER-SAMPLING ALIASING SIGNAL
1706

FIG. 18A

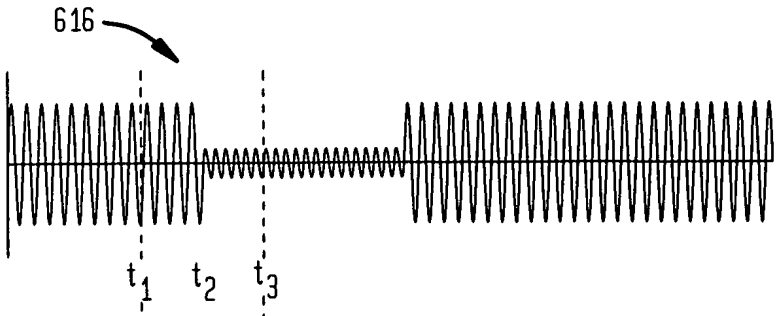



FIG. 18B

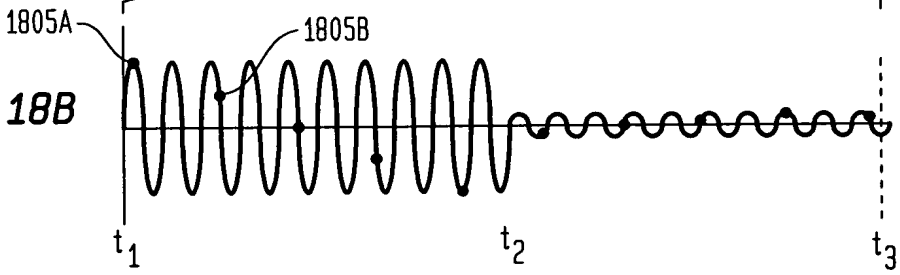



FIG. 18C

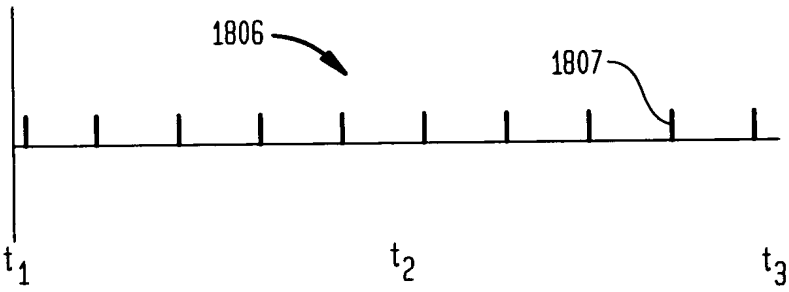



FIG. 18D

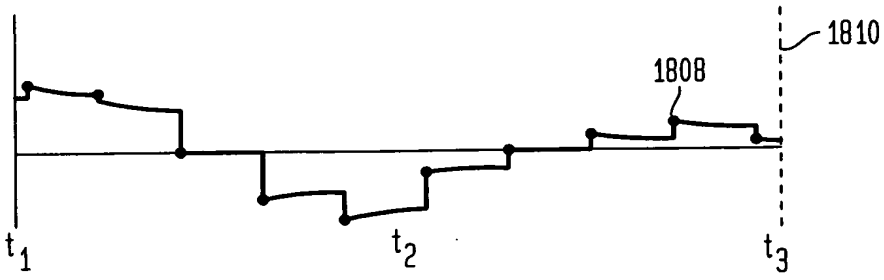



FIG. 18E

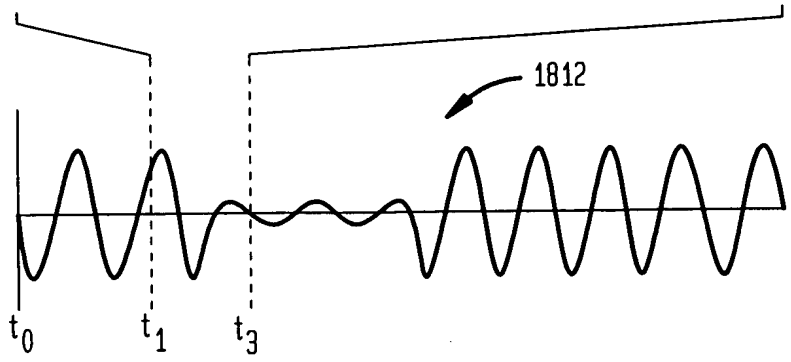


FIG. 19A

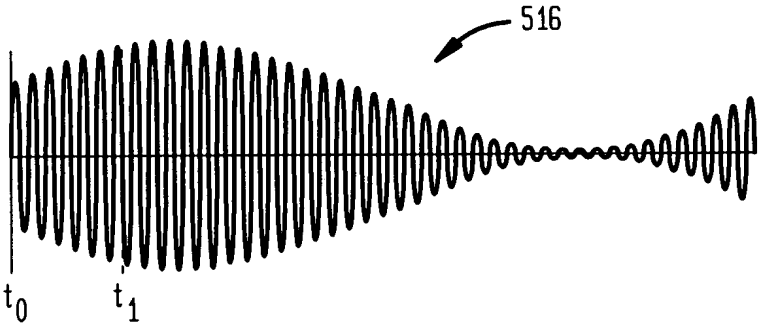



FIG. 19B

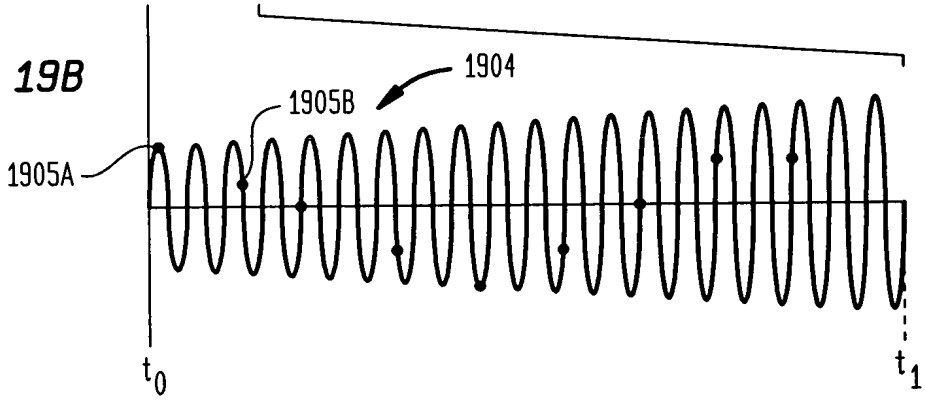



FIG. 19C

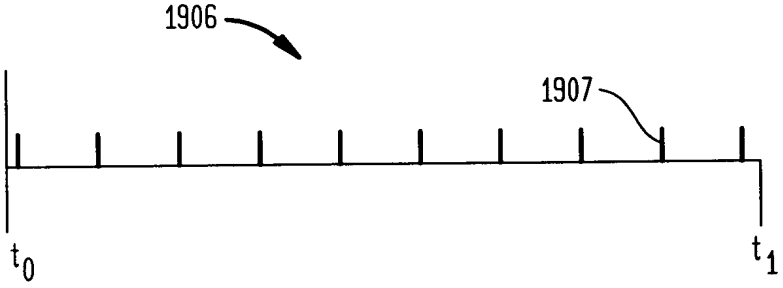



FIG. 19D

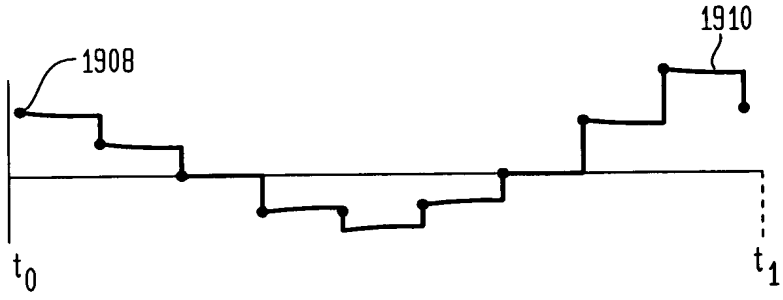



FIG. 19E

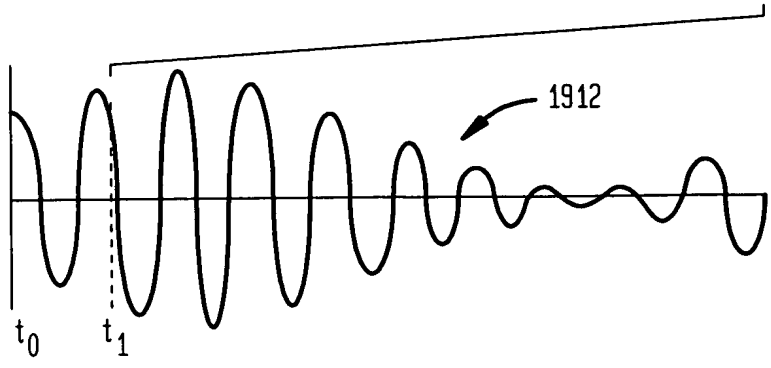


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FIG. 20A

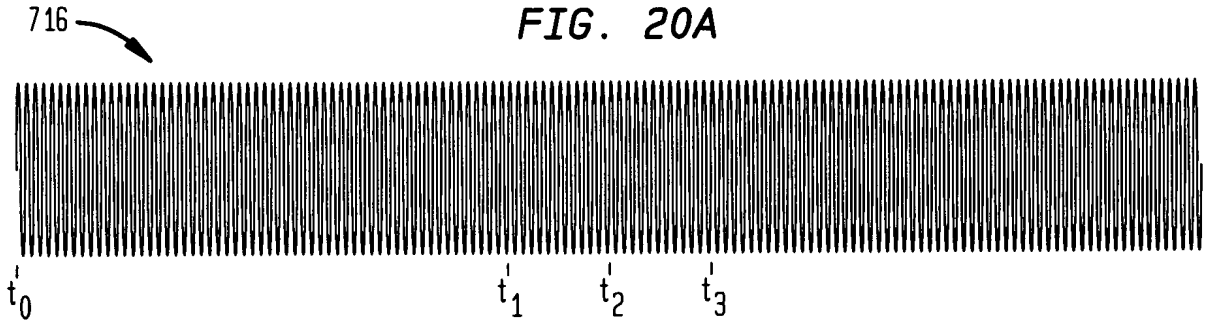



FIG. 20B

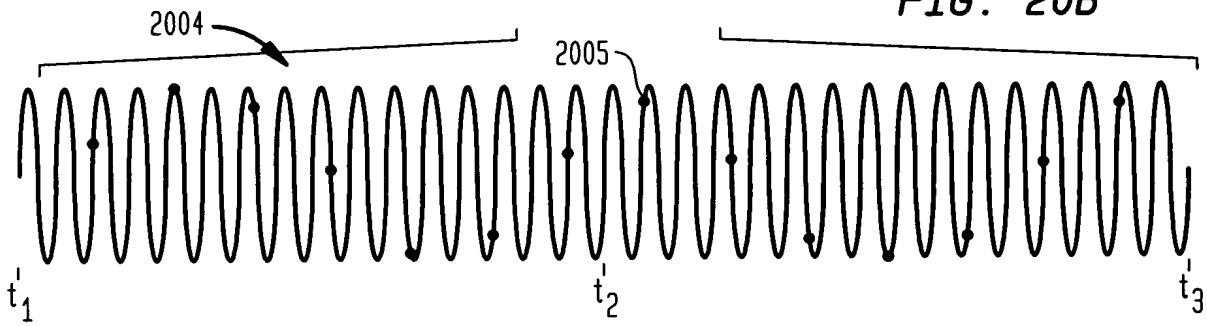



FIG. 20C

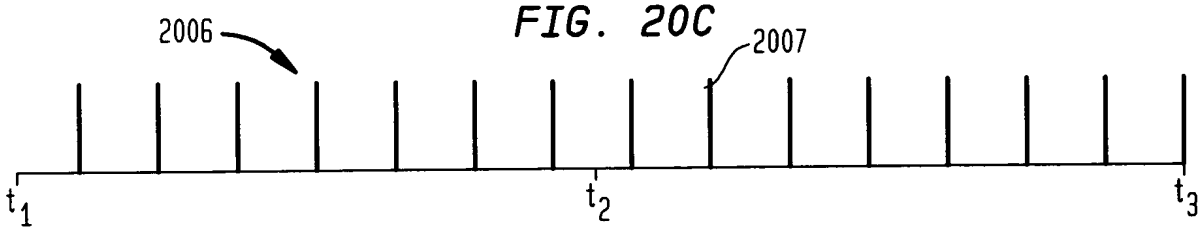



FIG. 20D

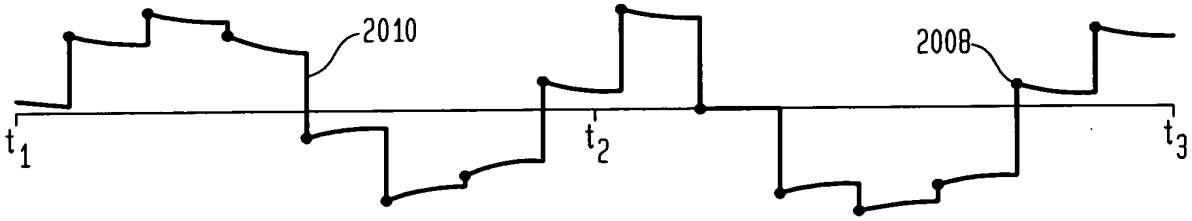



FIG. 20E

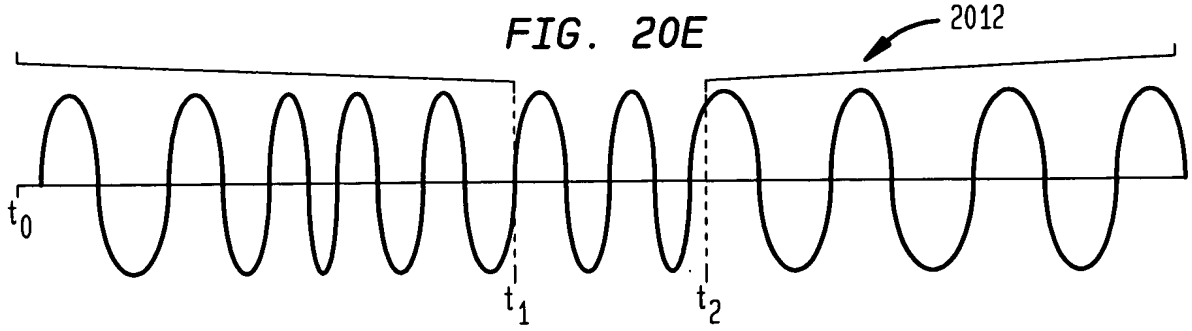


FIG. 21A

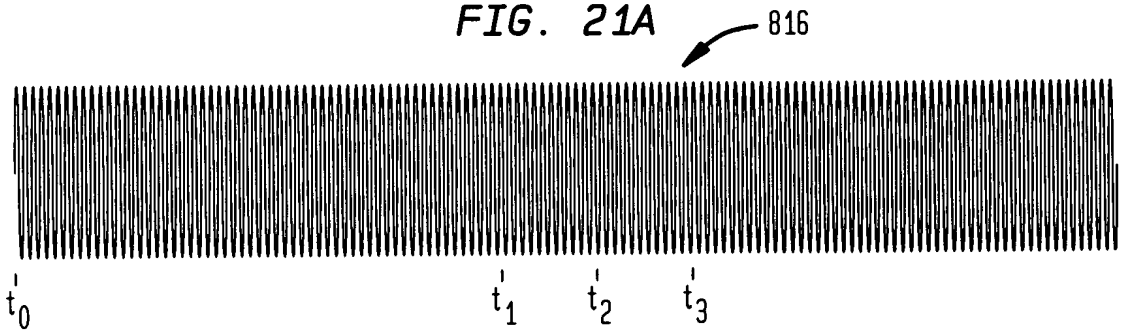



FIG. 21B

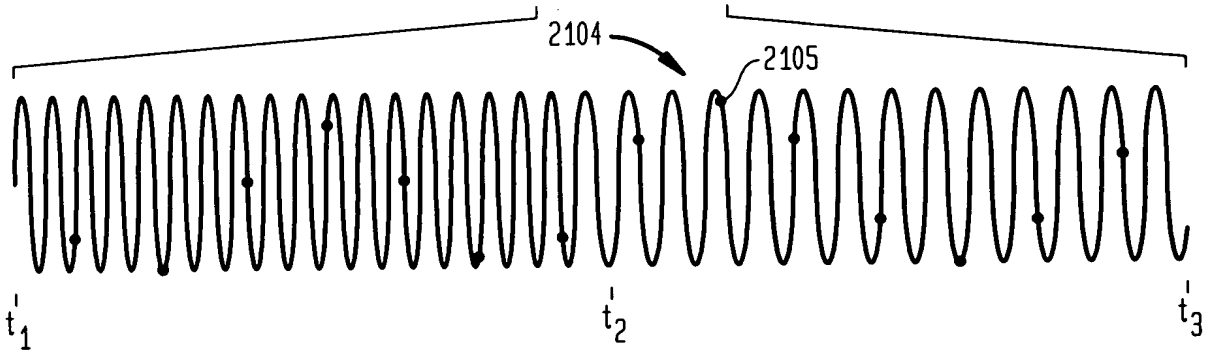



FIG. 21C

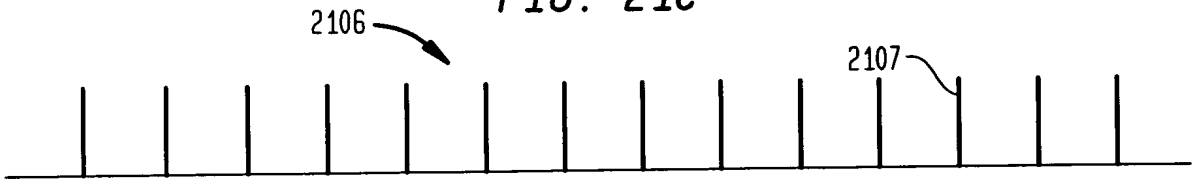



FIG. 21D

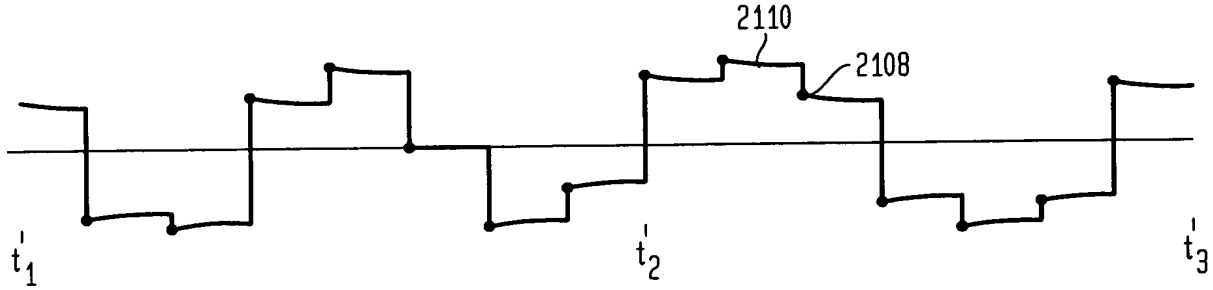



FIG. 21E

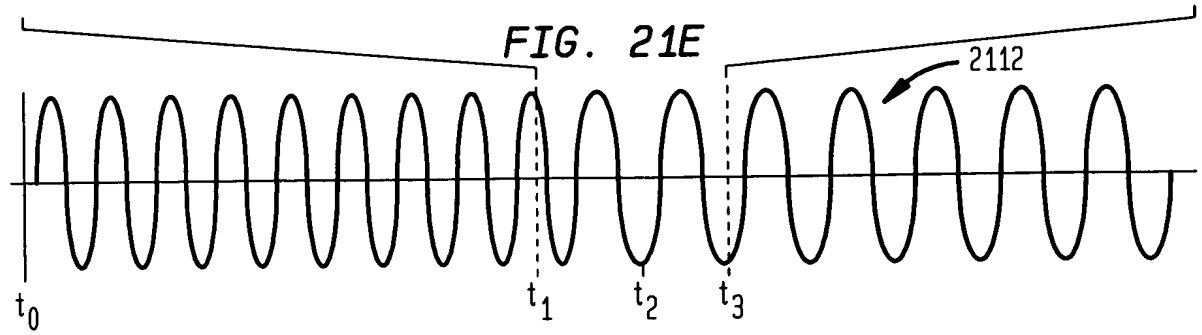


FIG. 22A

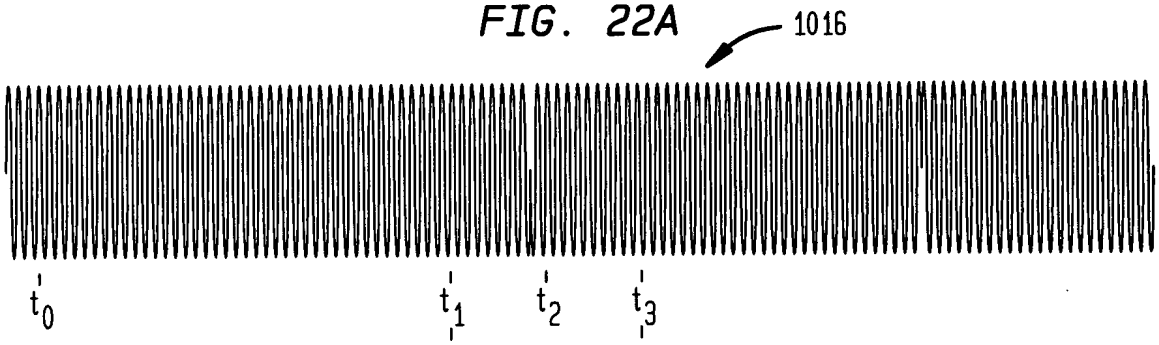



FIG. 22B

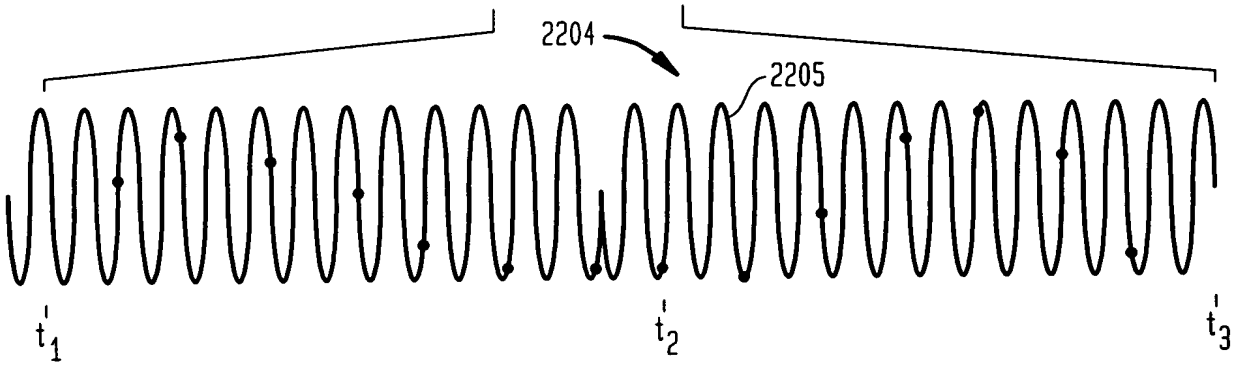



FIG. 22C

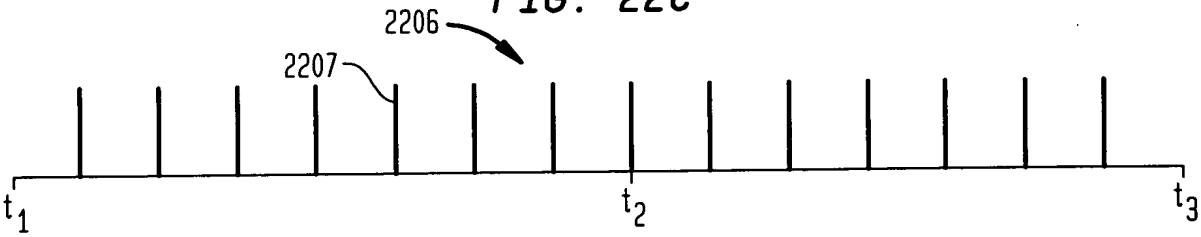



FIG. 22D

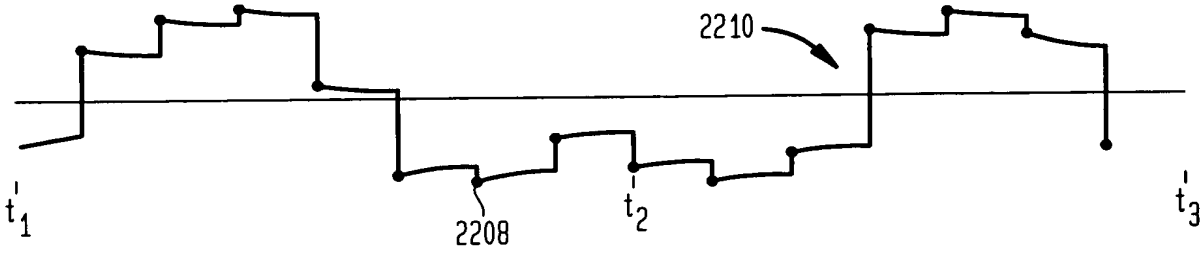



FIG. 22E

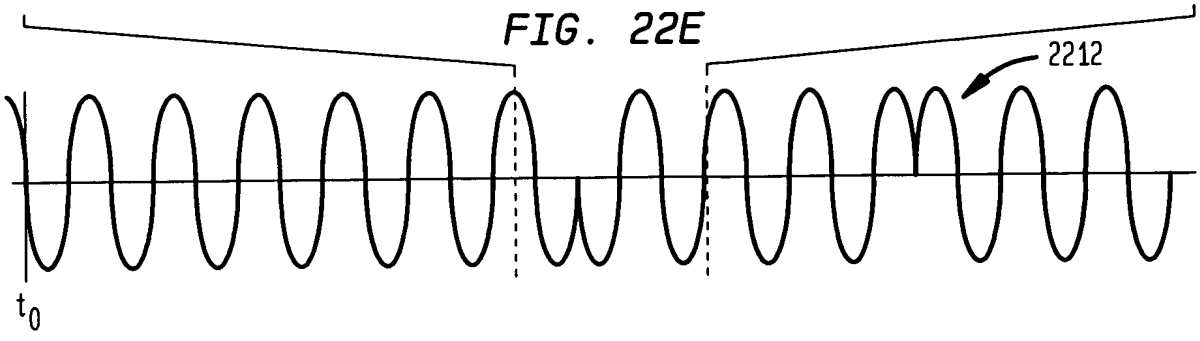


FIG. 23A

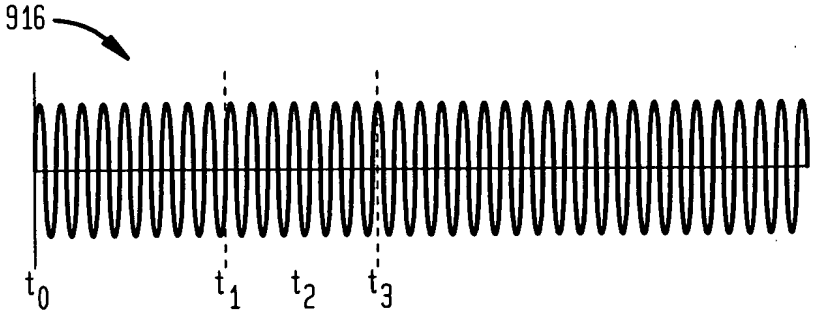



FIG. 23B

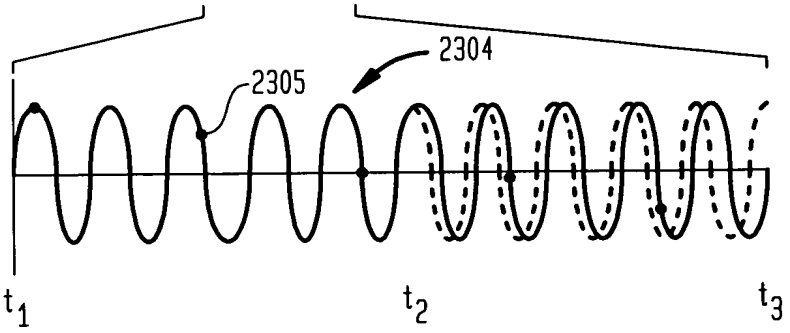



FIG. 23C

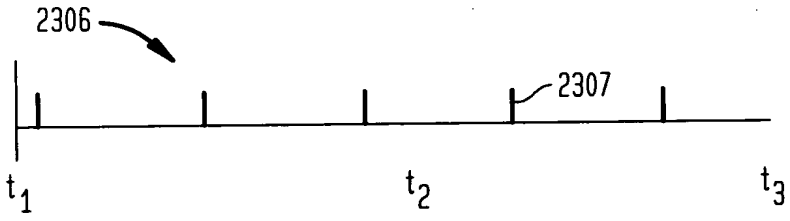



FIG. 23D

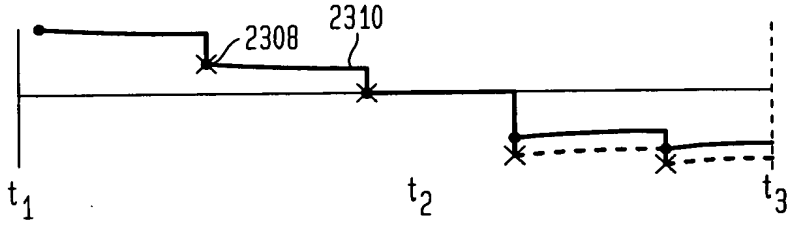
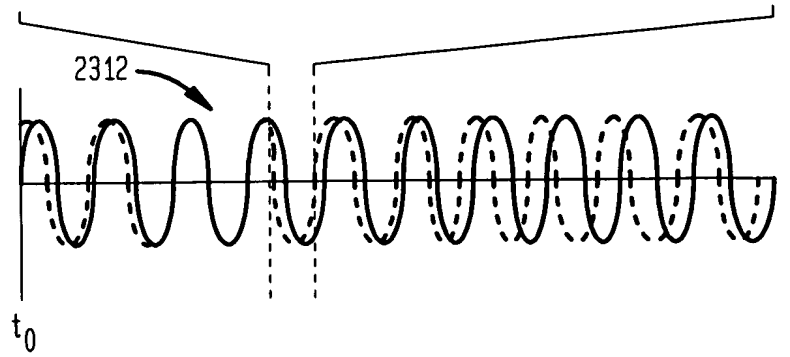



FIG. 23E



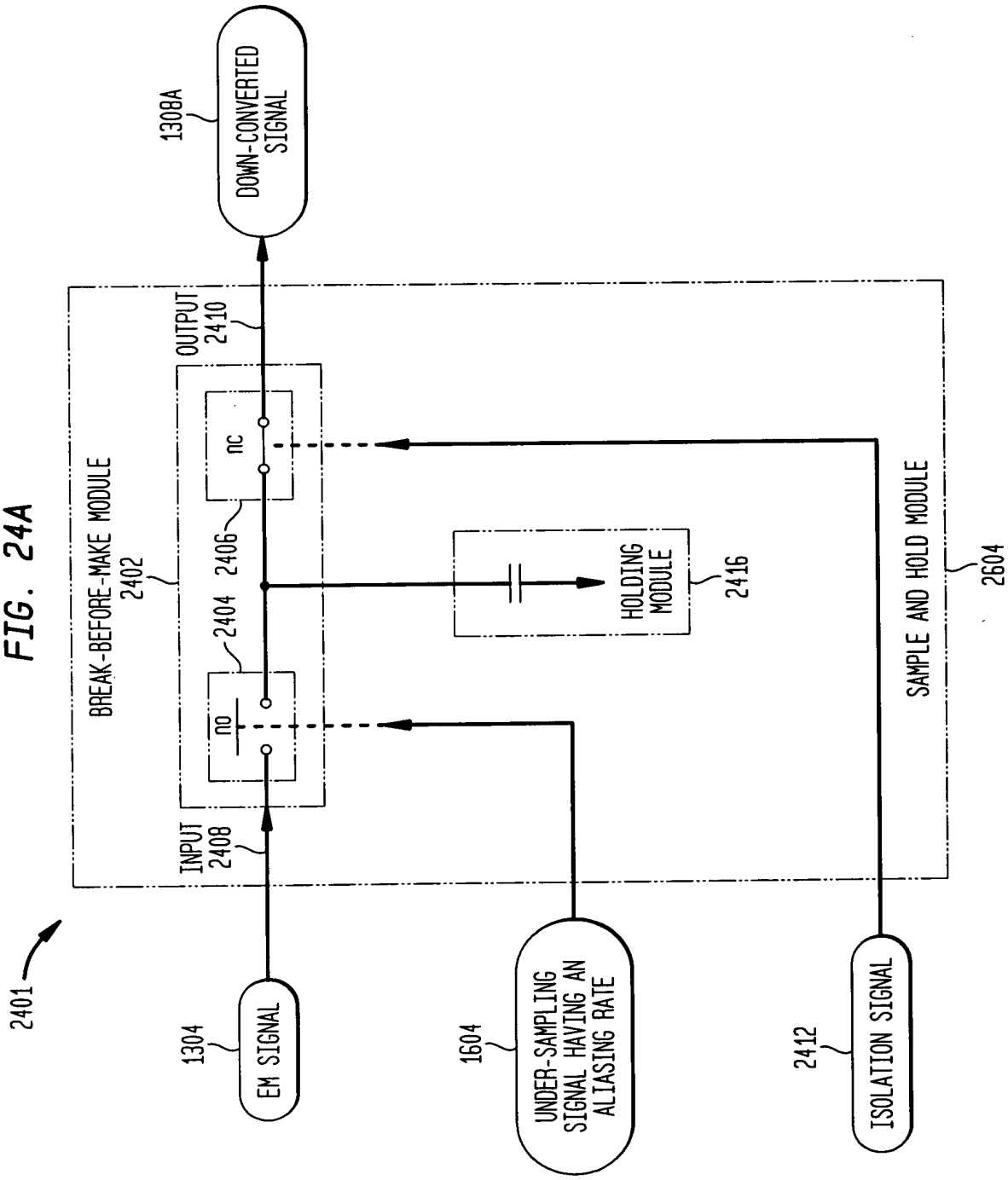

2401
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
2412
ISOLATION SIGNAL
BREAK-BEFORE-MAKE MODULE
2402
INPUT
2408
OUTPUT
2410
no
nc
2404
2406
HOLDING MODULE
2416
SAMPLE AND HOLD MODULE
2604
1308A
DOWN-CONVERTED SIGNAL

FIG. 24A

FIG. 24B

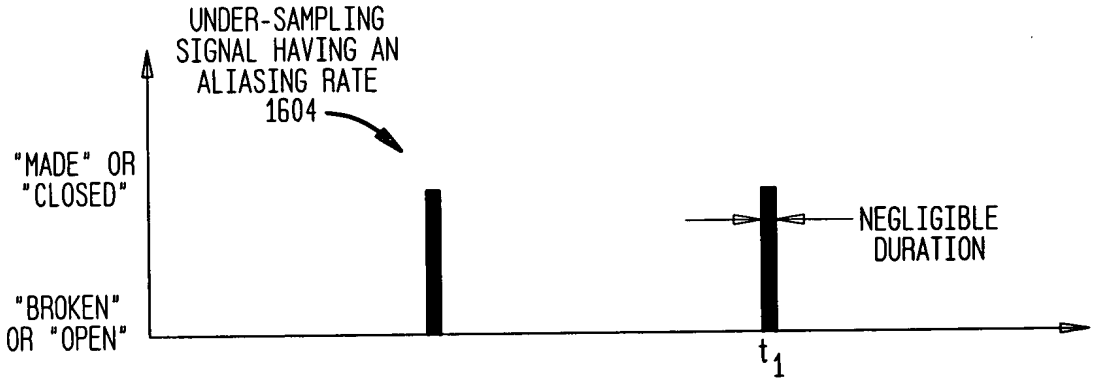
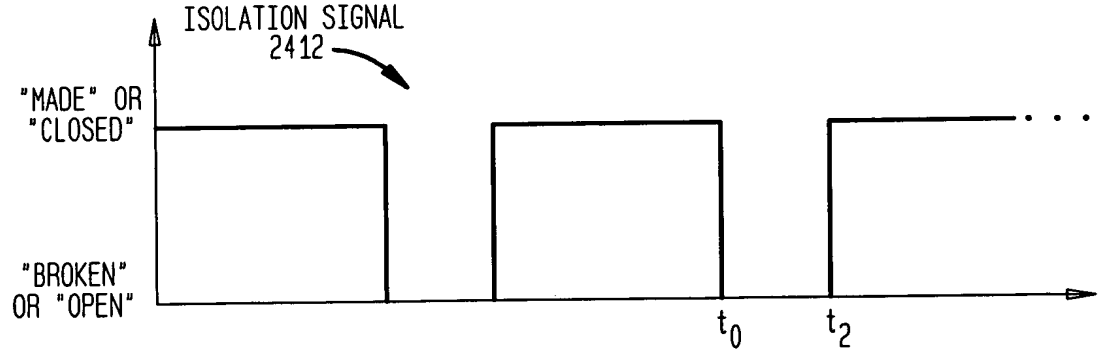



FIG. 24C



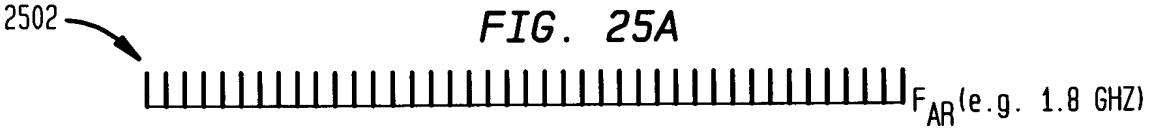



FIG. 25A

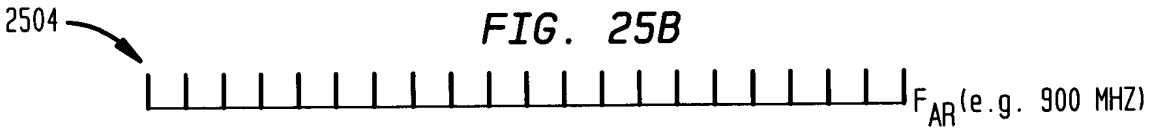



FIG. 25B

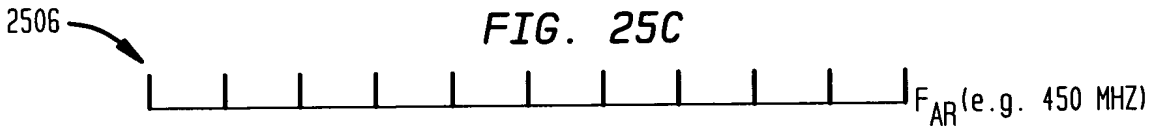



FIG. 25C

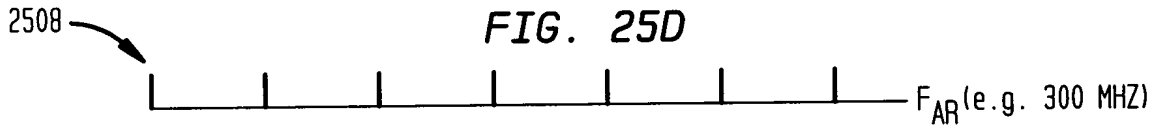



FIG. 25D

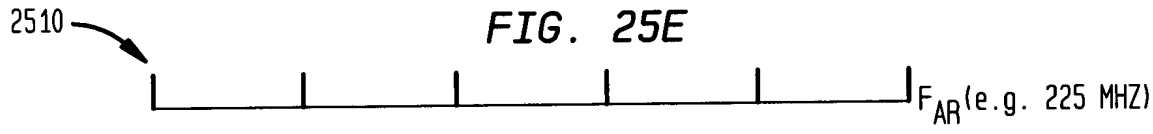



FIG. 25E

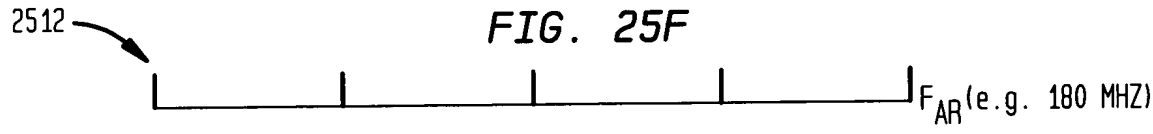



FIG. 25F

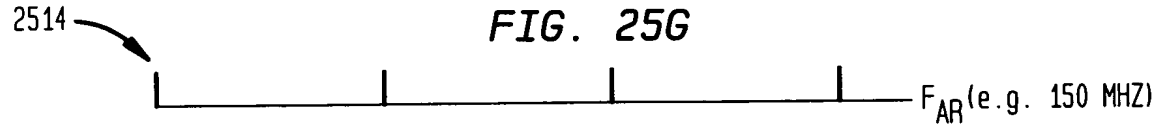



FIG. 25G

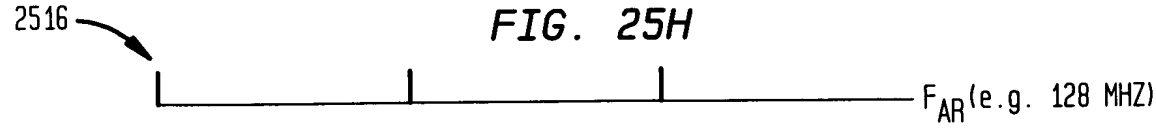



FIG. 25H

FIG. 26A

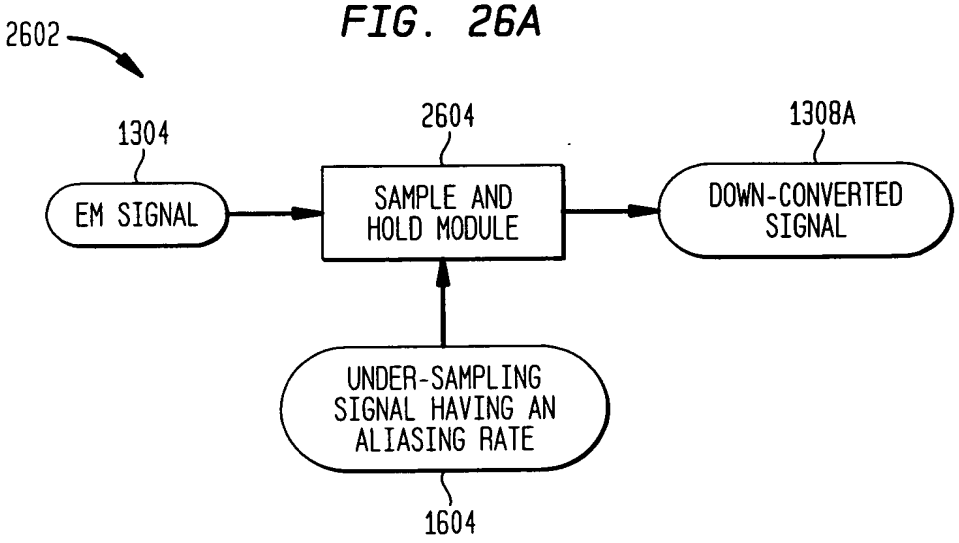
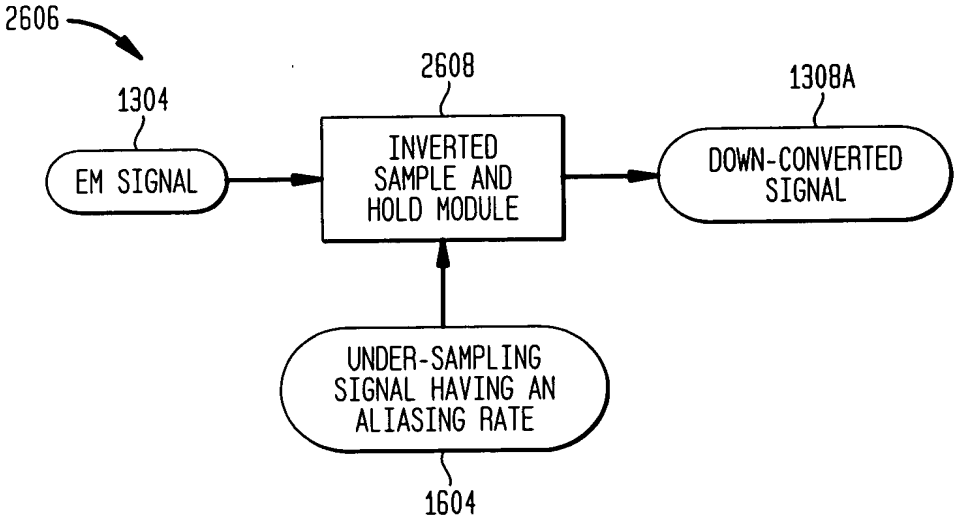



FIG. 26B



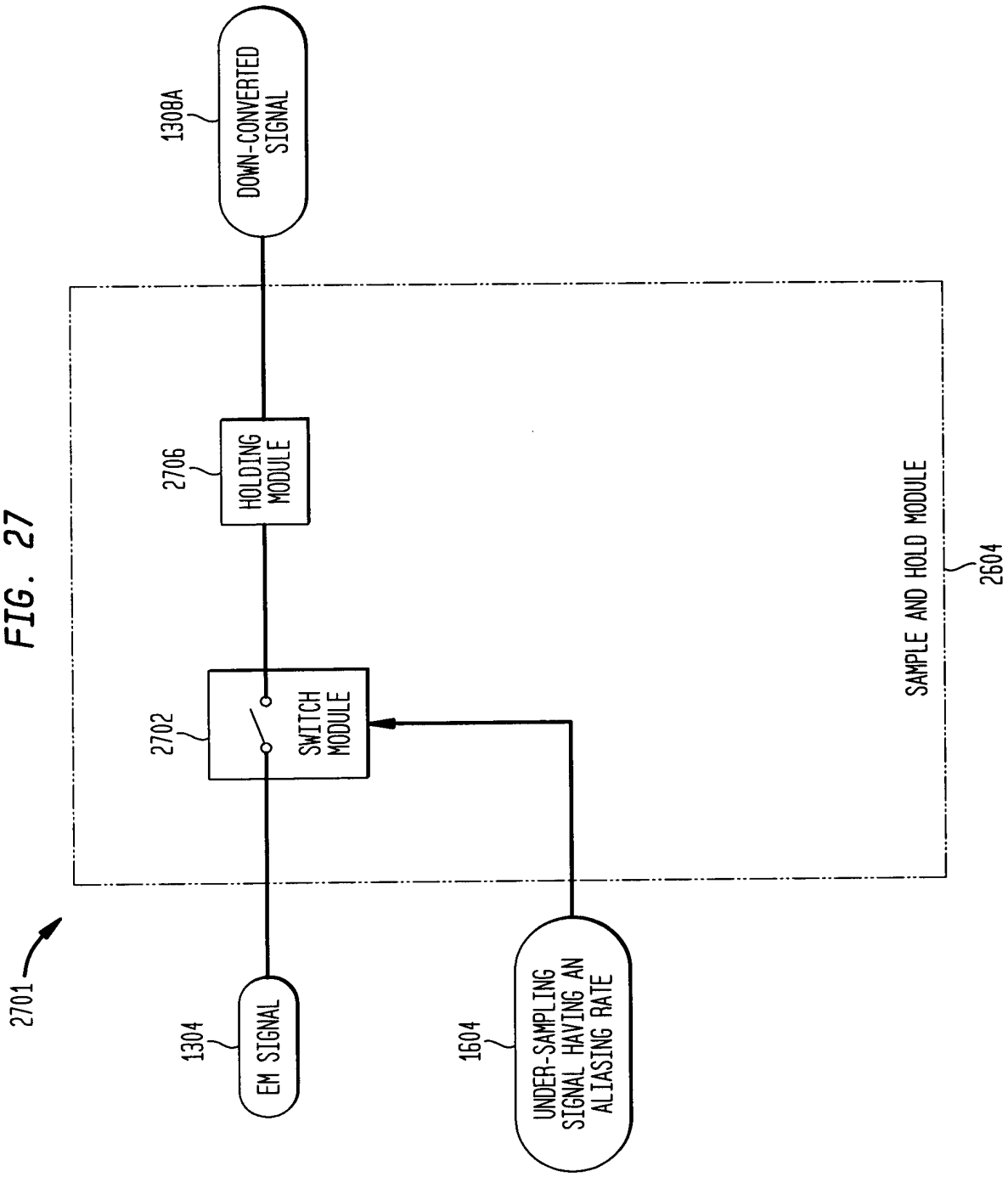

2701
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
2702
SWITCH MODULE
2706
HOLDING MODULE
1308A
DOWN-CONVERTED SIGNAL
SAMPLE AND HOLD MODULE
2604

FIG. 27

FIG. 28A

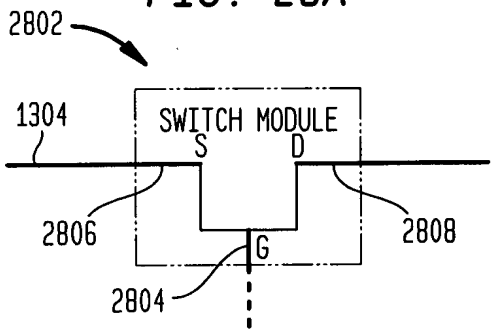



FIG. 28B

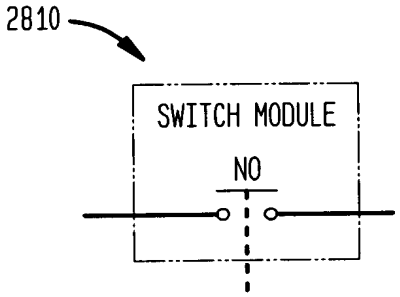



FIG. 28C

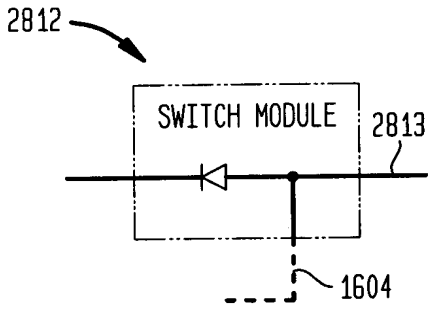



FIG. 28D

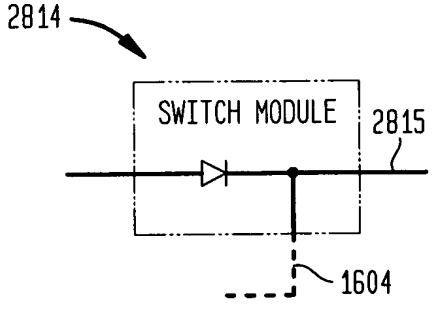


FIG. 29A

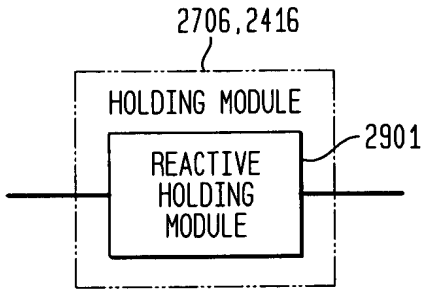



FIG. 29B

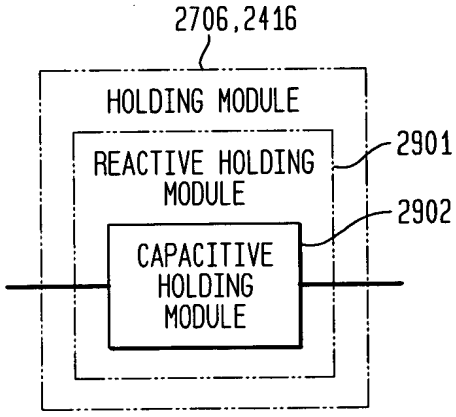



FIG. 29C

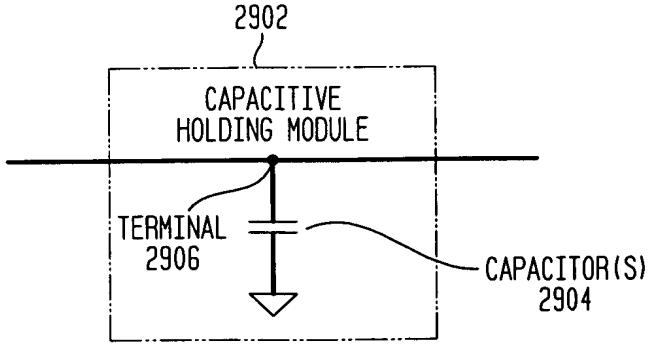


FIG. 29D

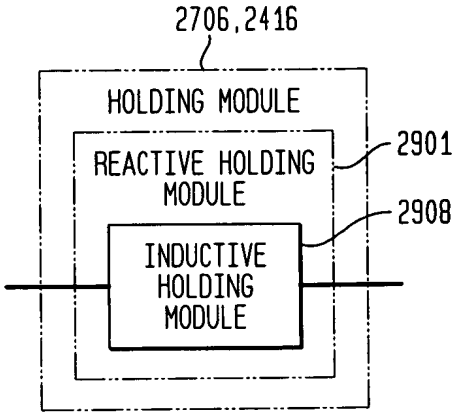



FIG. 29E

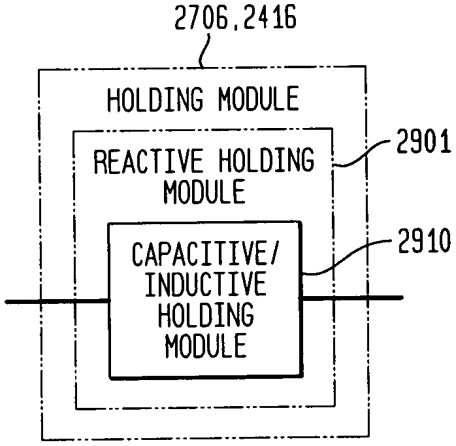



FIG. 29F

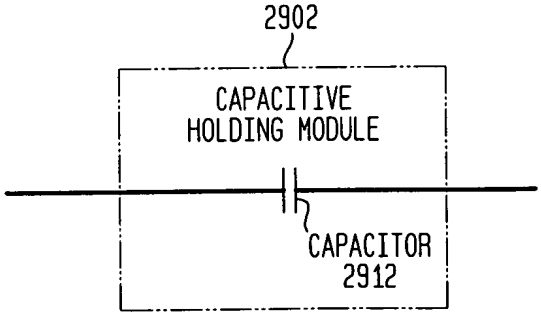


FIG. 29G

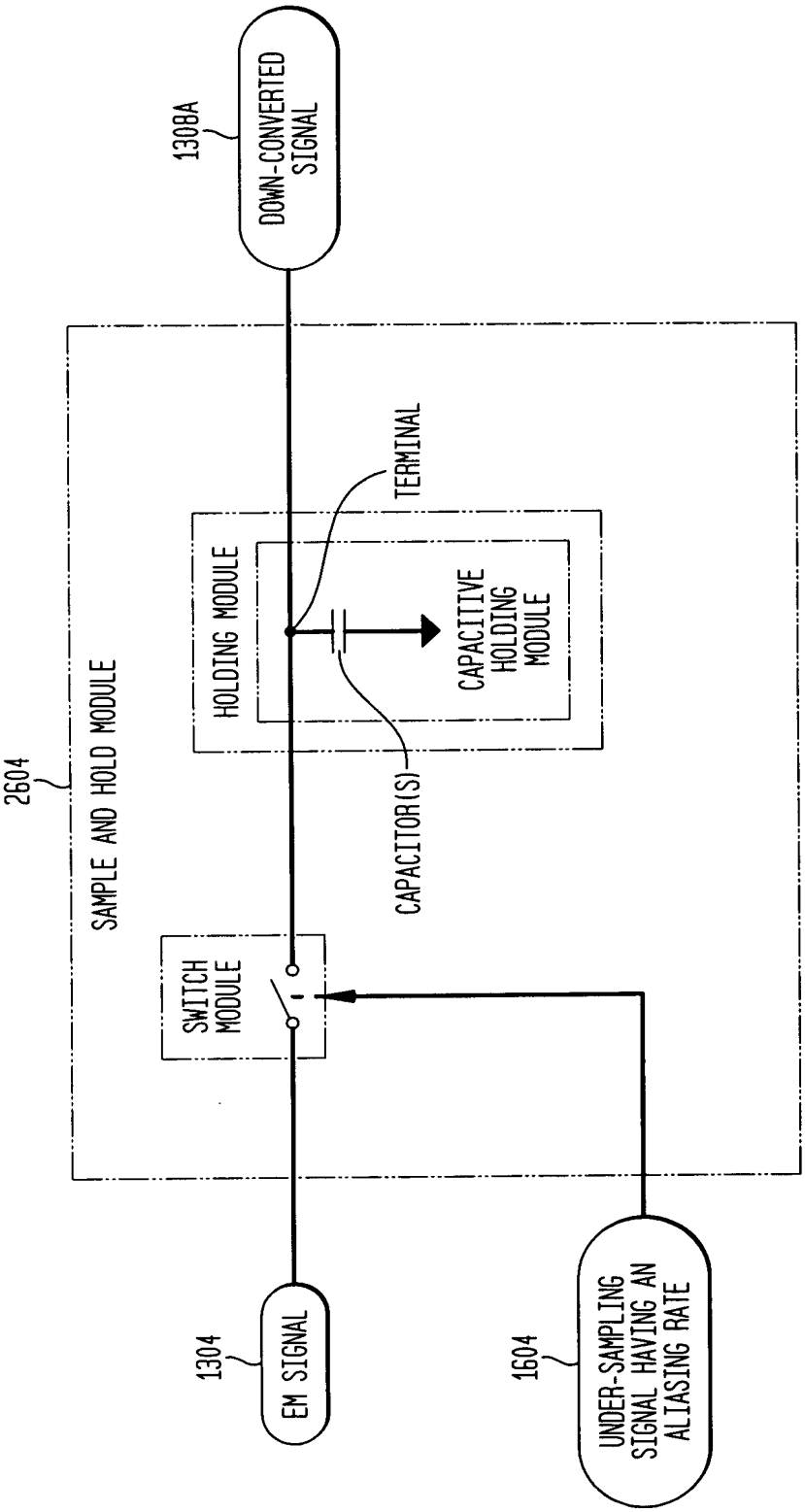
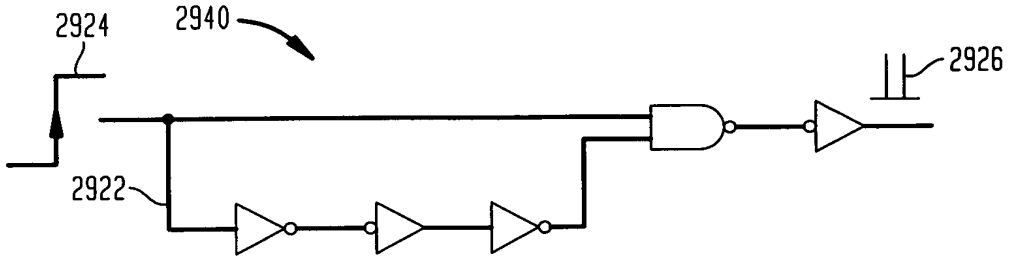
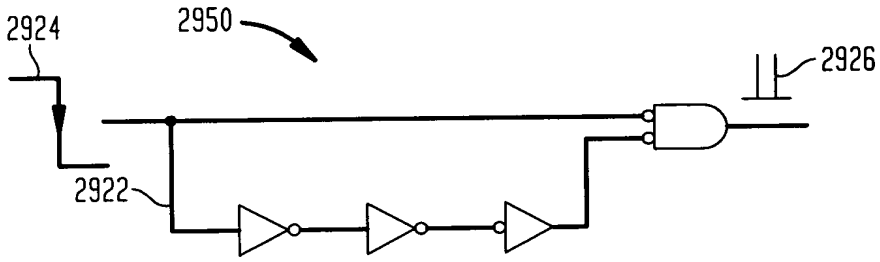

1308A
DOWN-CONVERTED SIGNAL
2604
SAMPLE AND HOLD MODULE
HOLDING MODULE
TERMINAL
CAPACITIVE HOLDING MODULE
CAPACITOR(S)
SWITCH MODULE
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE

FIG. 29H




A. RISING EDGE PULSE GENERATOR

FIG. 29I




B. FALLING-EDGE PULSE GENERATOR

FIG. 29J

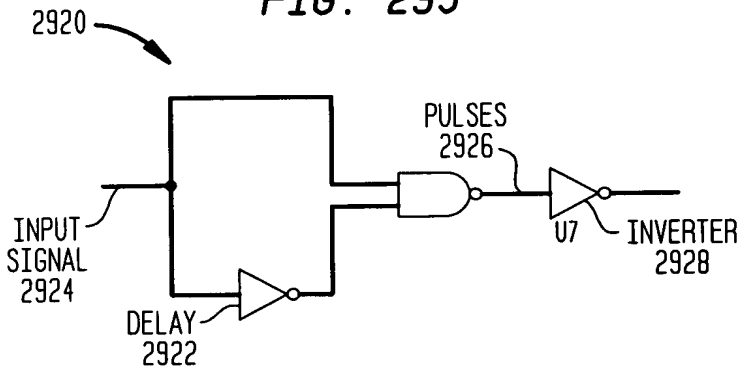


FIG. 29K

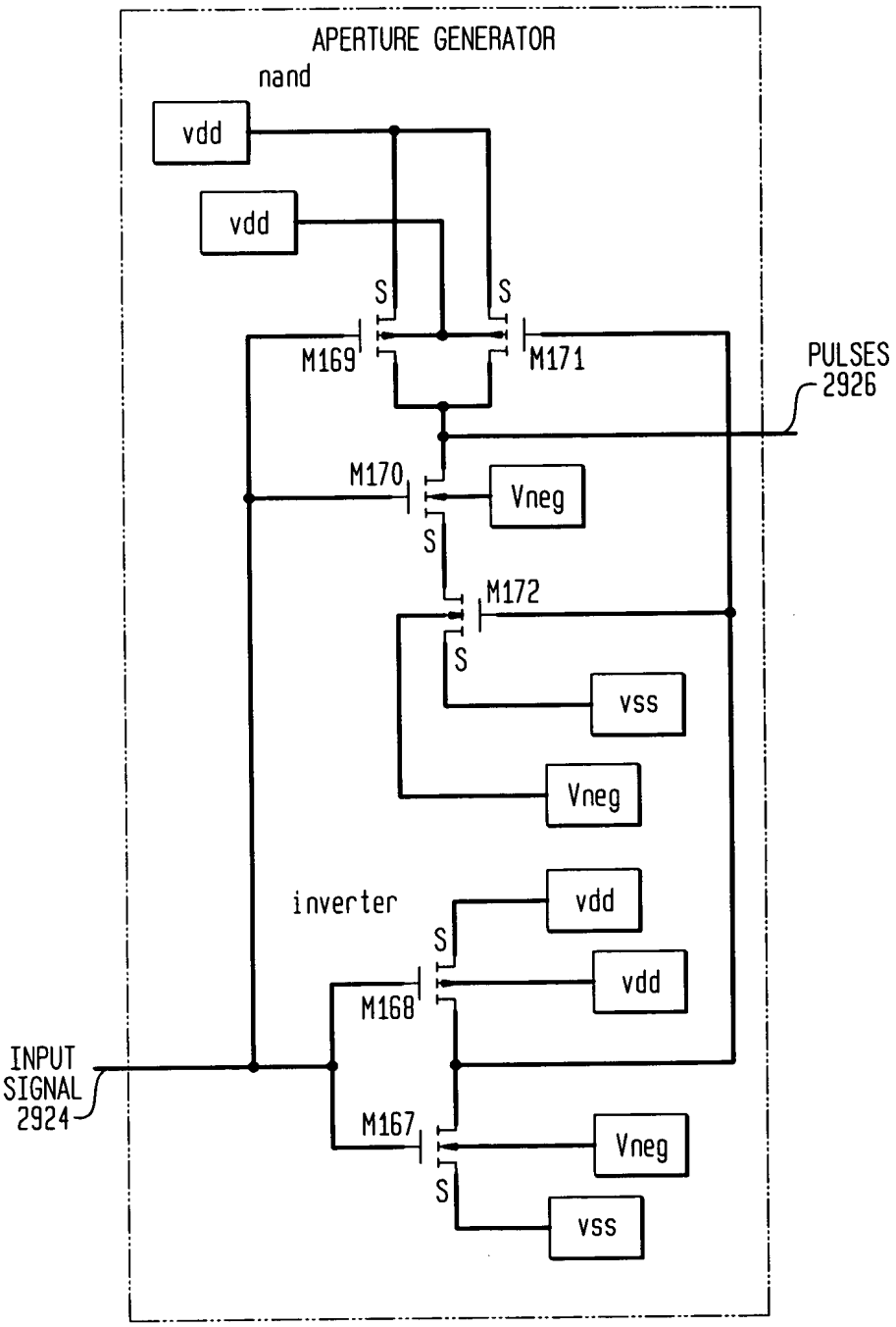
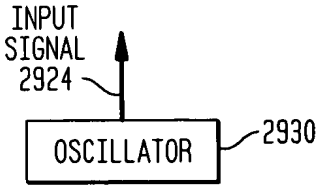



FIG. 29L



Replacement Sheet
Sheet 33 of 284
Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 30

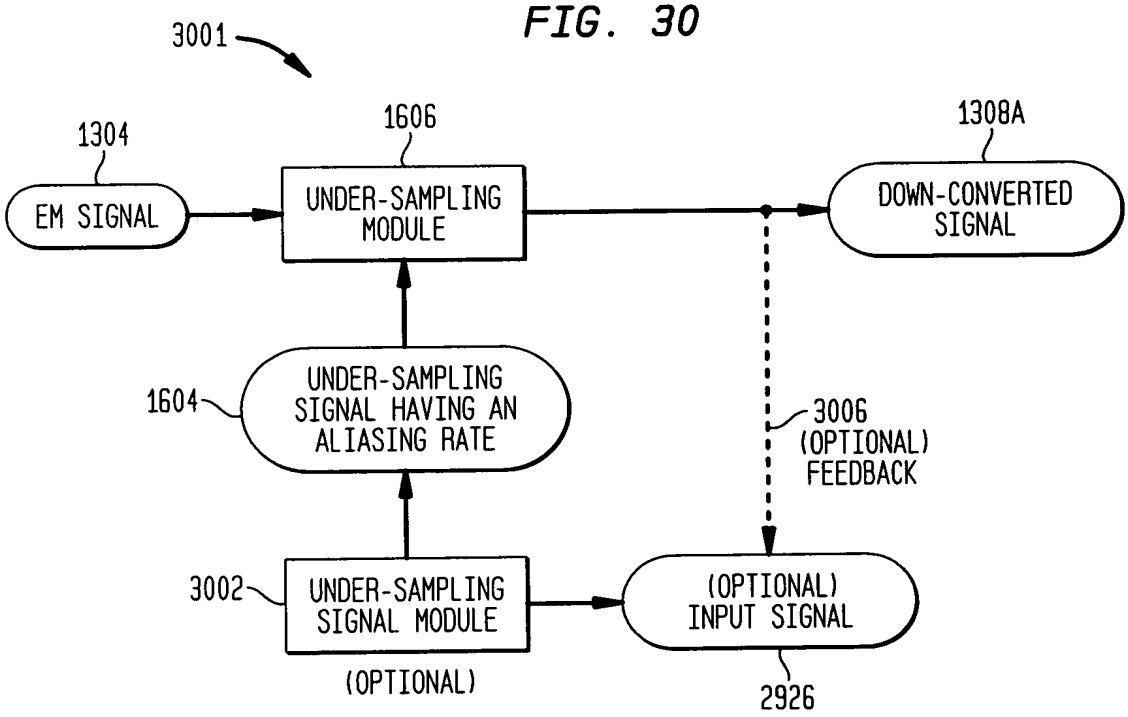


FIG. 31A

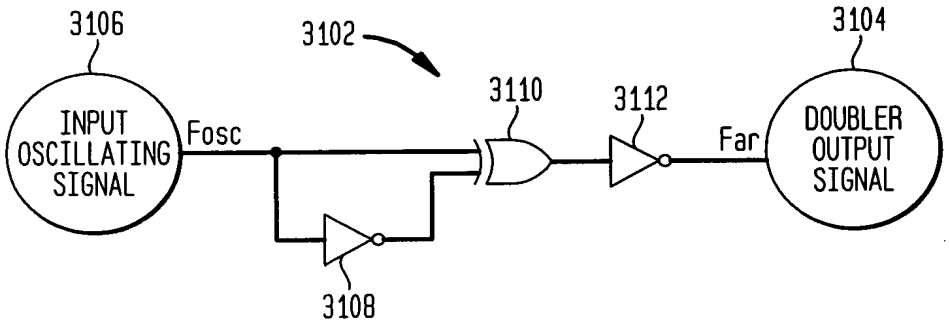

3106
3102
3104
3110
3112
INPUT OSCILLATING SIGNAL
Fosc
Far
DOUBLER OUTPUT SIGNAL
3108

FIG. 31B

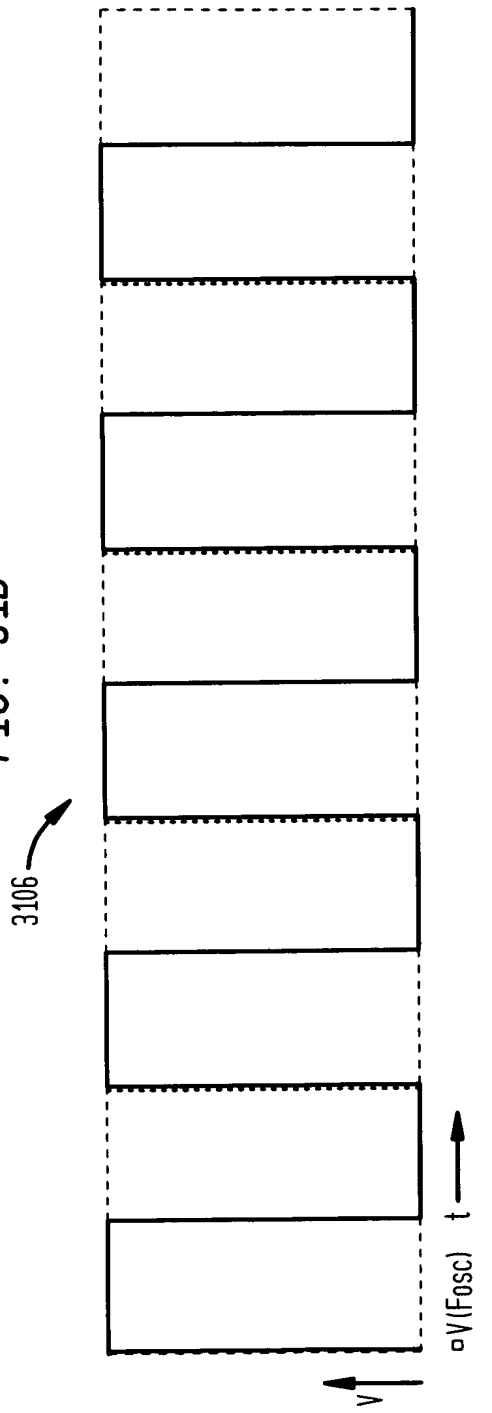



FIG. 31C

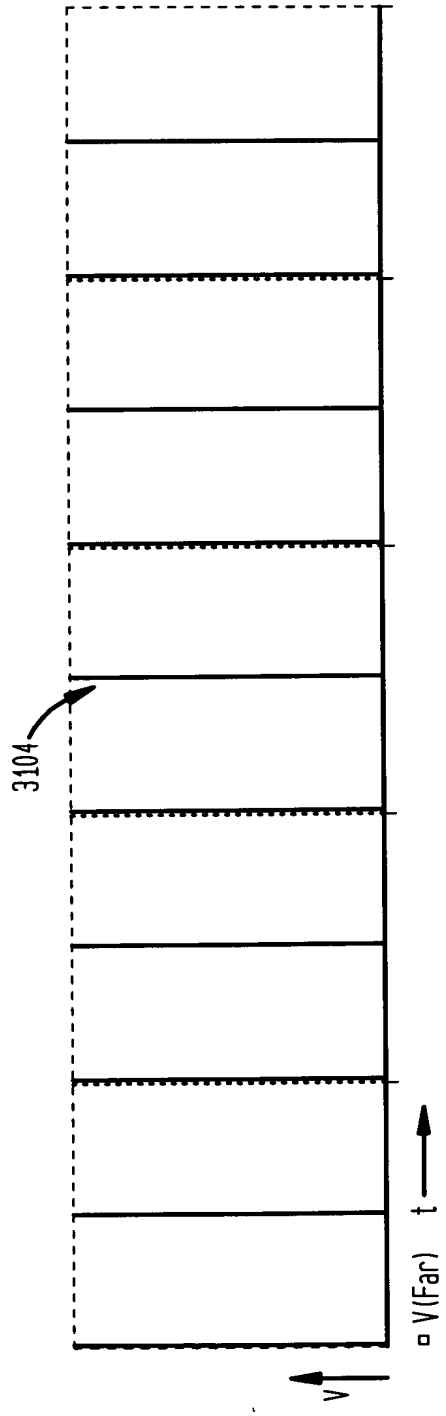
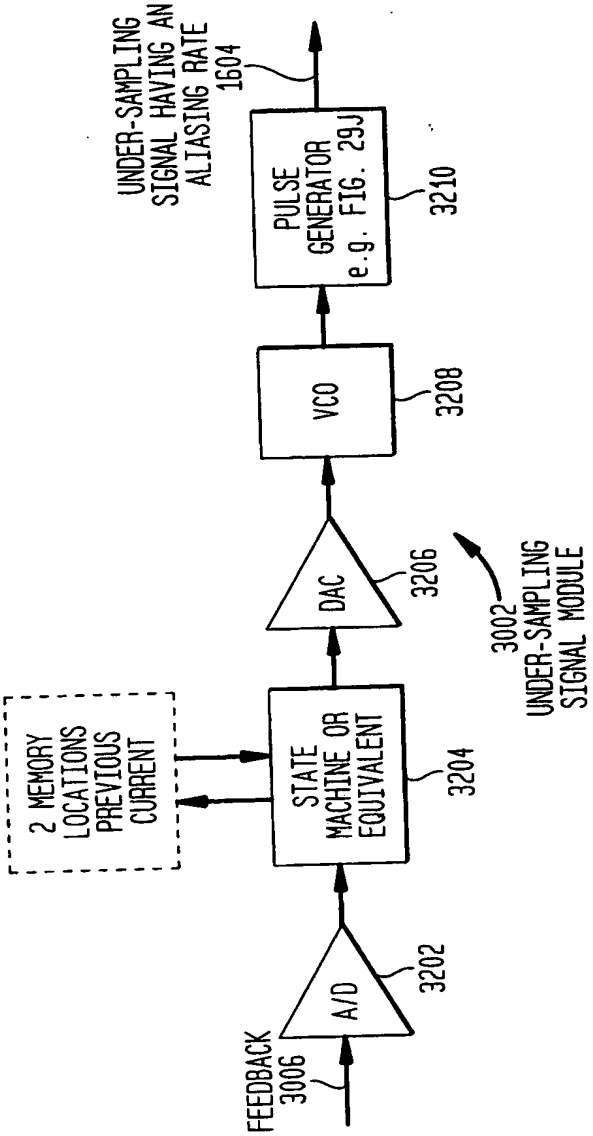
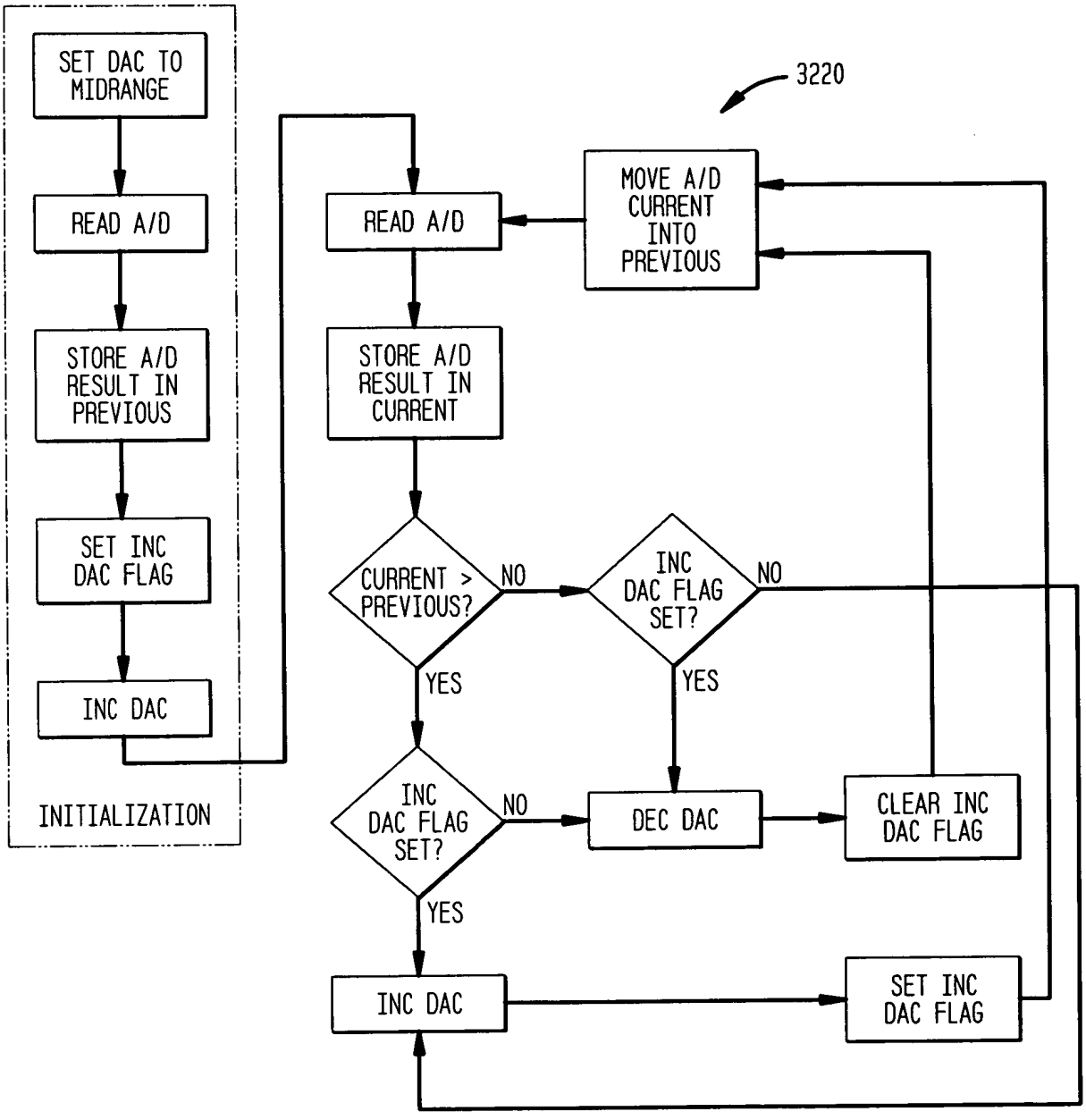


FIG. 32A


UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
1604
PULSE GENERATOR e.g. FIG. 29J
3210
VCO
3208
DAC
3206
3002
UNDER-SAMPLING SIGNAL MODULE
2 MEMORY LOCATIONS PREVIOUS CURRENT
STATE MACHINE OR EQUIVALENT
3204
A/D
3202
FEEDBACK
3006

Replacement Sheet
Sheet 37 of 284
Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 32B




STATE MACHINE FLOWCHART

Replacement Sheet
Sheet 38 of 284
Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
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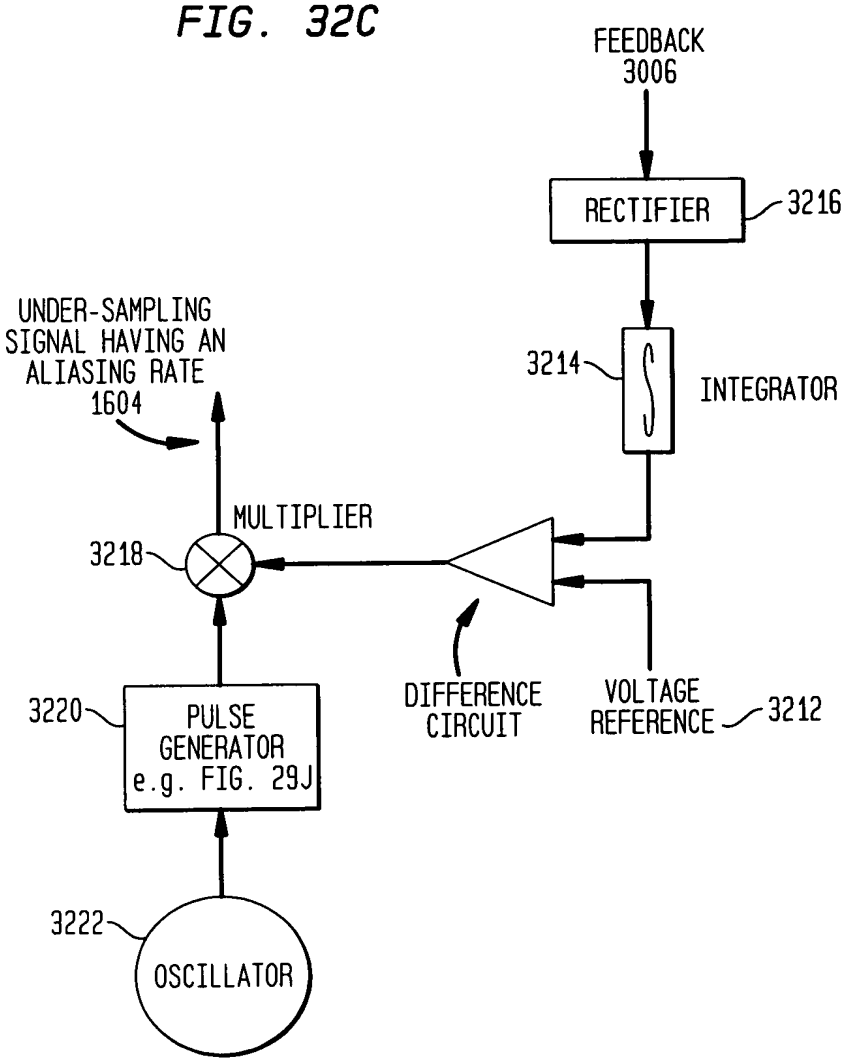
FIG. 32C




ENERGY TRANSFER SIGNAL MODULE 3002

FIG. 33A

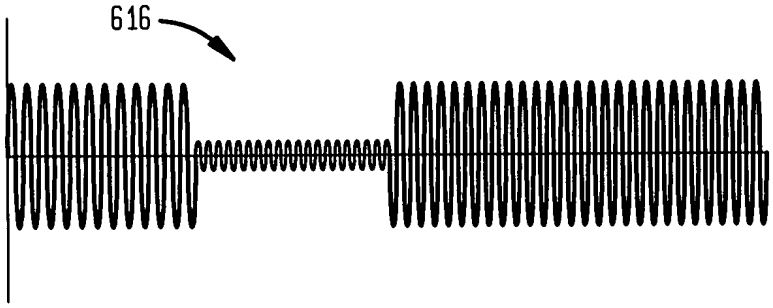



FIG. 33B

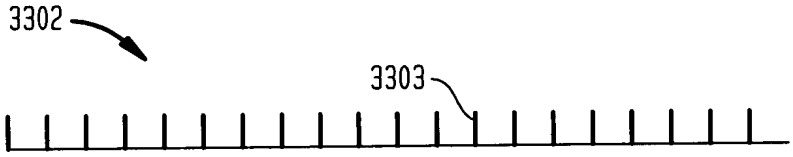



FIG. 33C

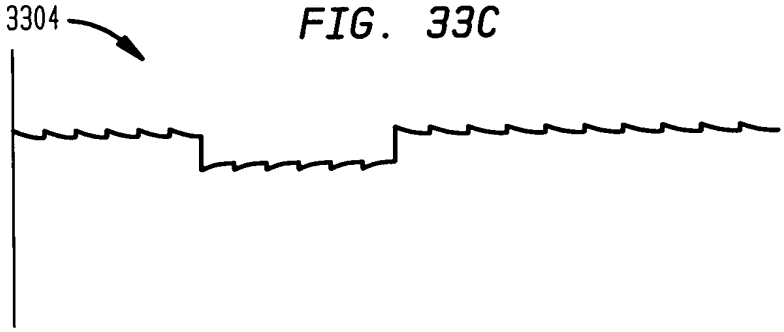



FIG. 33D

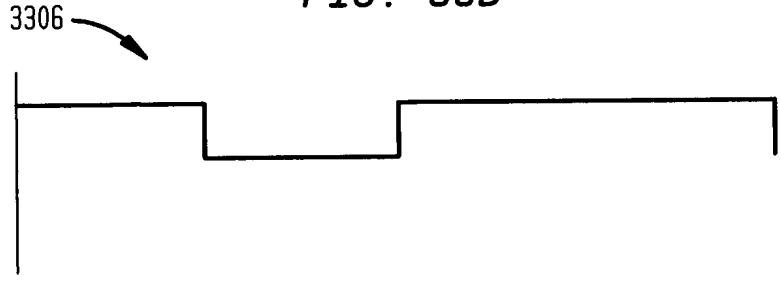


FIG. 34A

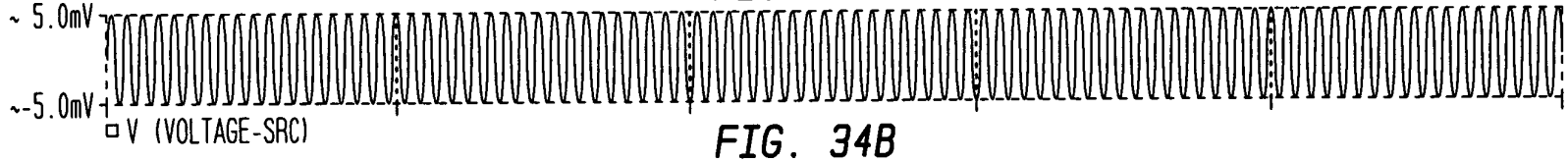



FIG. 34B

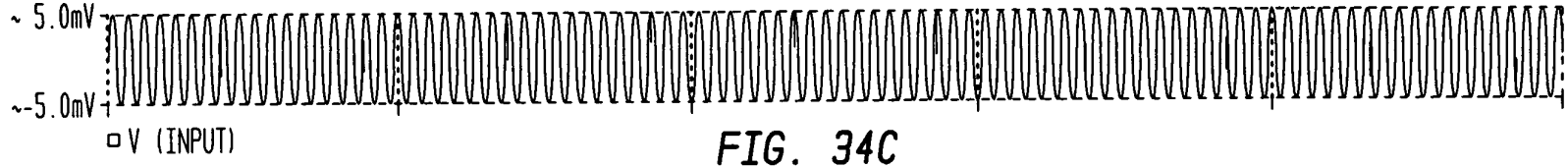



FIG. 34C

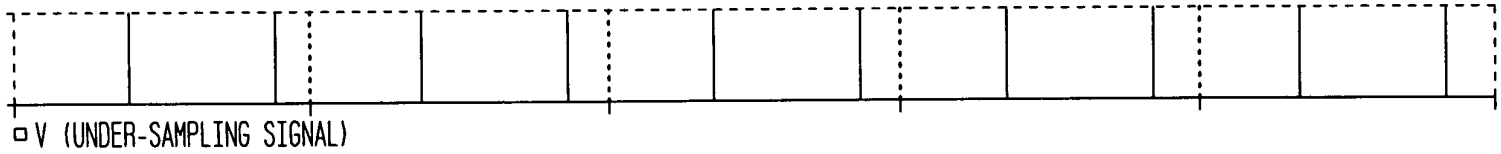



FIG. 34D

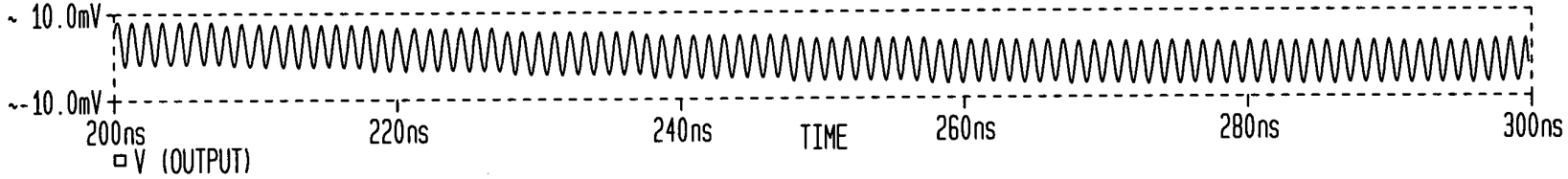



FIG. 34E

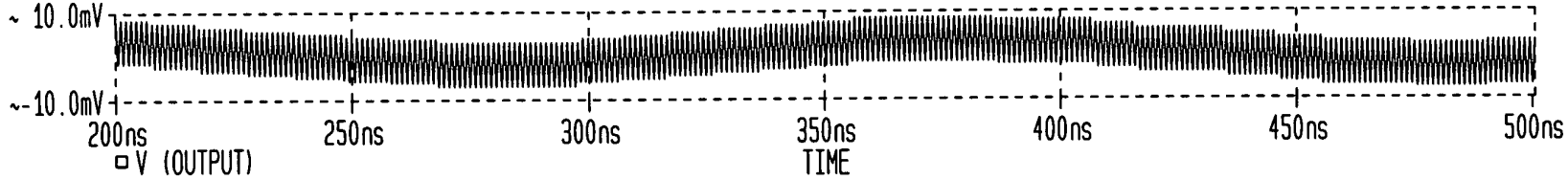



FIG. 34F

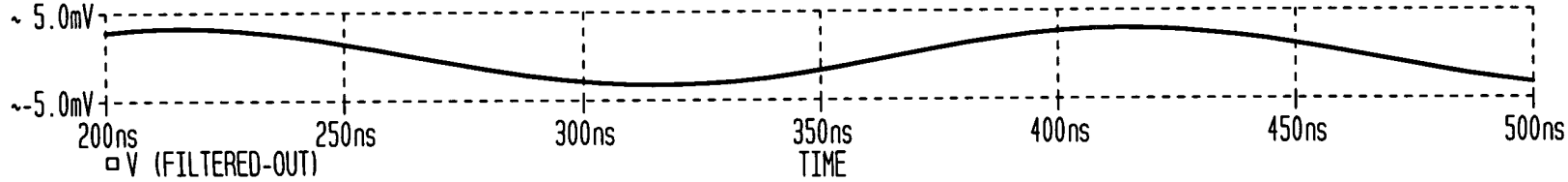



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FIG. 35A

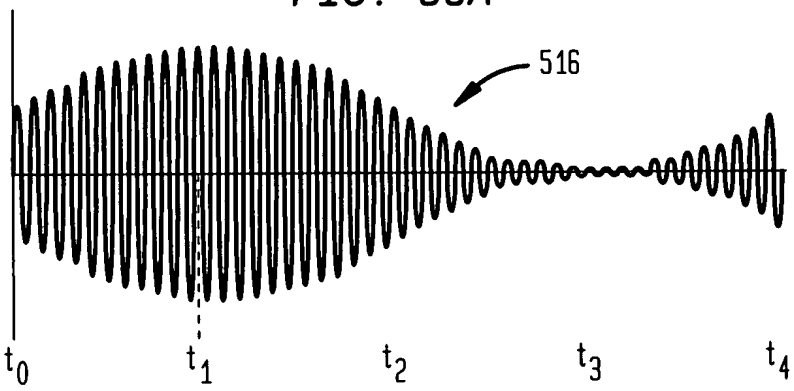


FIG. 35B

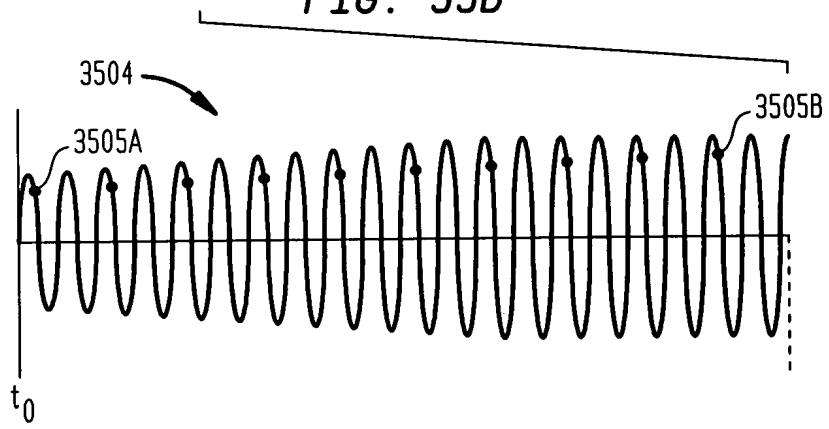


FIG. 35C

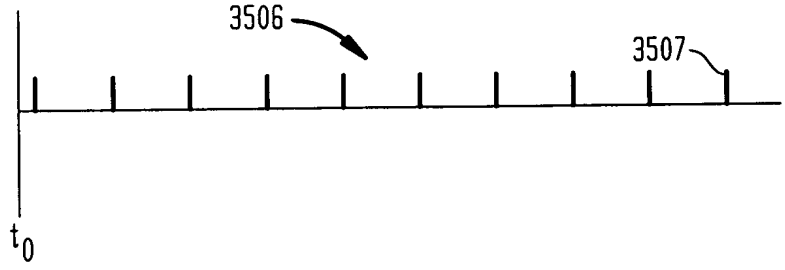


FIG. 35D

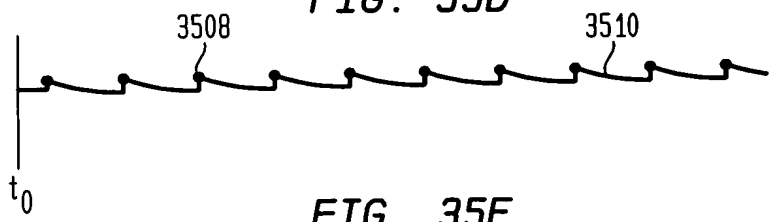


FIG. 35E

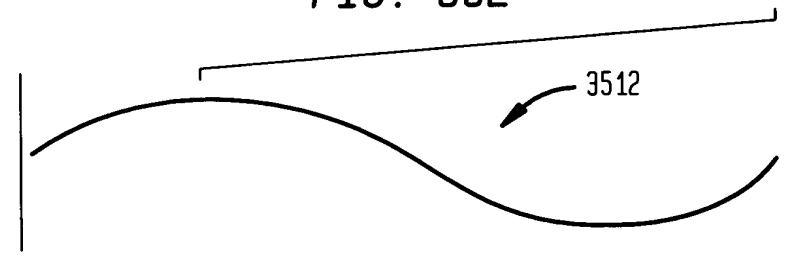

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FIG. 36A

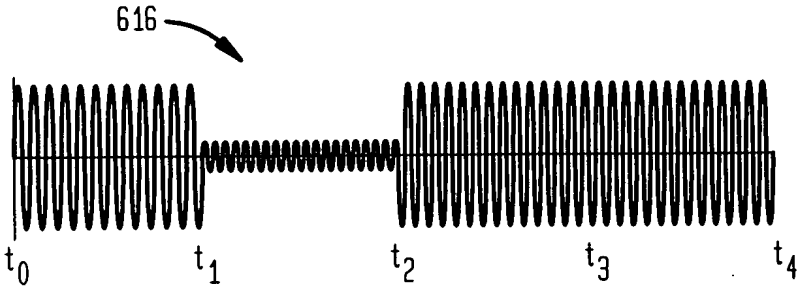


FIG. 36B

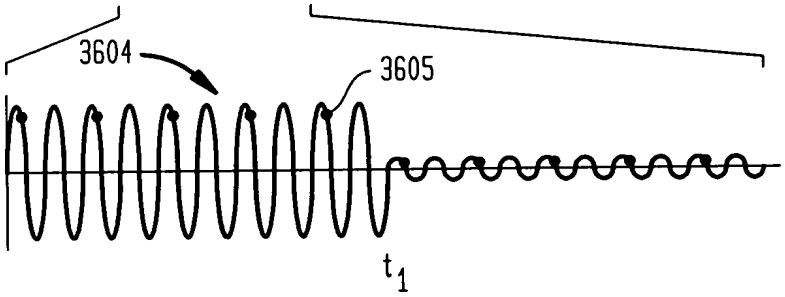


FIG. 36C

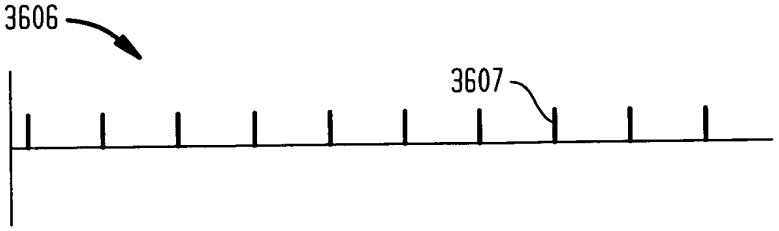


FIG. 36D

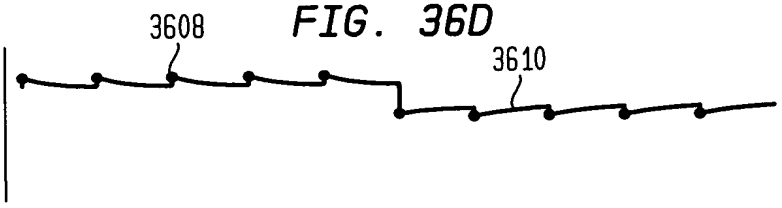


FIG. 36E

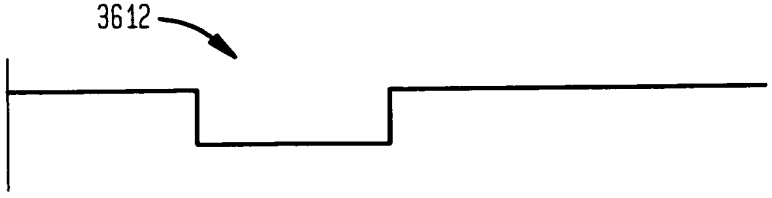

FIG. 37A

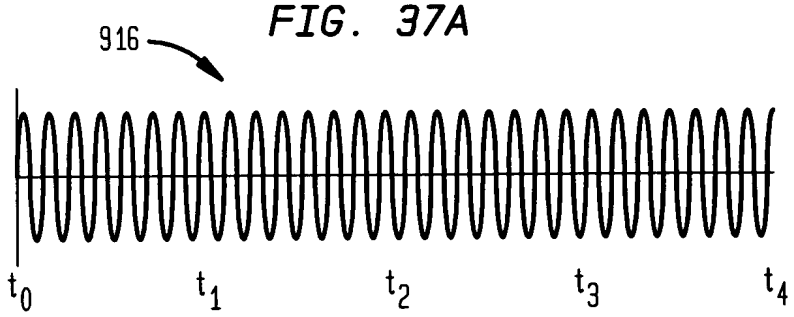


FIG. 37B

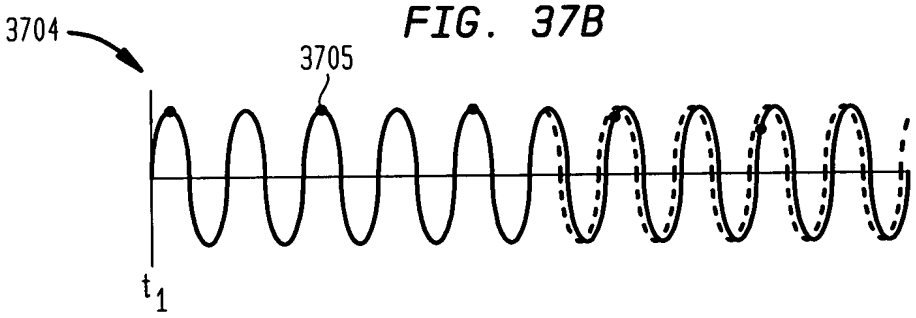


FIG. 37C

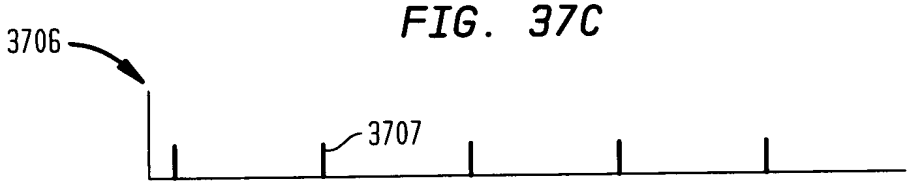


FIG. 37D

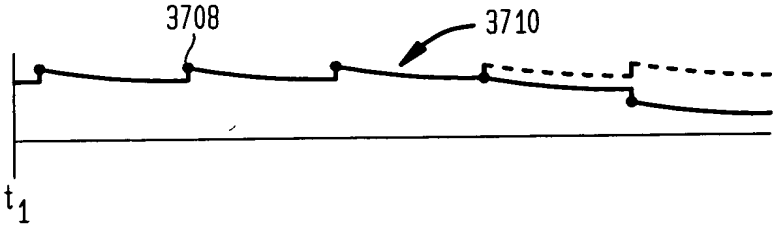


FIG. 37E

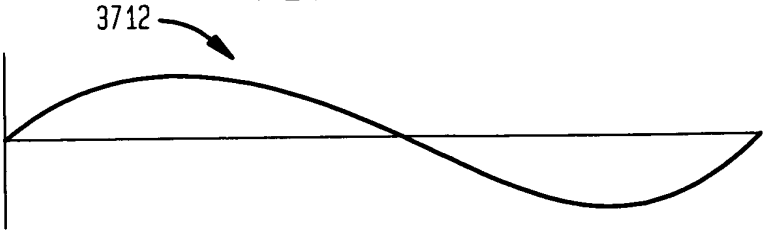

FIG. 38A

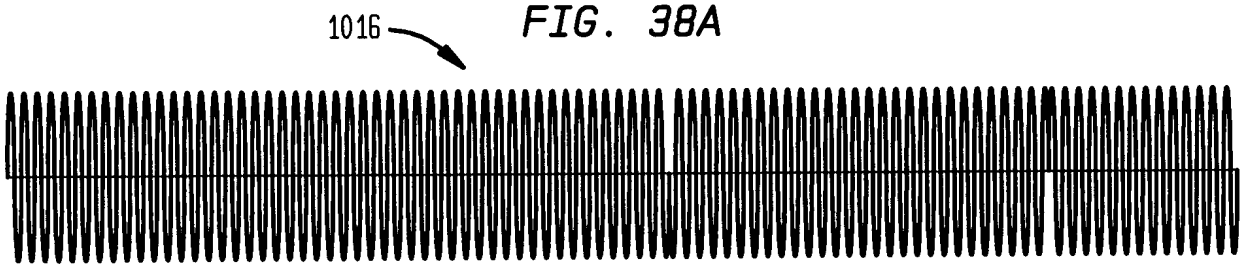


FIG. 38B

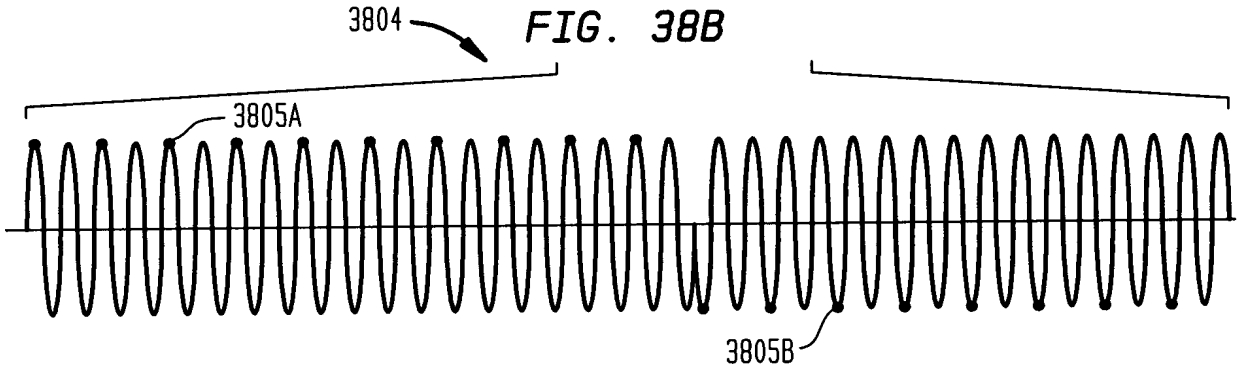


FIG. 38C

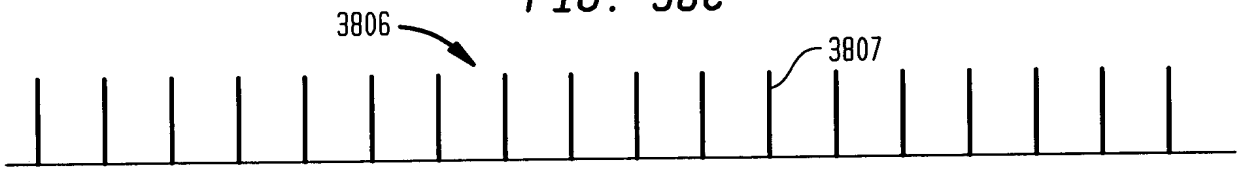


FIG. 38D

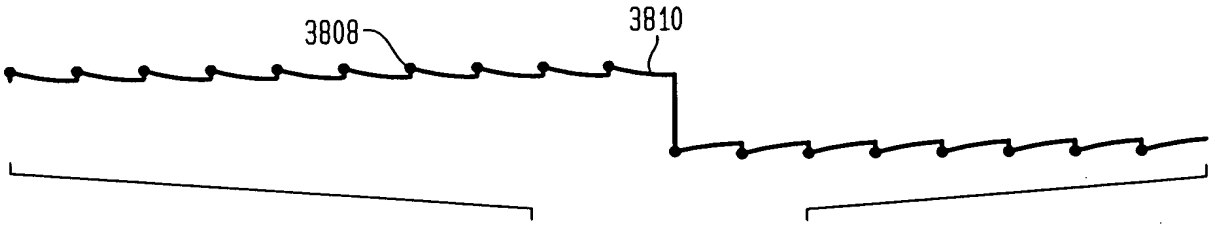


FIG. 38E

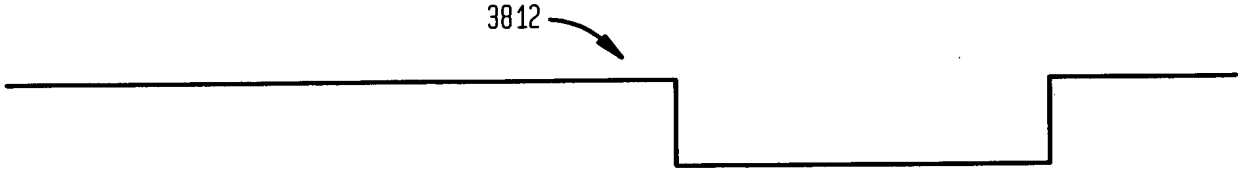

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FIG. 39A

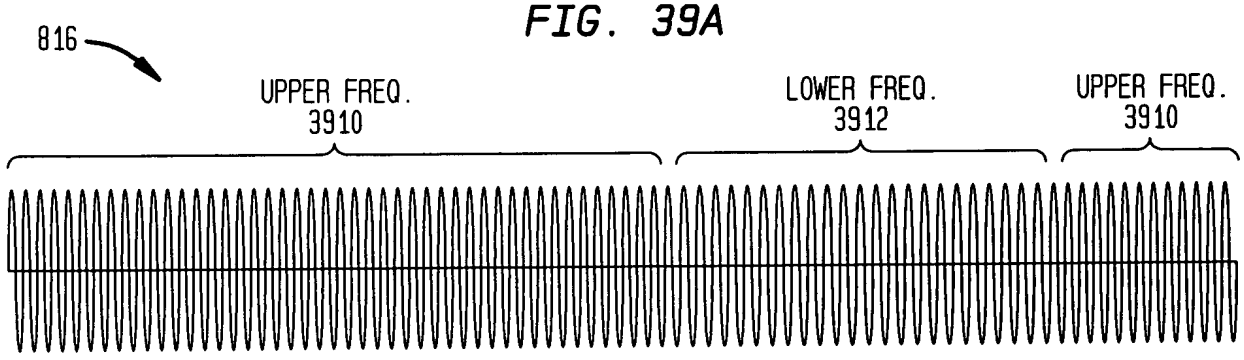


FIG. 39B

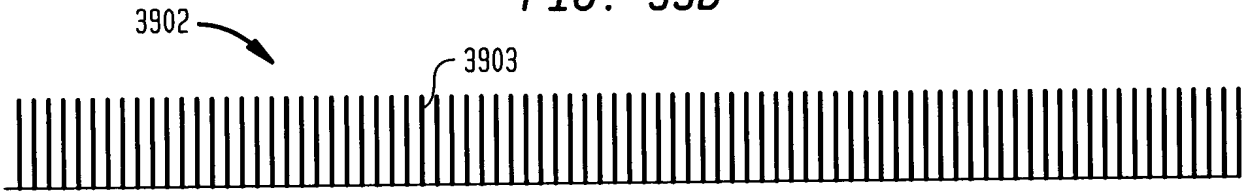


FIG. 39C

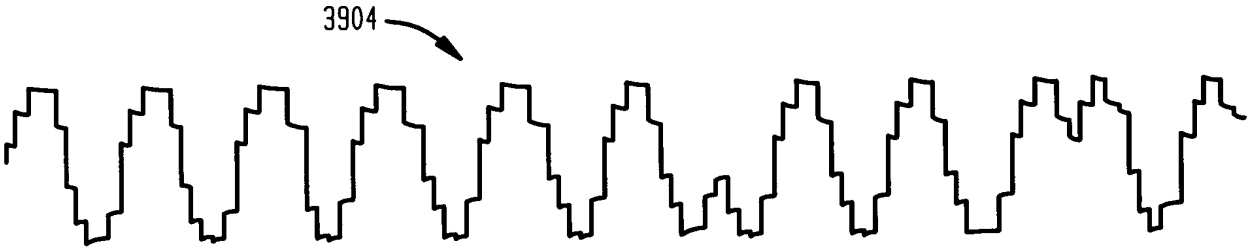


FIG. 39D

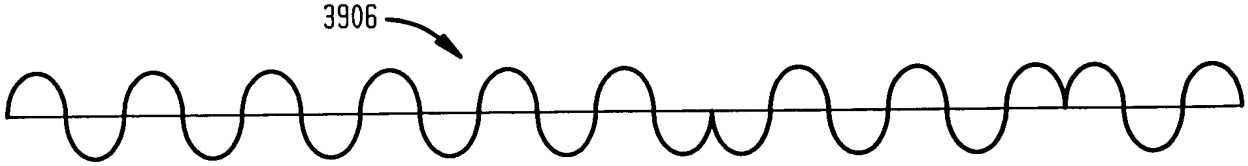

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FIG. 40A

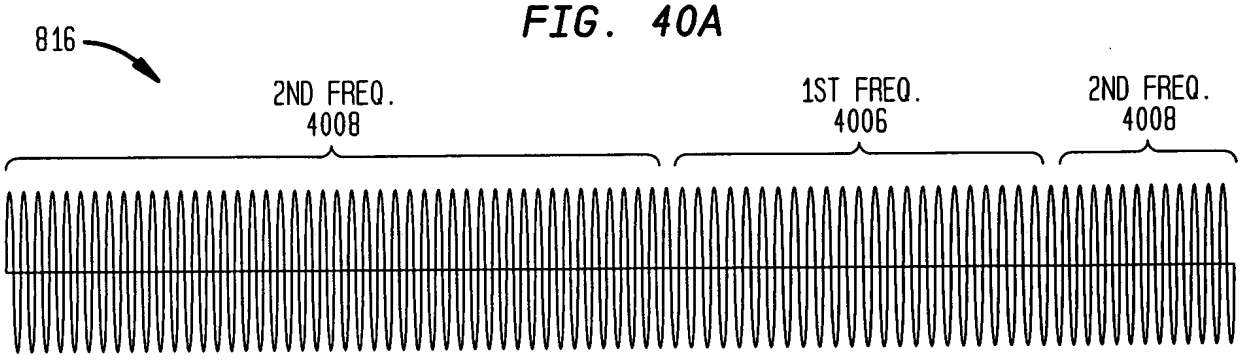



FIG. 40B

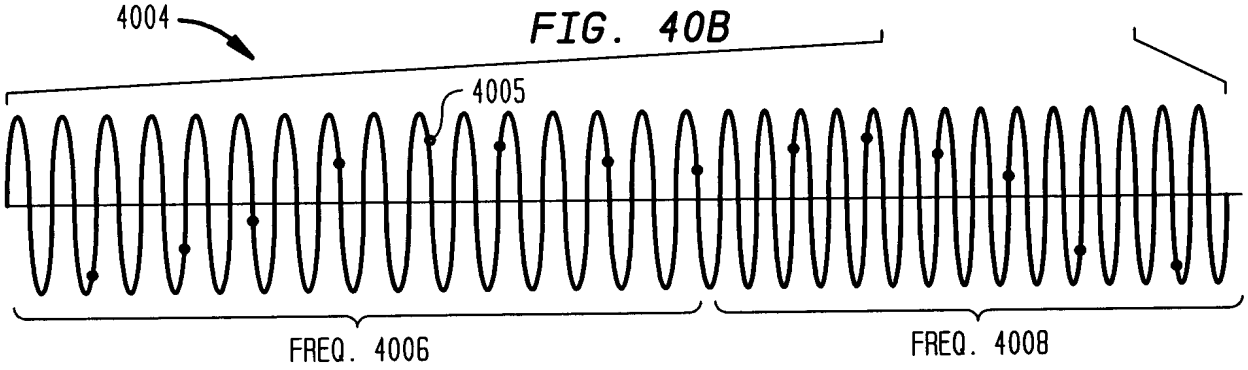



FIG. 40C

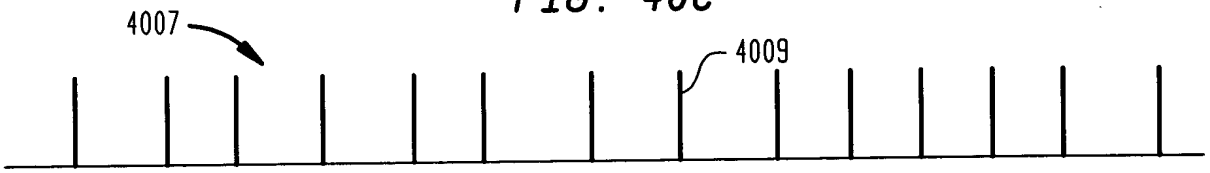



FIG. 40D

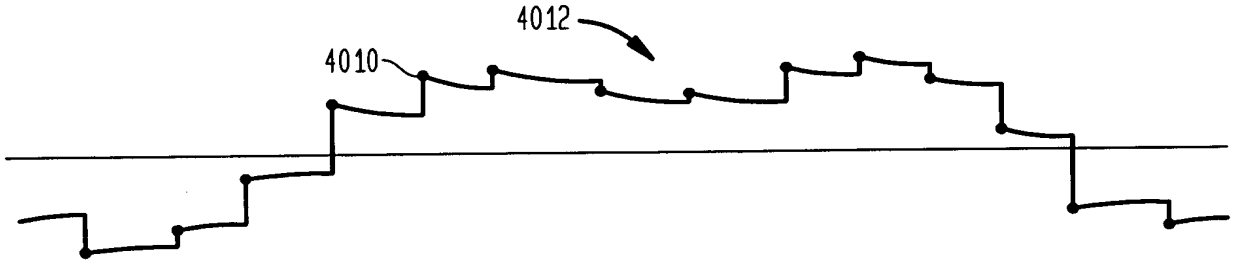
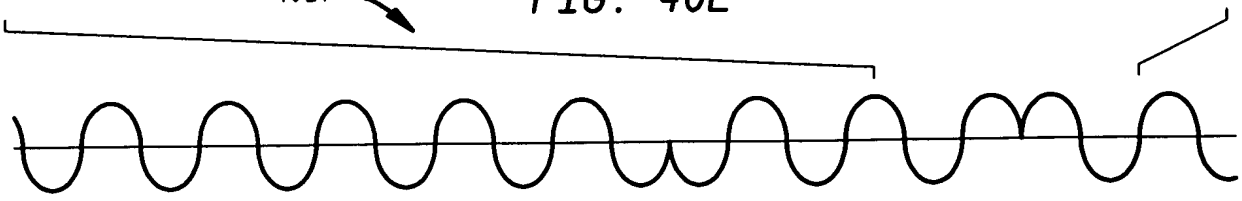



FIG. 40E



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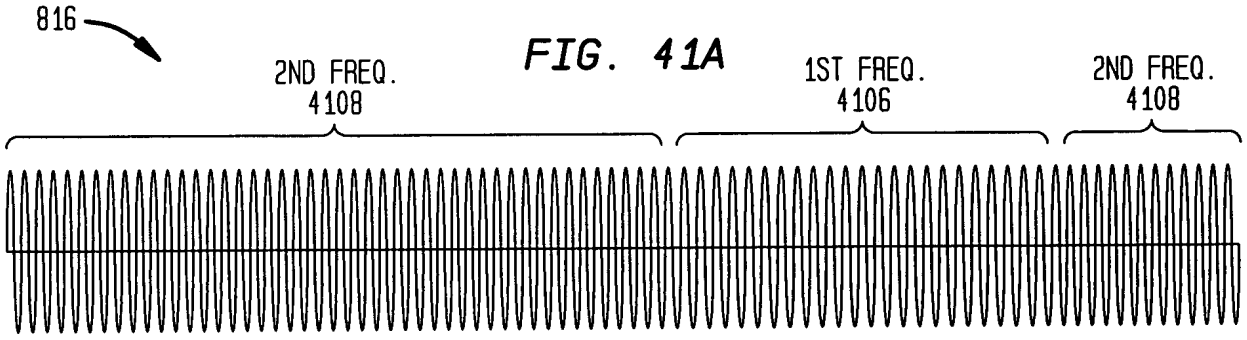


FIG. 41A

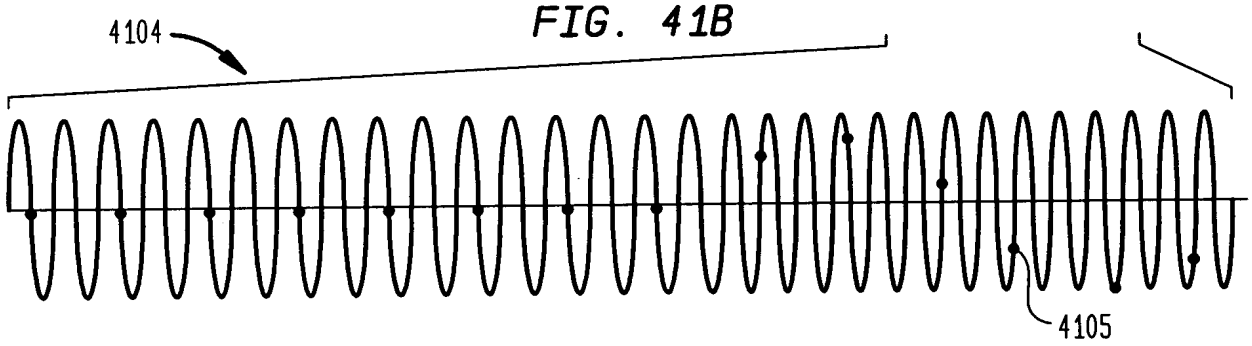


FIG. 41B

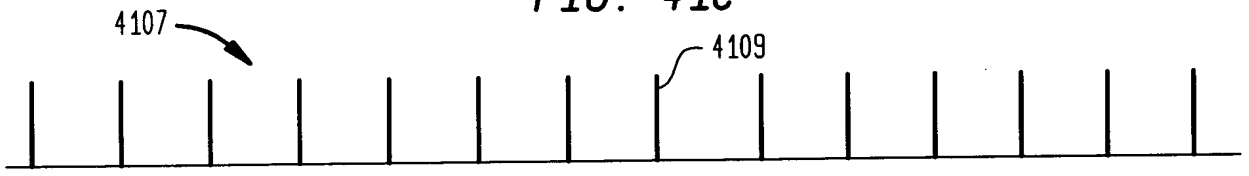


FIG. 41C

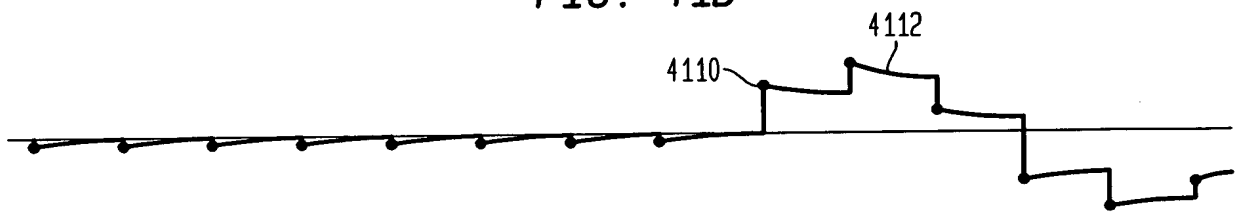


FIG. 41D

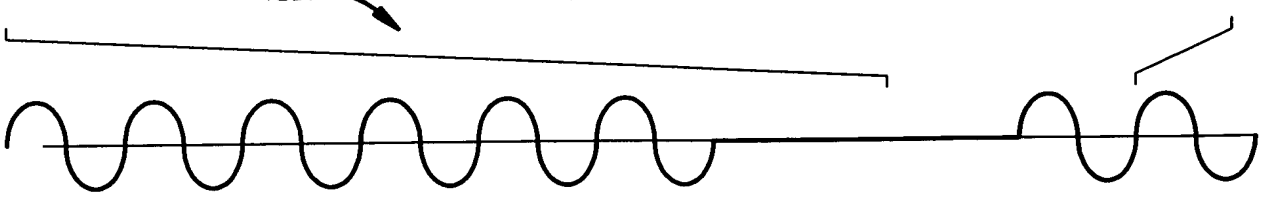


FIG. 41E

FIG. 42

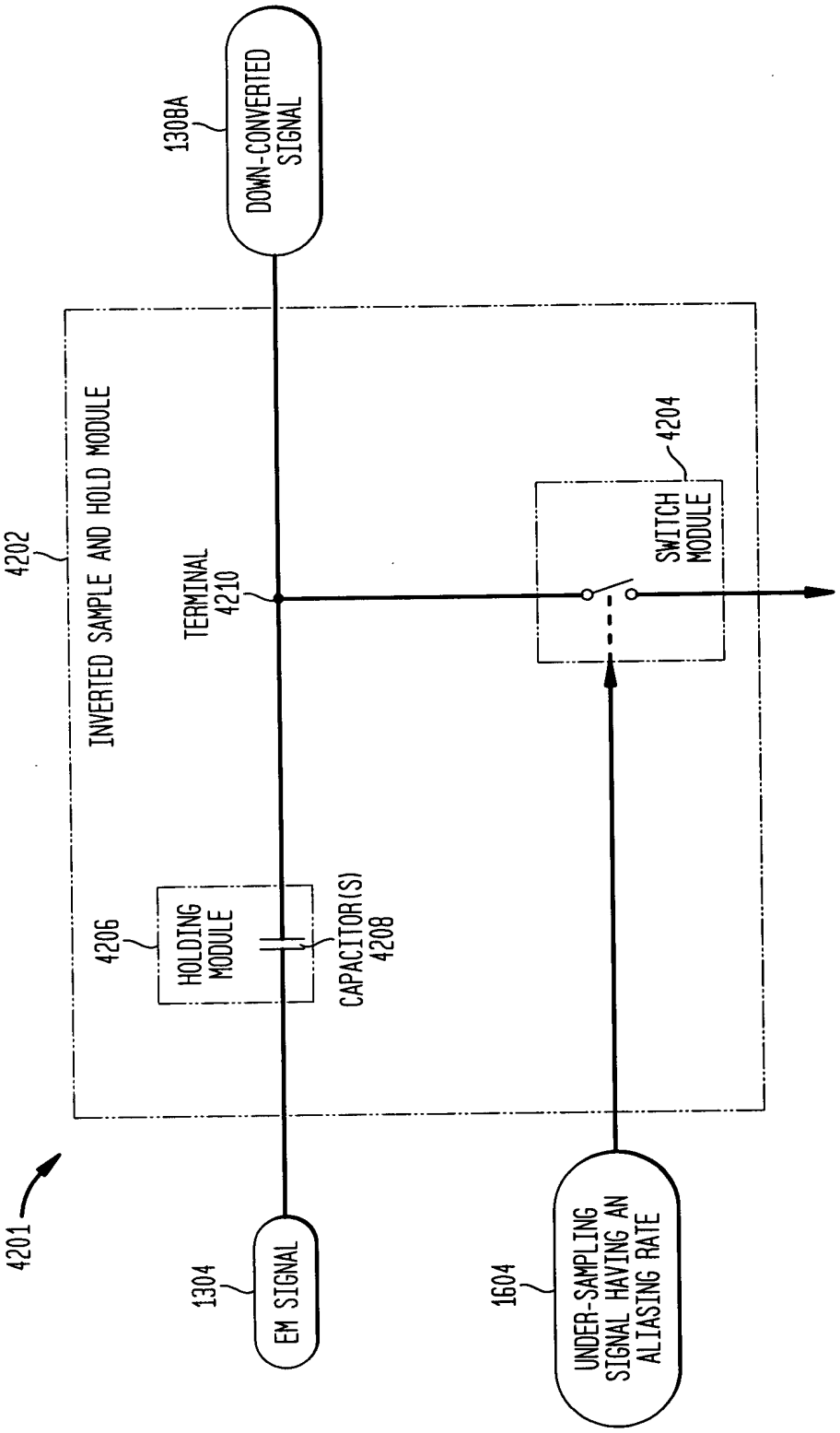
1308A
DOWN-CONVERTED SIGNAL
4202
INVERTED SAMPLE AND HOLD MODULE
TERMINAL 4210
4204
SWITCH MODULE
4206
HOLDING MODULE
CAPACITOR(S) 4208
4201
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE

**FIG. 43**

$$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin\left(\frac{1}{2} \cdot T\right) \cdot \cos\left(t - \frac{1}{2} \cdot T\right)$$

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FIG. 44A

DIFFERENTIAL CONFIGURATION

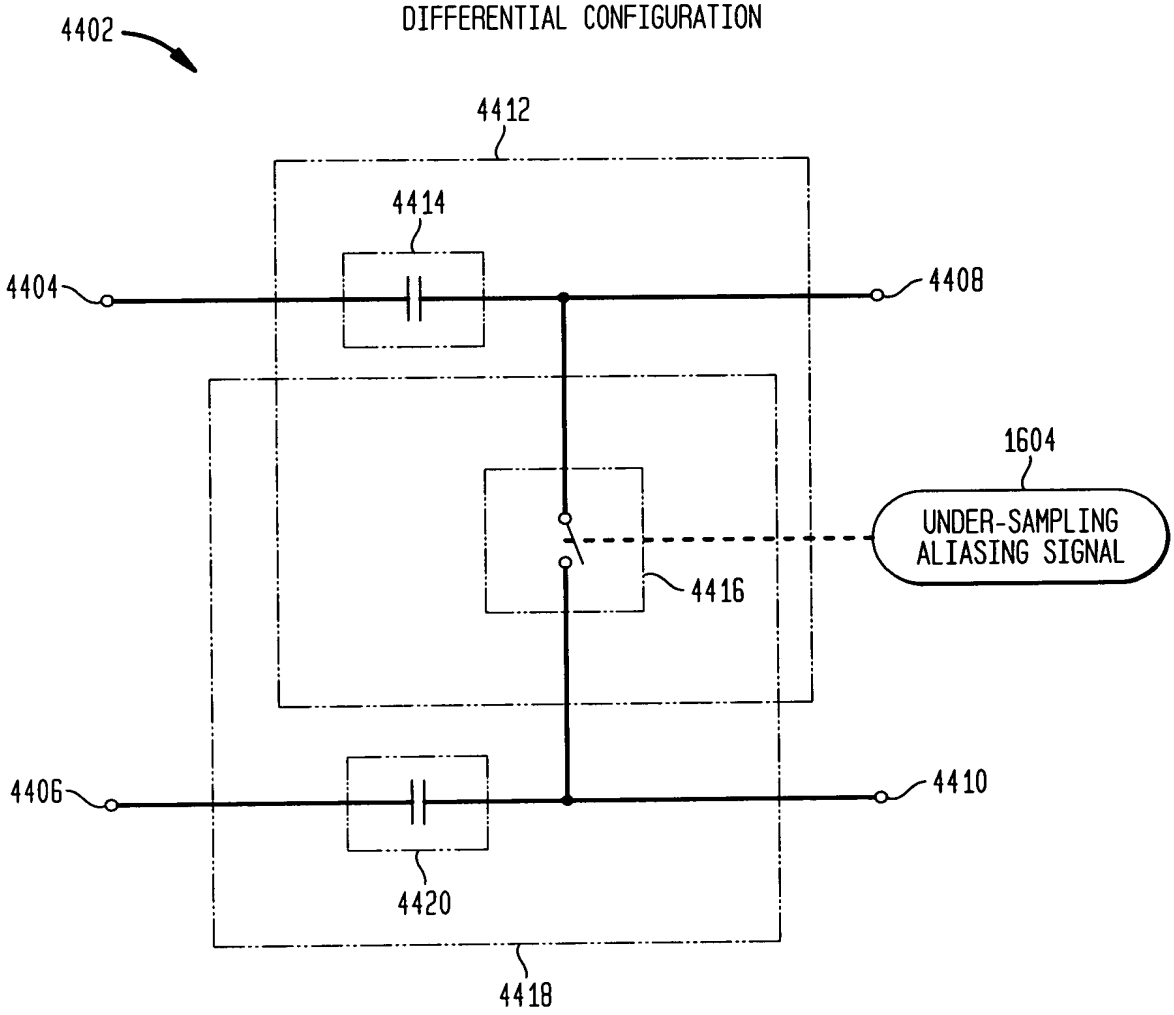

*FIG. 44B*

DIFFERENTIAL INPUT TO DIFFERENTIAL OUTPUT

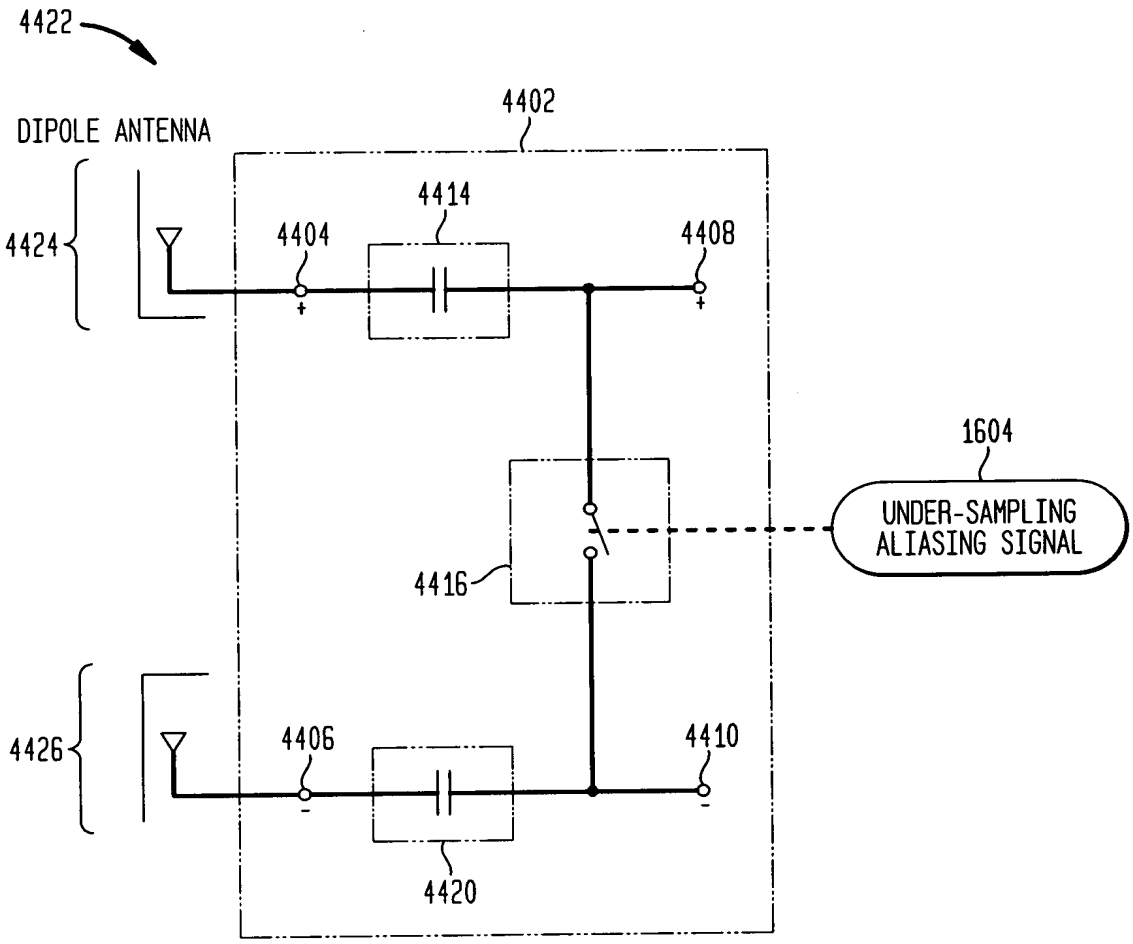

*FIG. 44C*

SINGLE INPUT TO DIFFERENTIAL OUTPUT

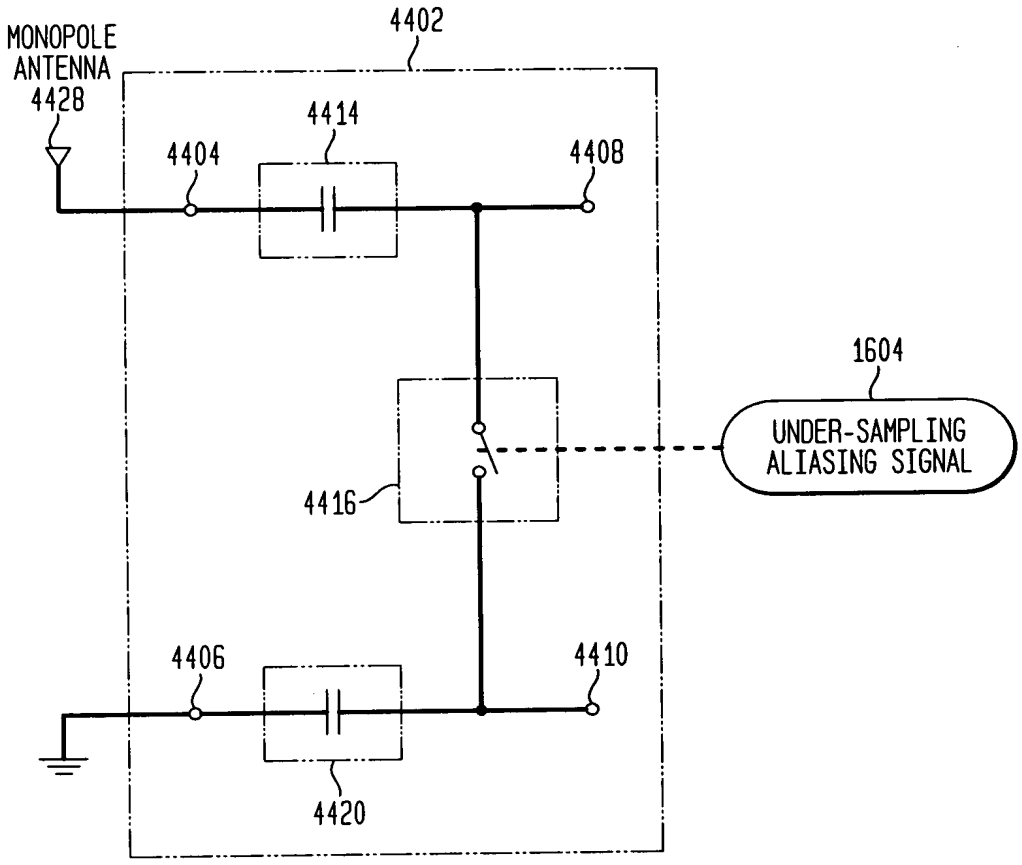

*FIG. 44D*

DIFFERENTIAL INPUT TO SINGLE OUTPUT

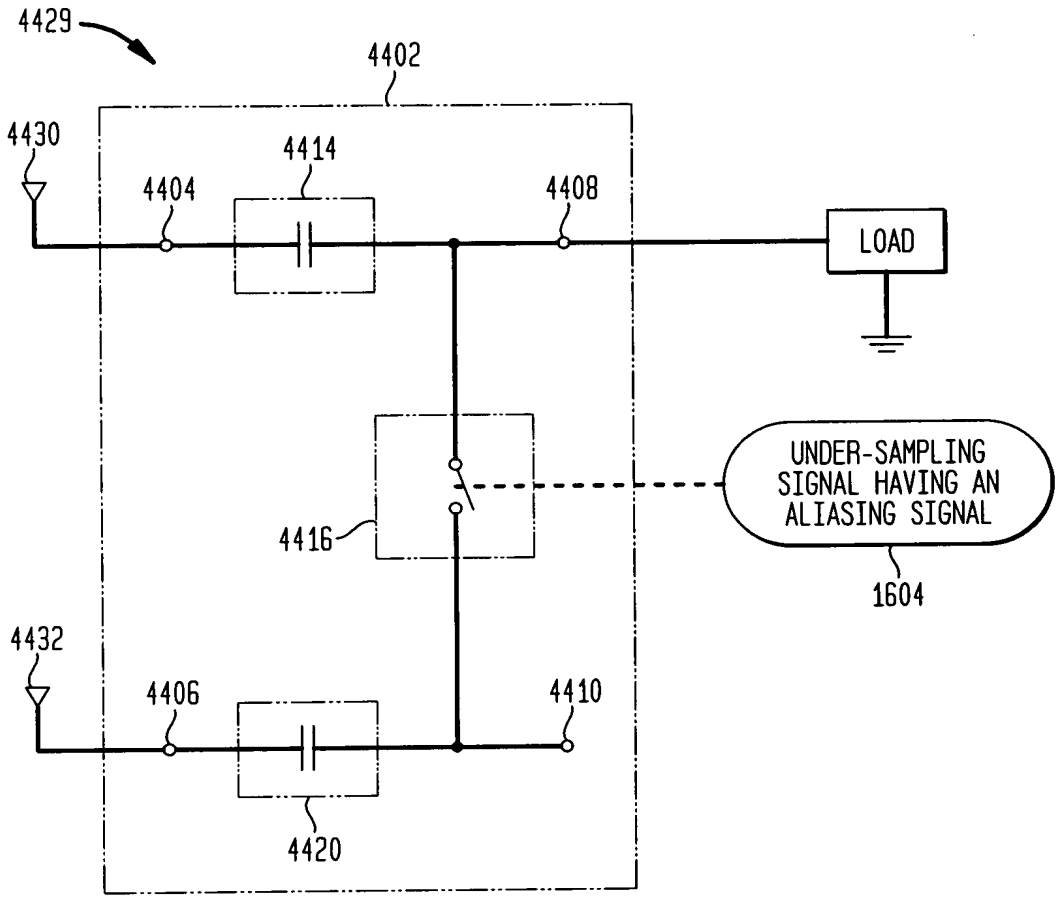

*FIG. 44E*

EXAMPLE INPUT/OUTPUT CIRCUITRY

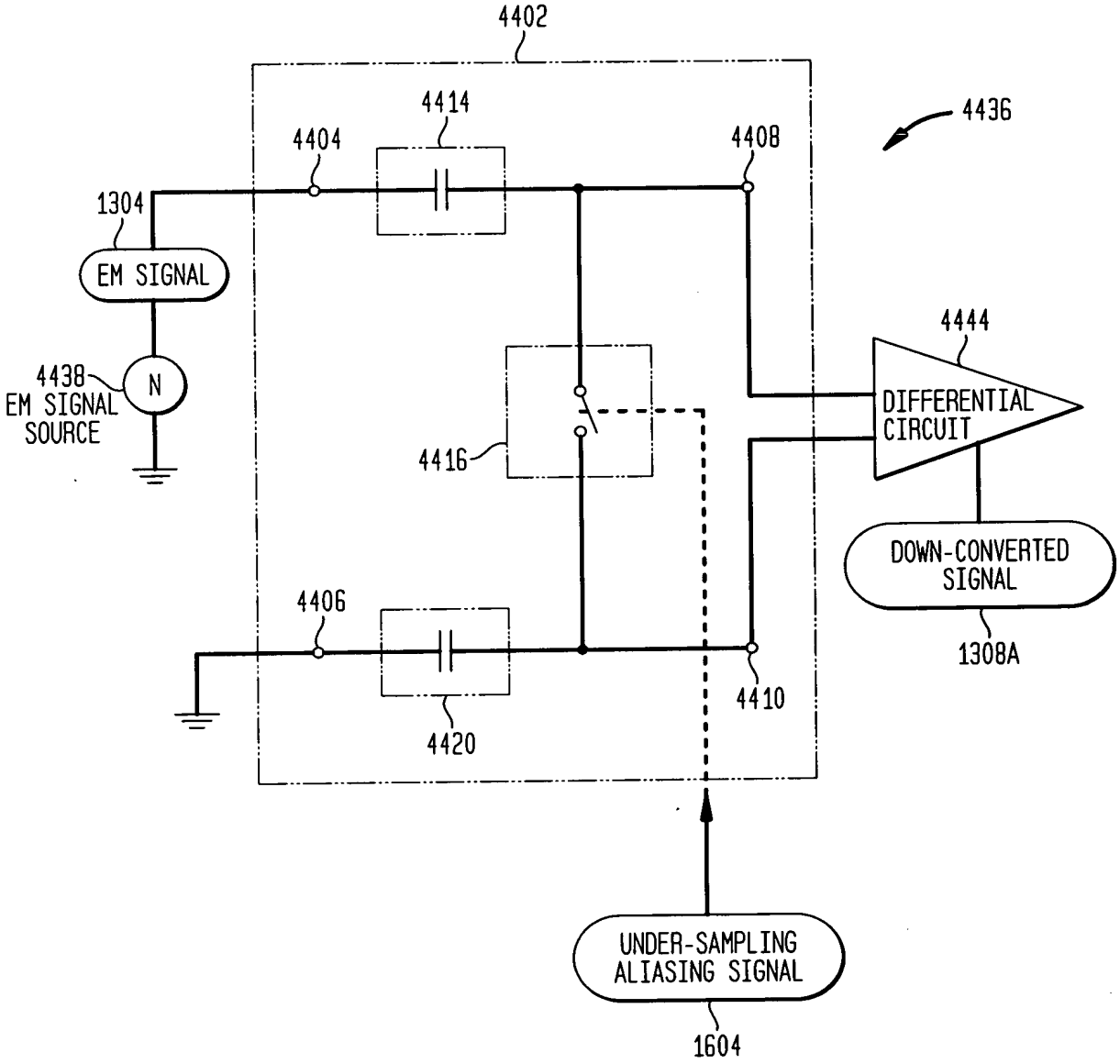

FIG. 45A

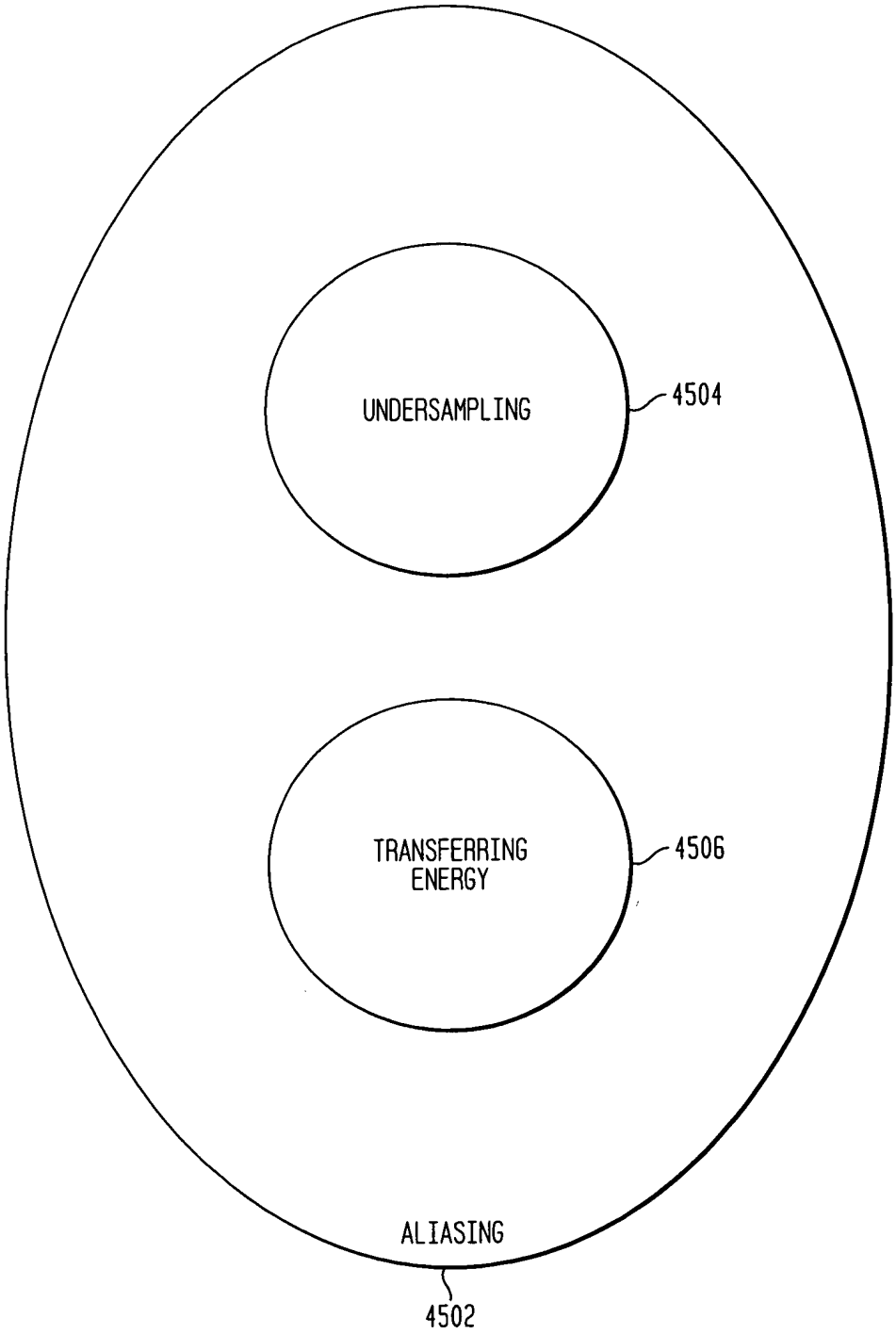
UNDERSAMPLING
4504
TRANSFERRING ENERGY
4506
ALIASING
4502

FIG. 45B

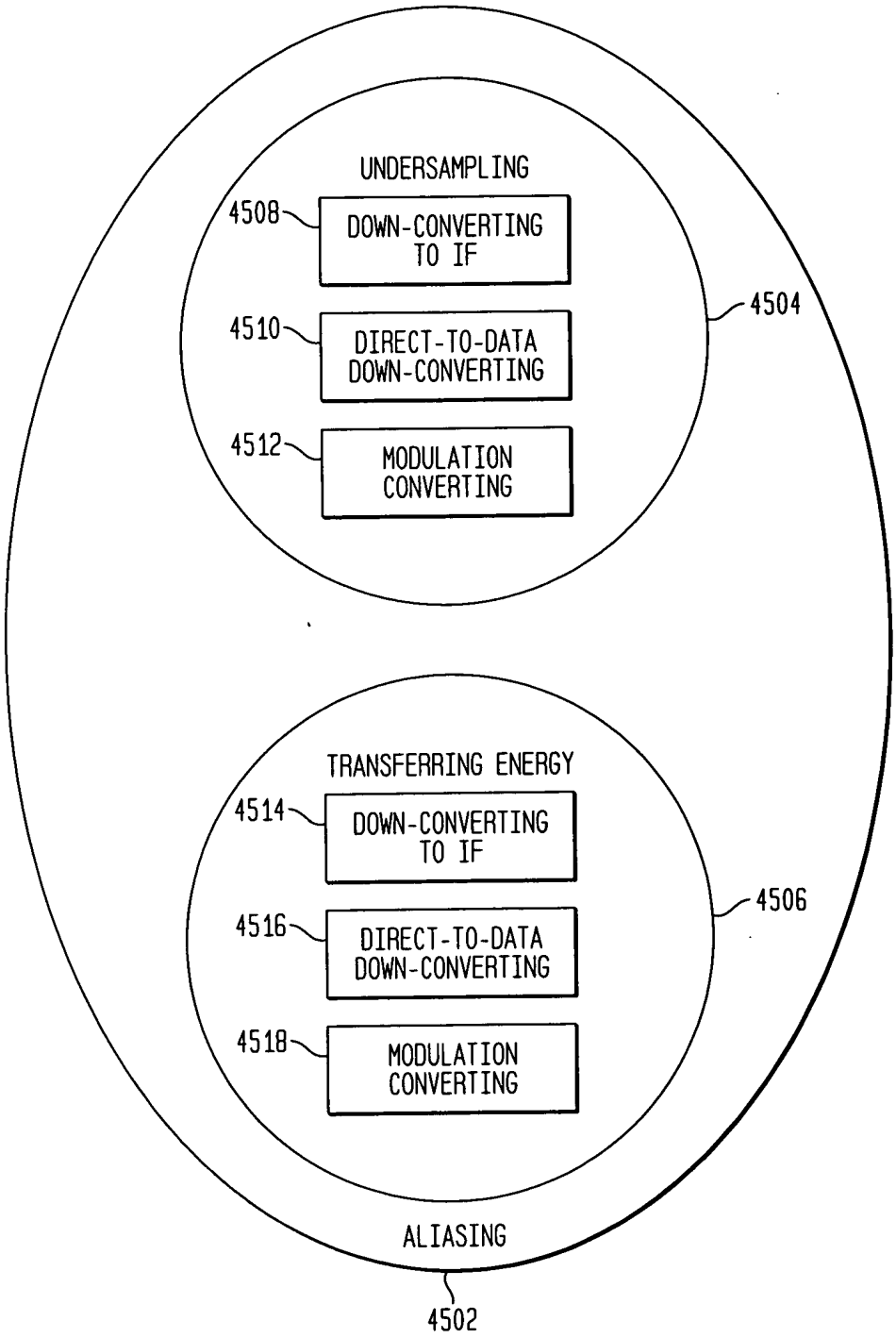
UNDERSAMPLING
4508
DOWN-CONVERTING TO IF
4510
DIRECT-TO-DATA DOWN-CONVERTING
4512
MODULATION CONVERTING
4504
TRANSFERRING ENERGY
4514
DOWN-CONVERTING TO IF
4516
DIRECT-TO-DATA DOWN-CONVERTING
4518
MODULATION CONVERTING
4506
ALIASING
4502

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FIG. 46A

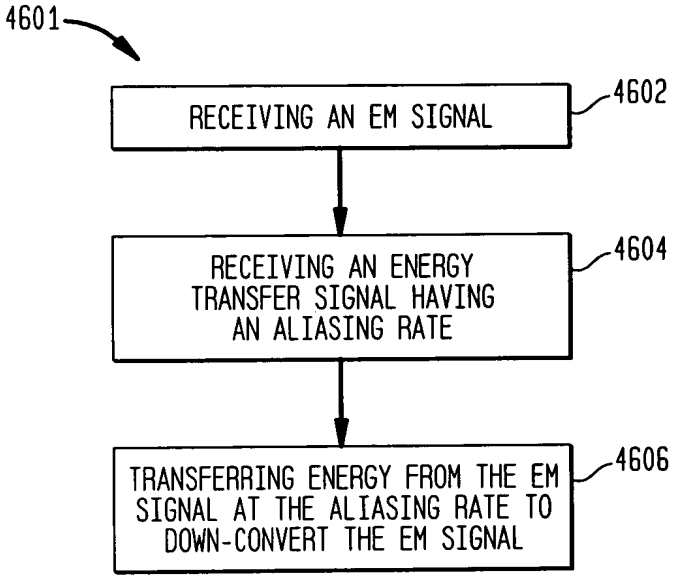


FIG. 46B

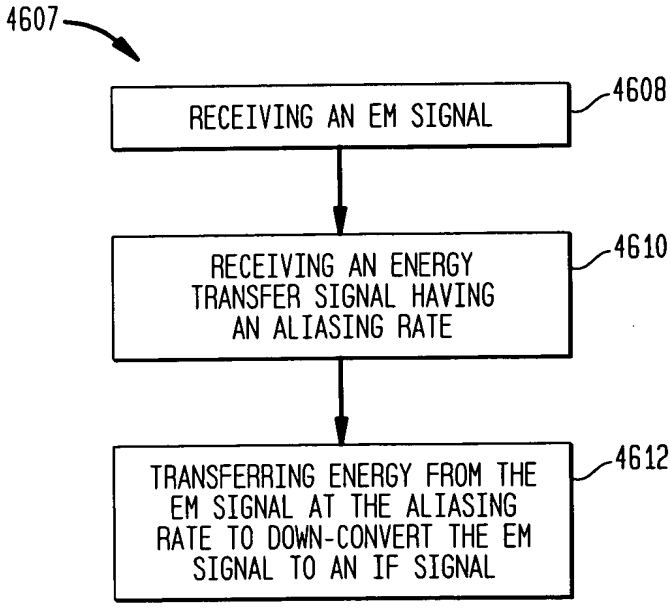

FIG. 46C

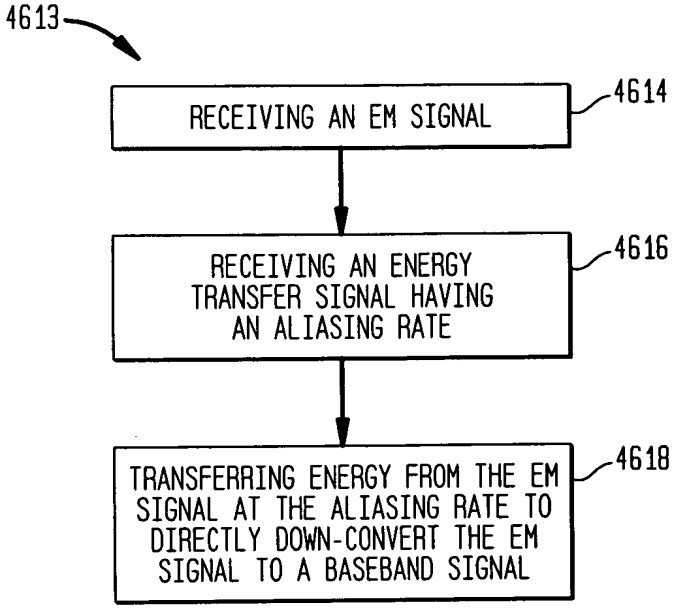


FIG. 46D

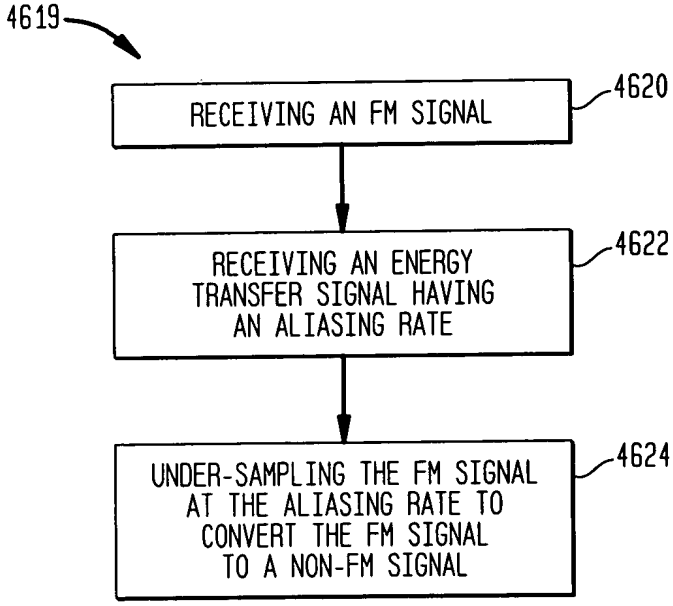

FIG. 47E

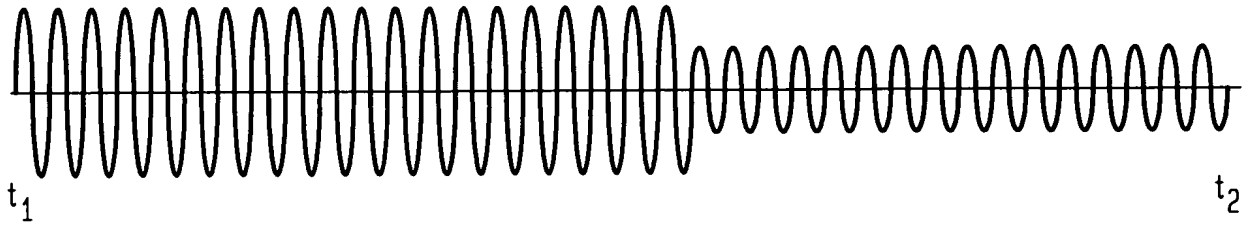


FIG. 47A

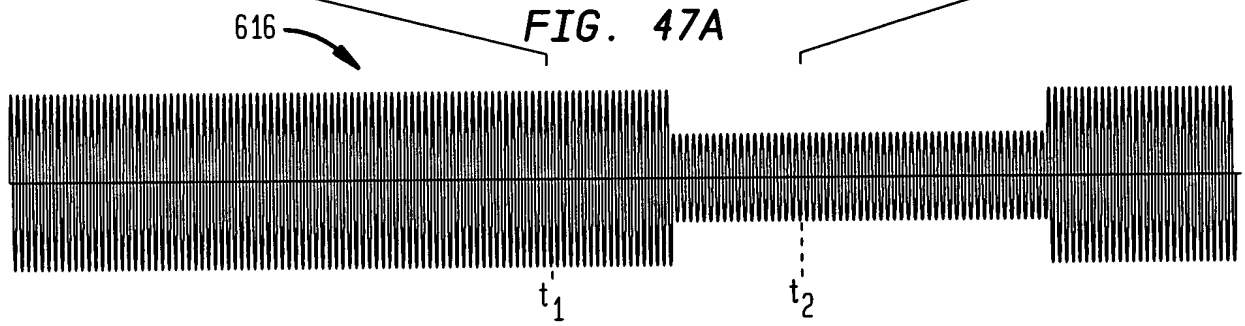


FIG. 47B

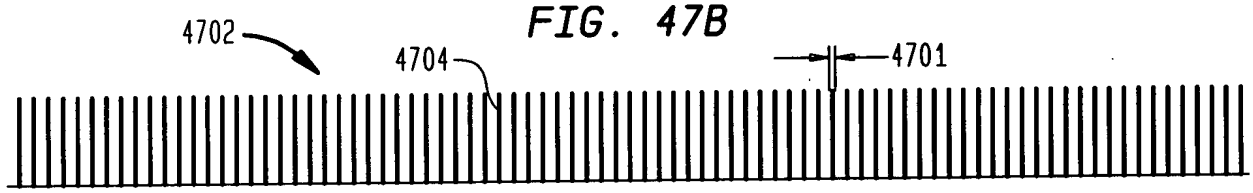


FIG. 47C

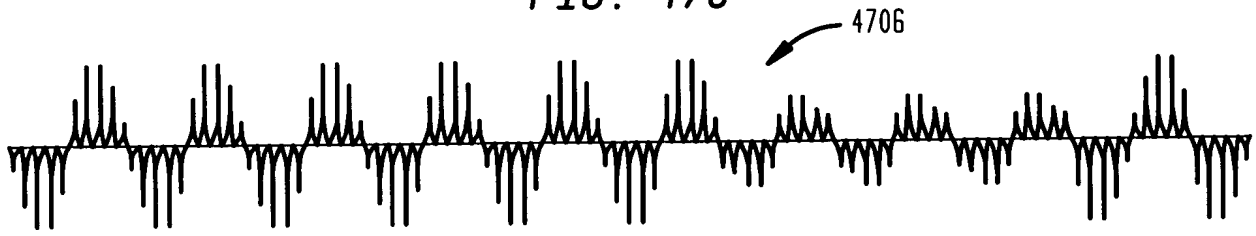


FIG. 47D

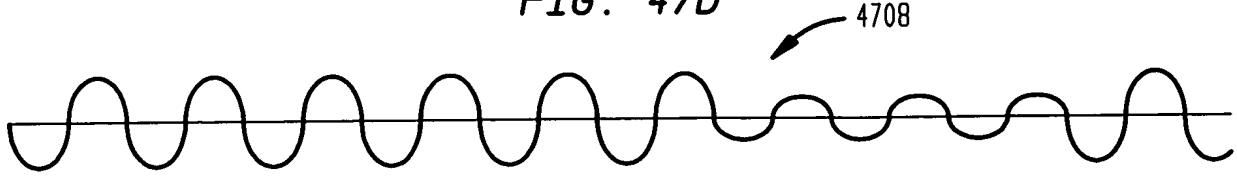

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FIG. 48

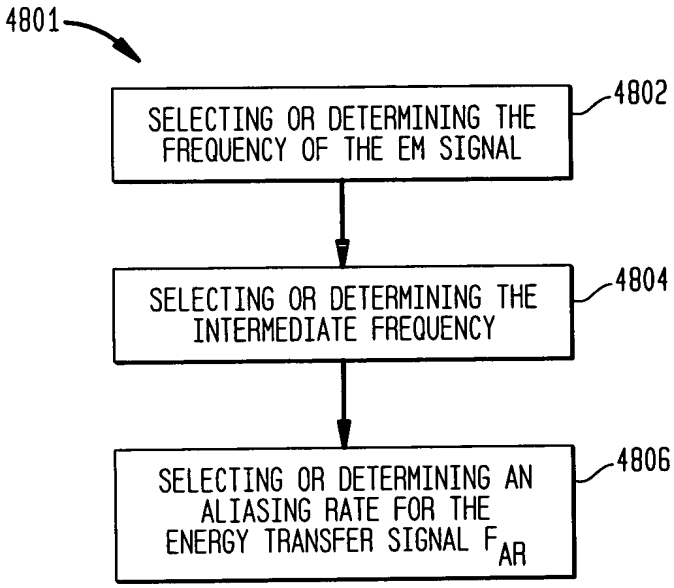

FIG. 49A


FIG. 49B

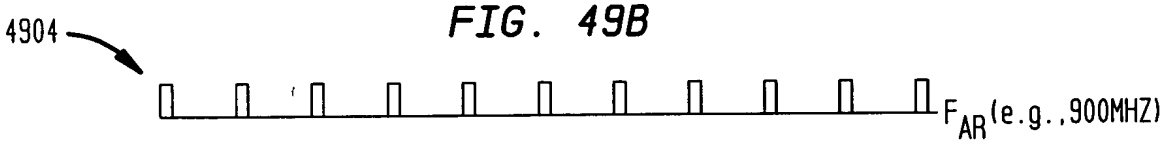


FIG. 49C

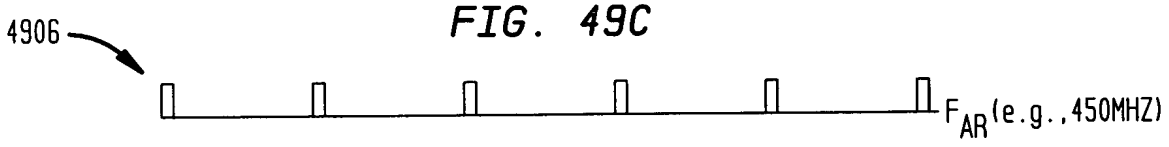


FIG. 49D

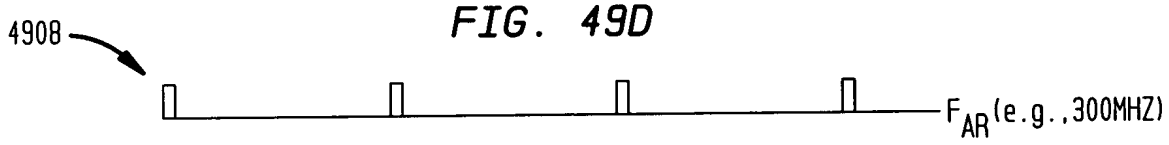


FIG. 49E

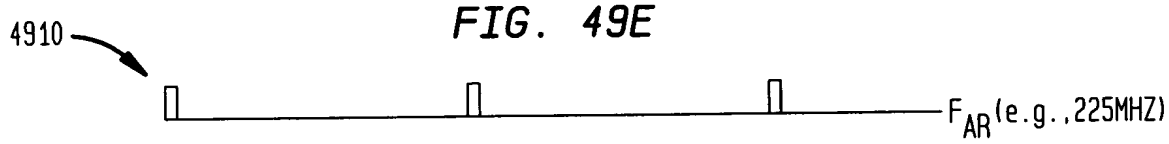


FIG. 49F

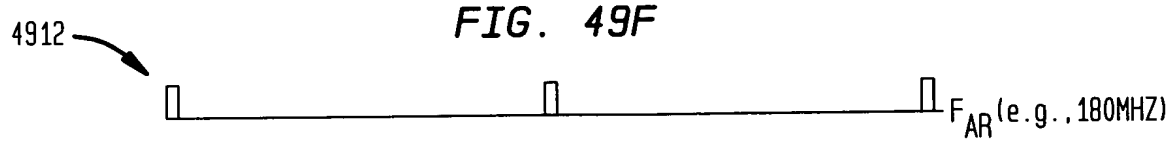


FIG. 49G

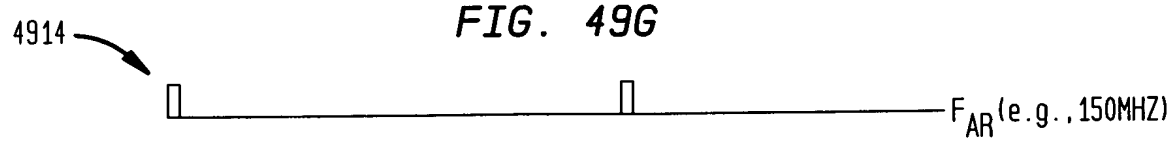


FIG. 49H

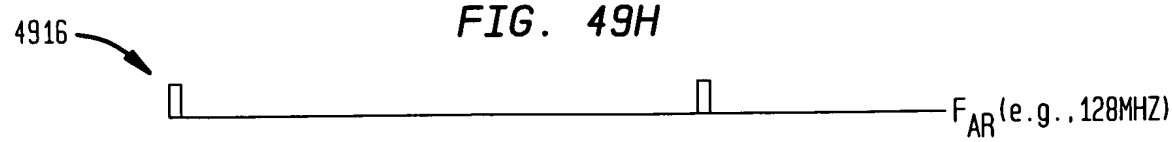

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FIG. 50A

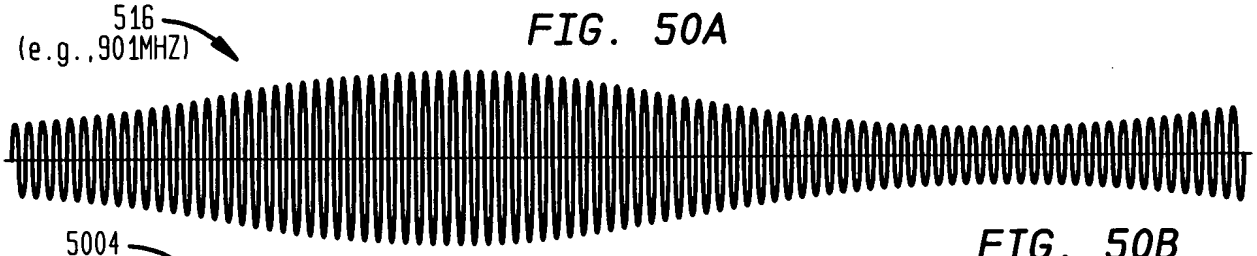


FIG. 50B

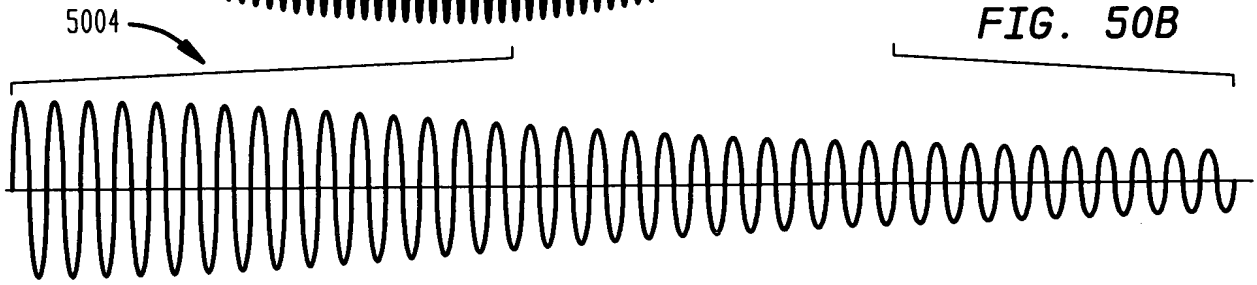


FIG. 50D

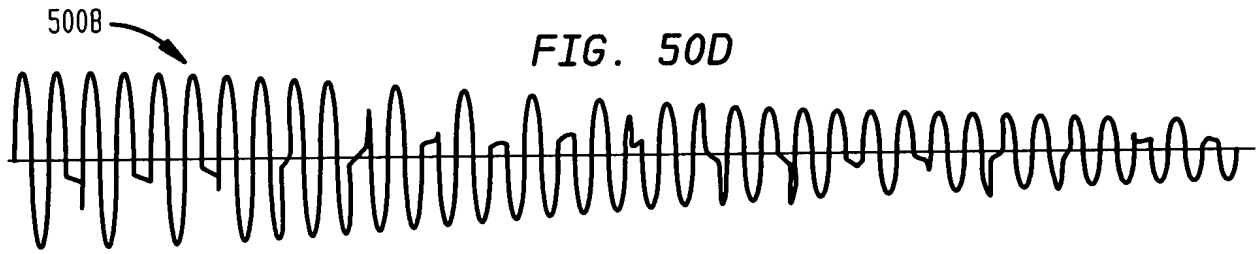


FIG. 50C

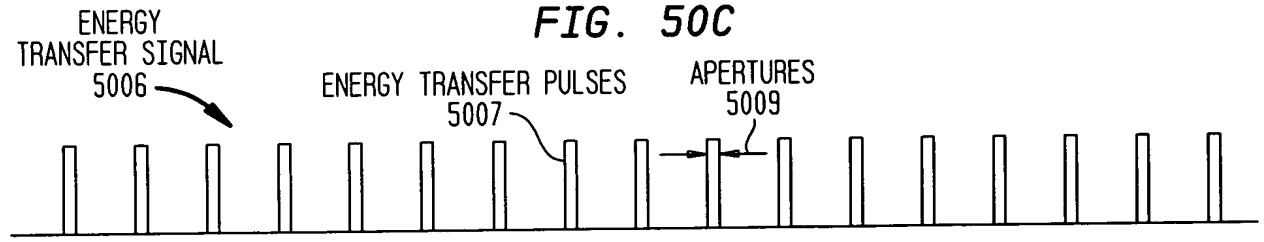


FIG. 50E

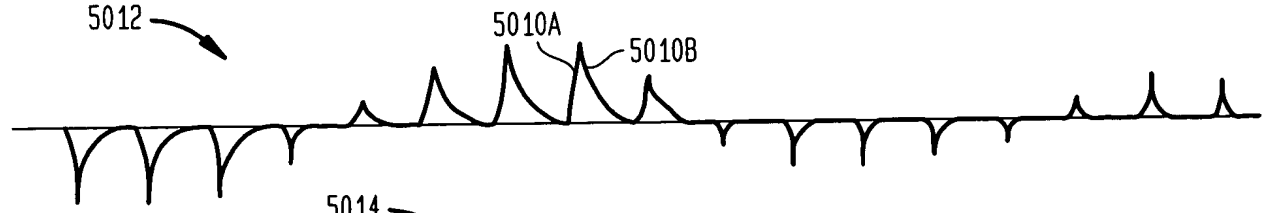


FIG. 50F

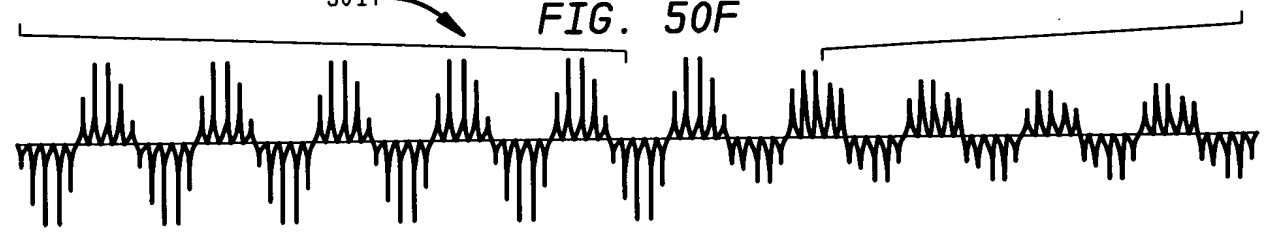


FIG. 50G

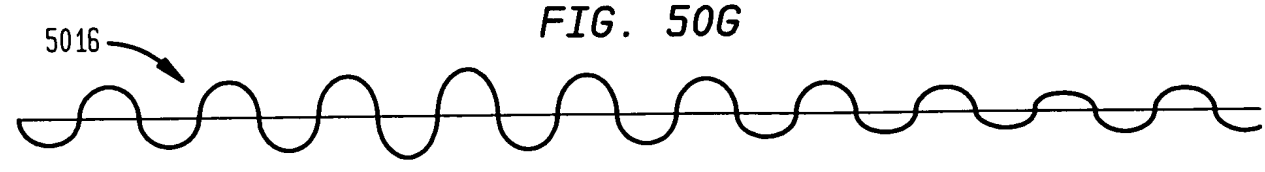

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FIG. 51A

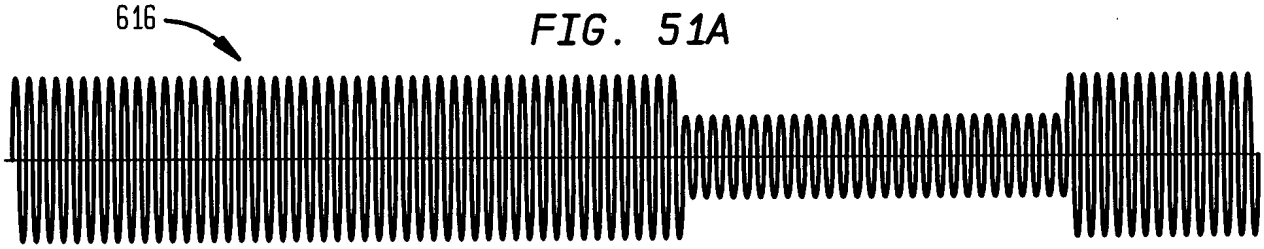


FIG. 51B

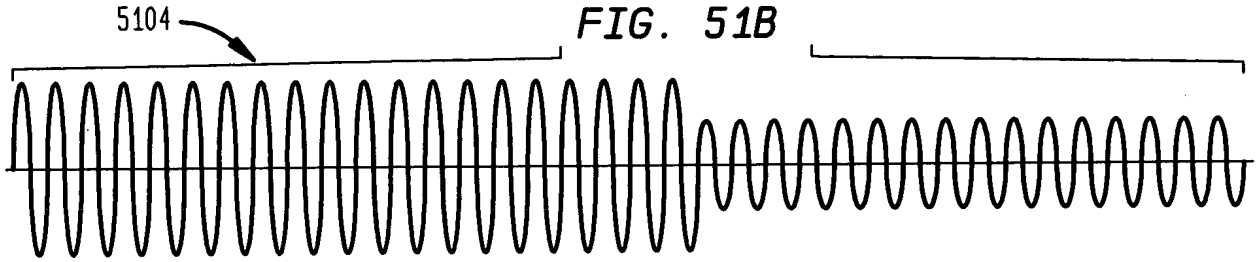


FIG. 51D

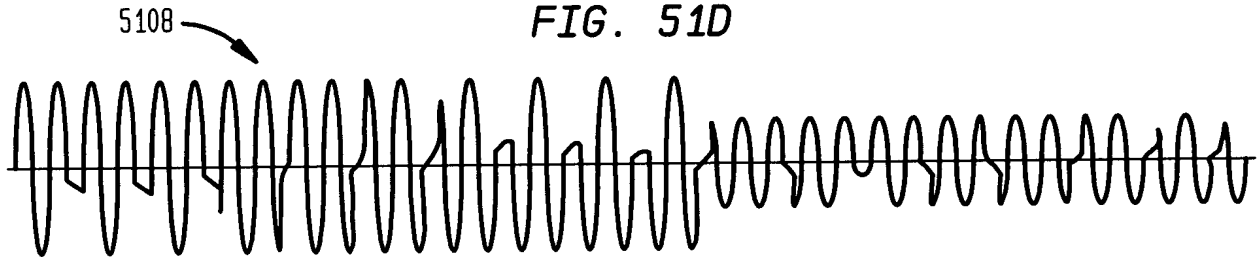


FIG. 51C

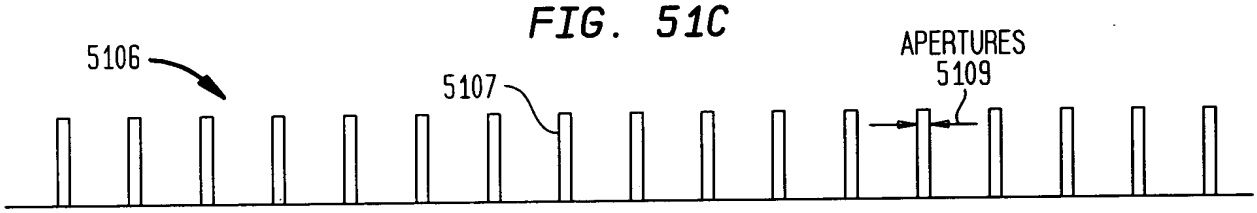


FIG. 51E

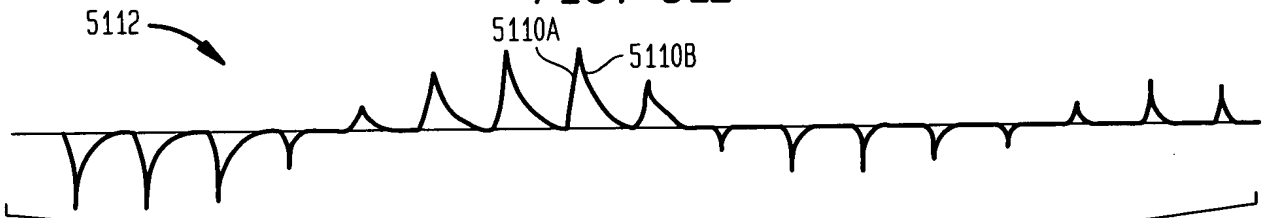


FIG. 51F

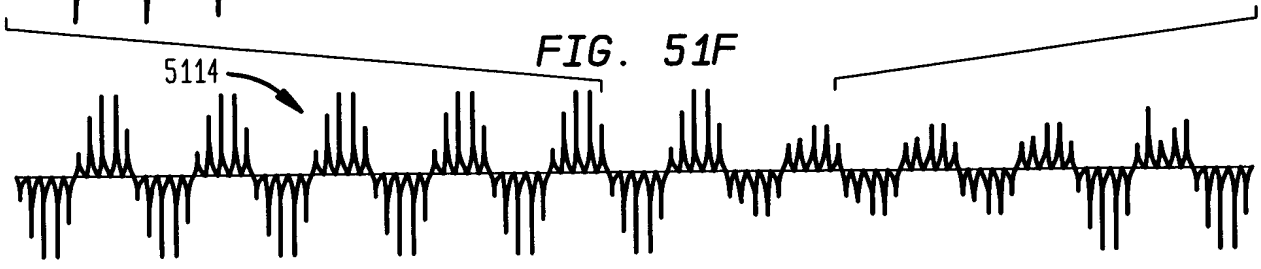


FIG. 51G

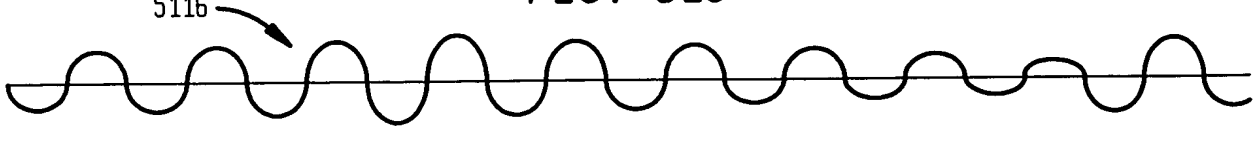

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FIG. 52A

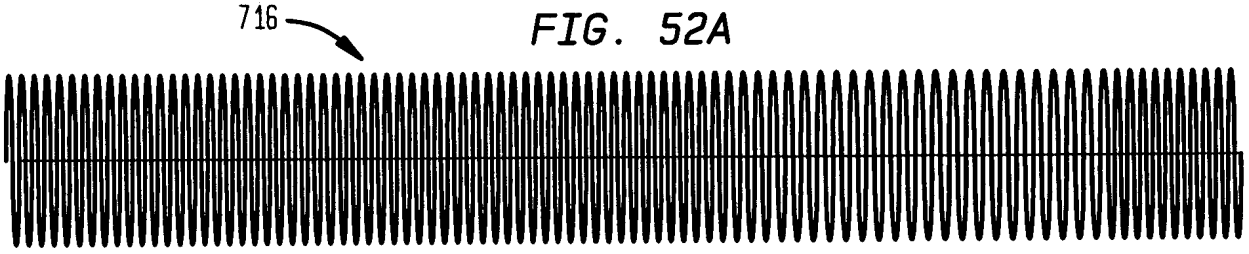



FIG. 52B

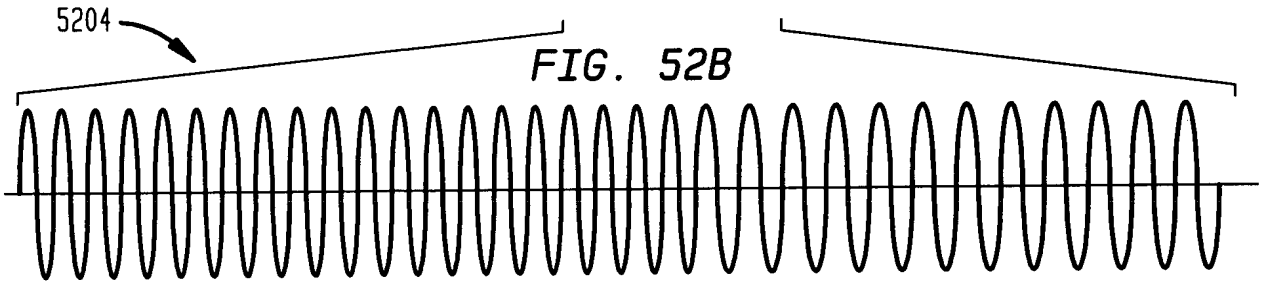



FIG. 52D

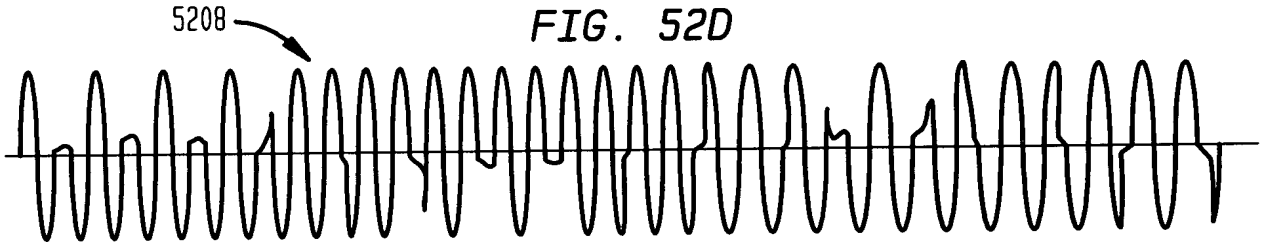



FIG. 52C

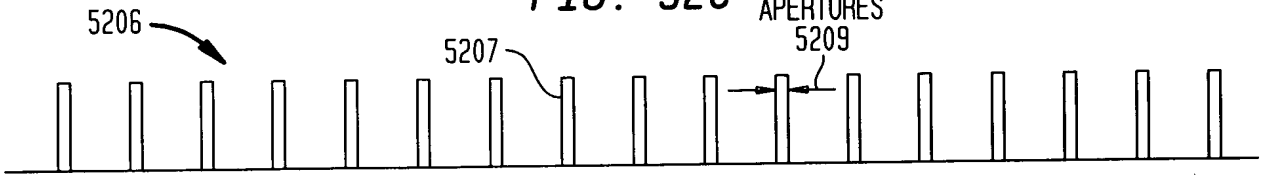



FIG. 52E

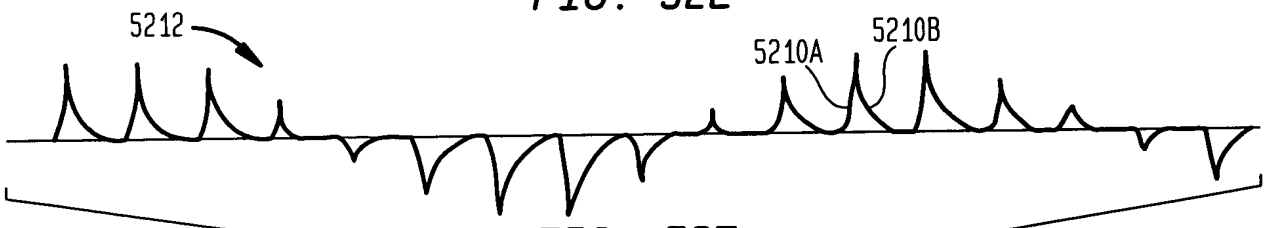



FIG. 52F

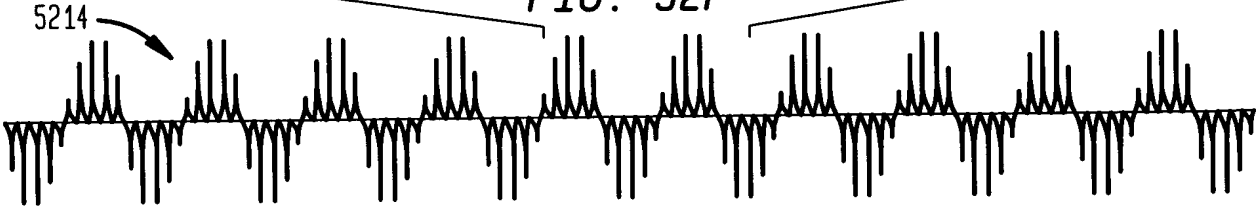
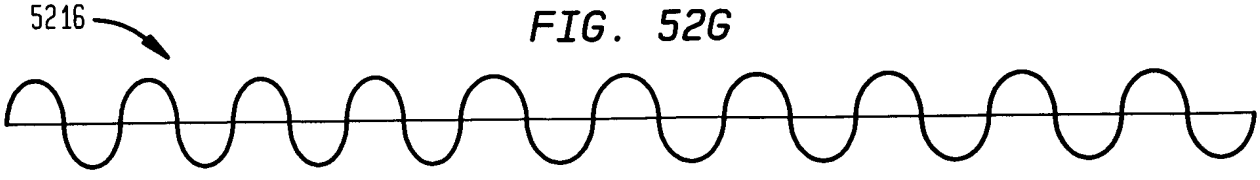



FIG. 52G



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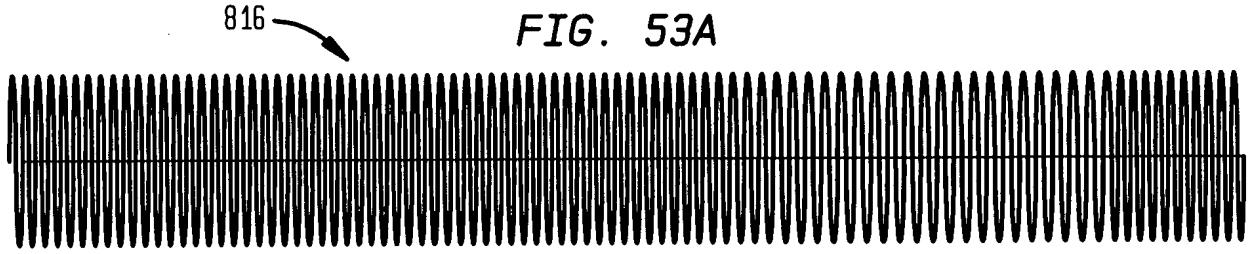


FIG. 53A

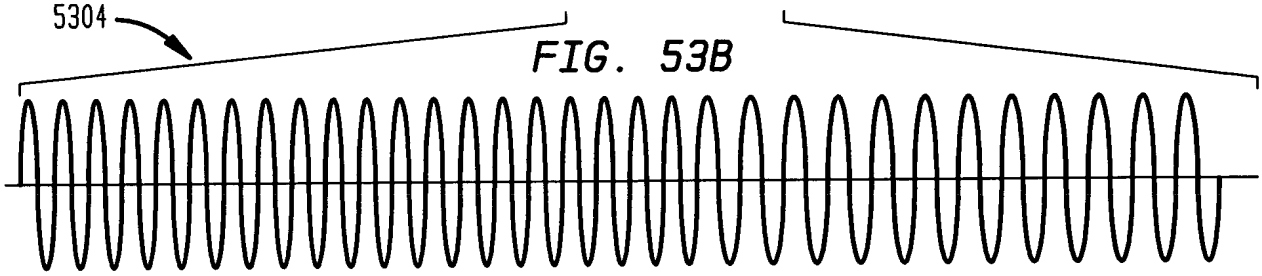


FIG. 53B

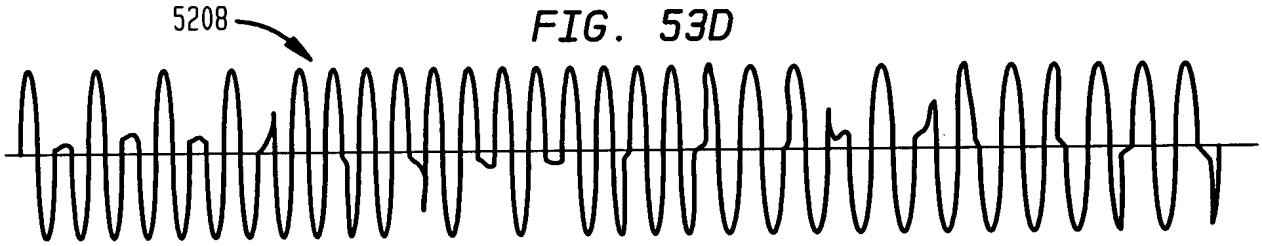


FIG. 53D

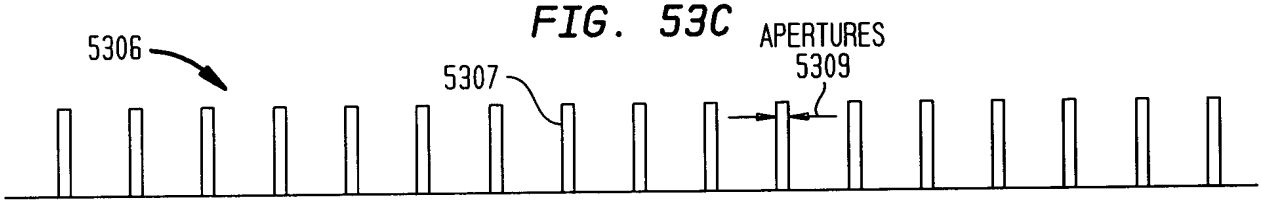


FIG. 53C

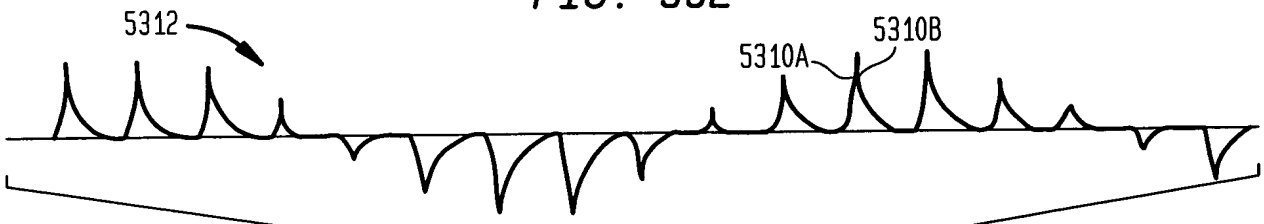


FIG. 53E

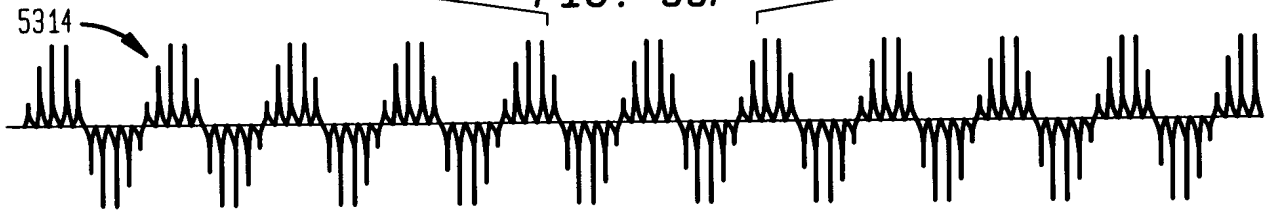


FIG. 53F

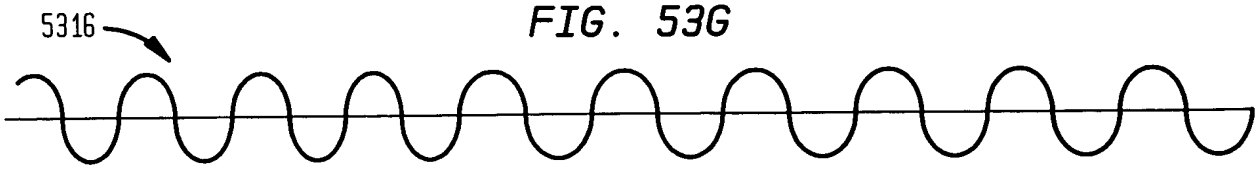


FIG. 53G

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FIG. 54A

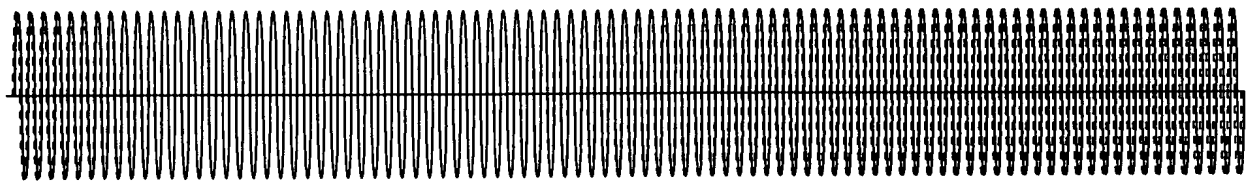



FIG. 54B

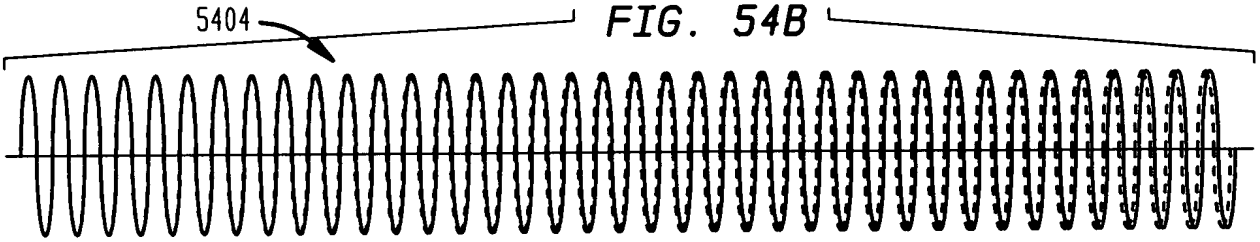



FIG. 54D

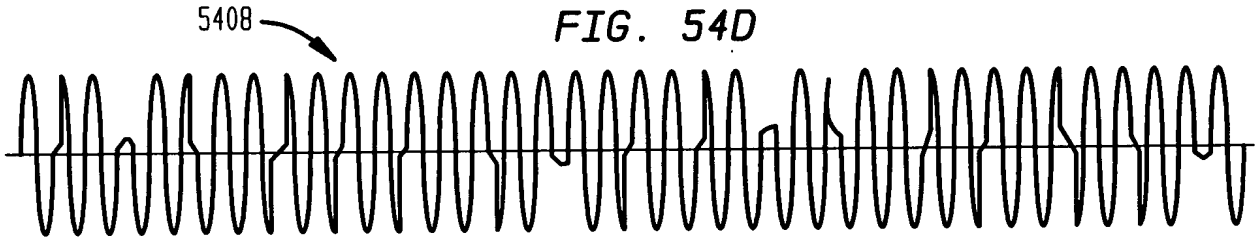



FIG. 54C

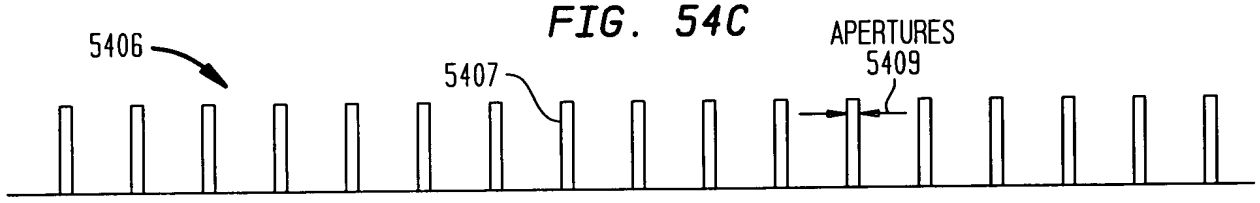



FIG. 54E

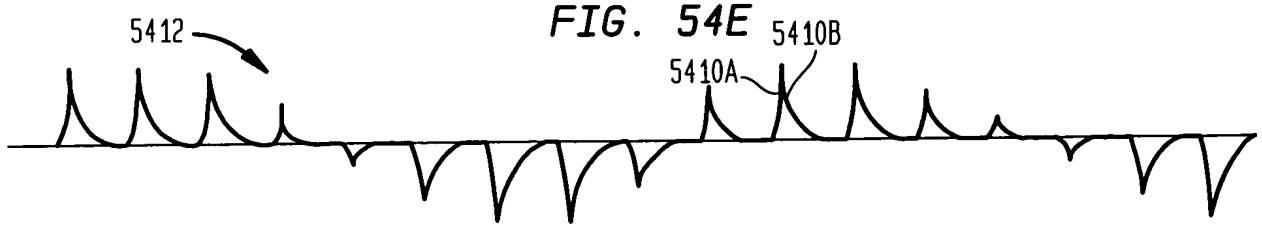



FIG. 54F

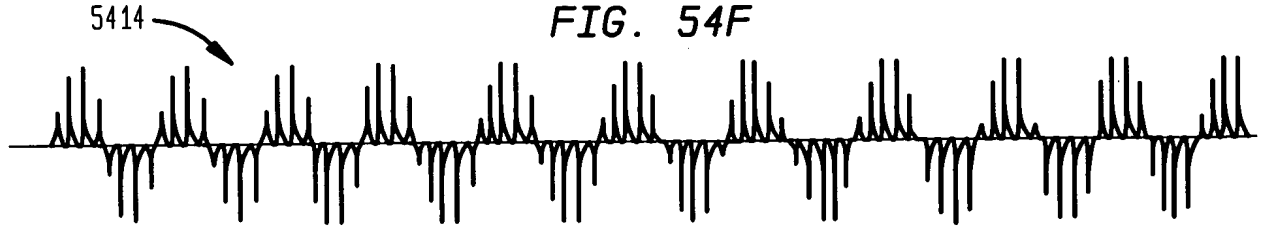
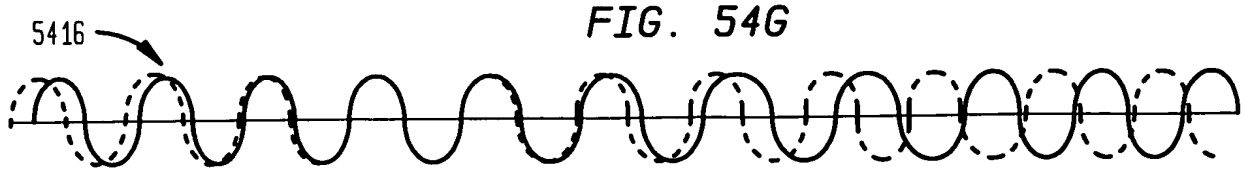



FIG. 54G



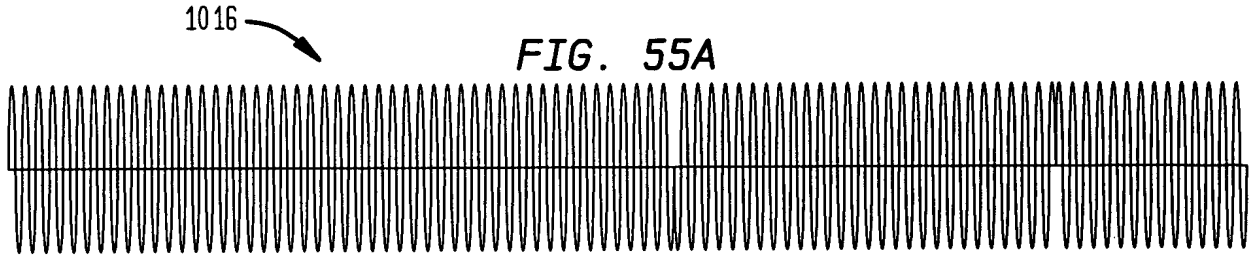



FIG. 55A

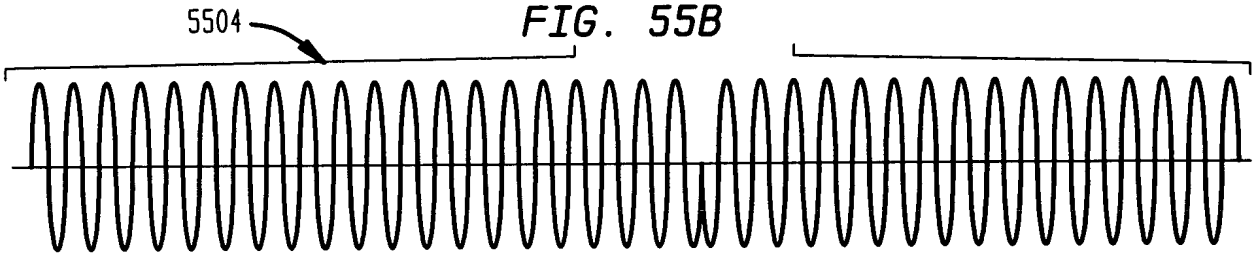



FIG. 55B

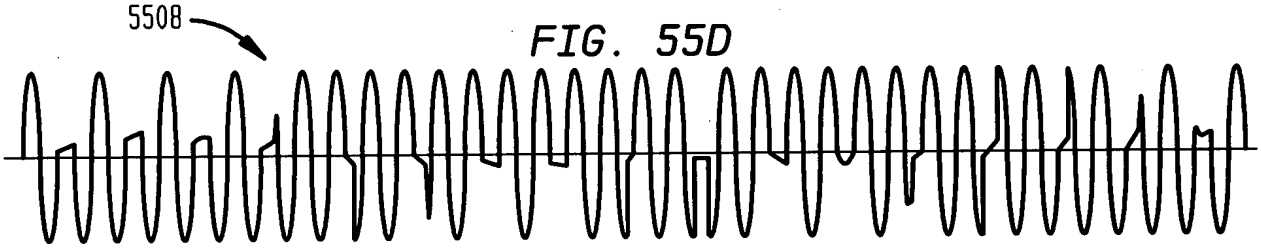
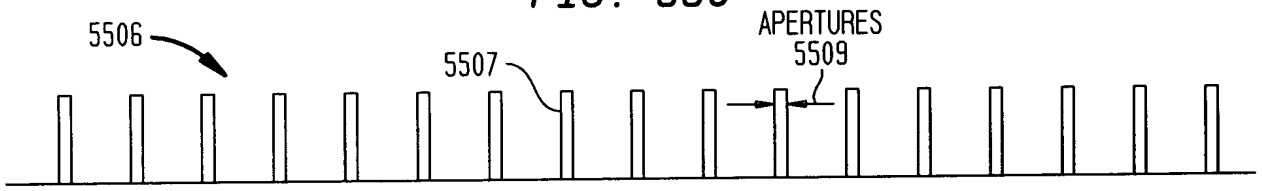



FIG. 55D

FIG. 55C



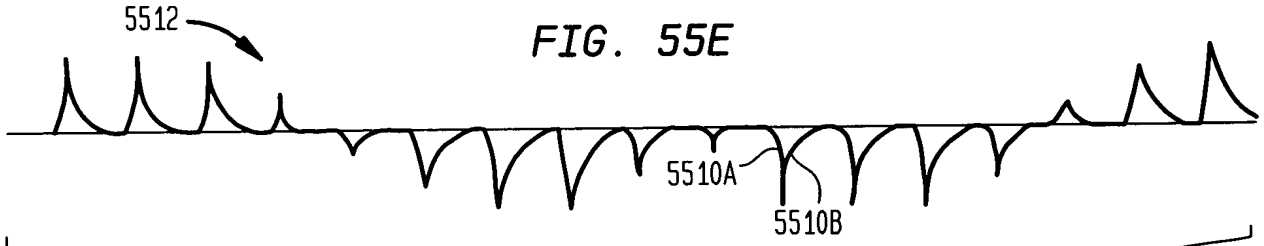
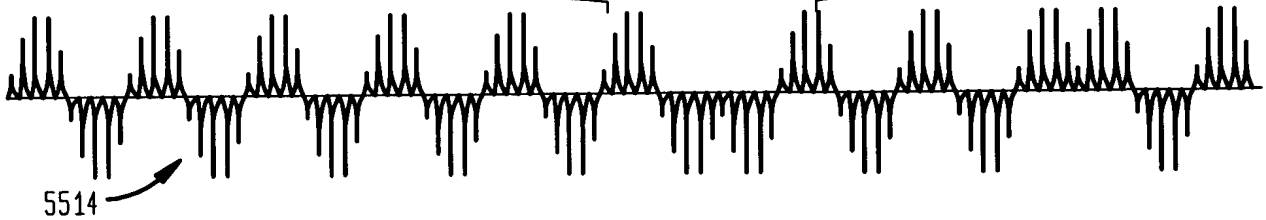




FIG. 55E

FIG. 55F



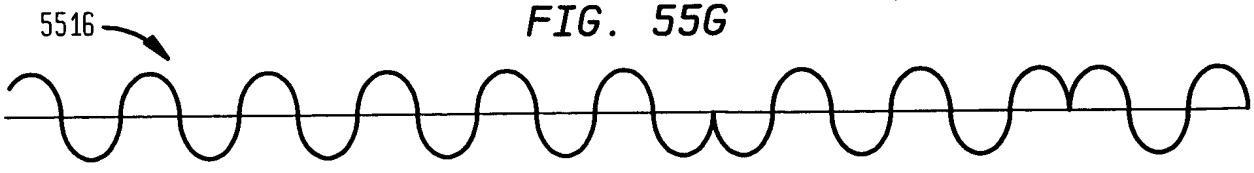




FIG. 55G

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FIG. 56A

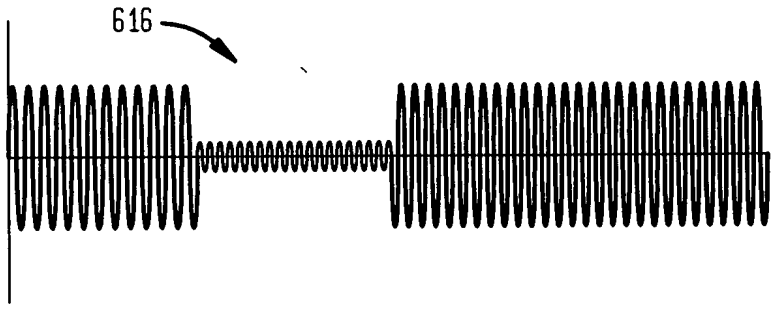


FIG. 56B

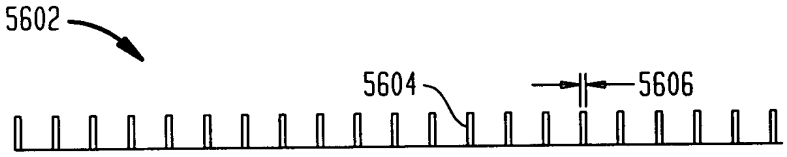


FIG. 56C

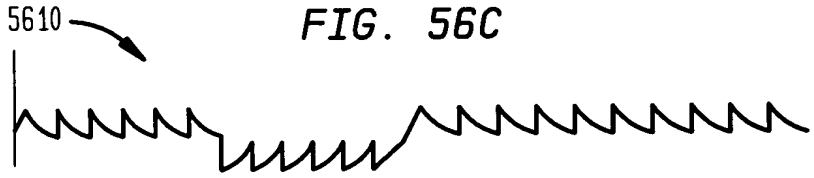


FIG. 56D

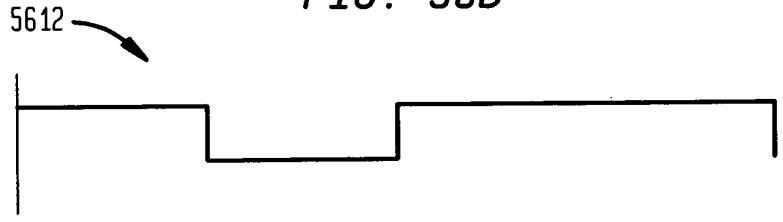

FIG. 57A

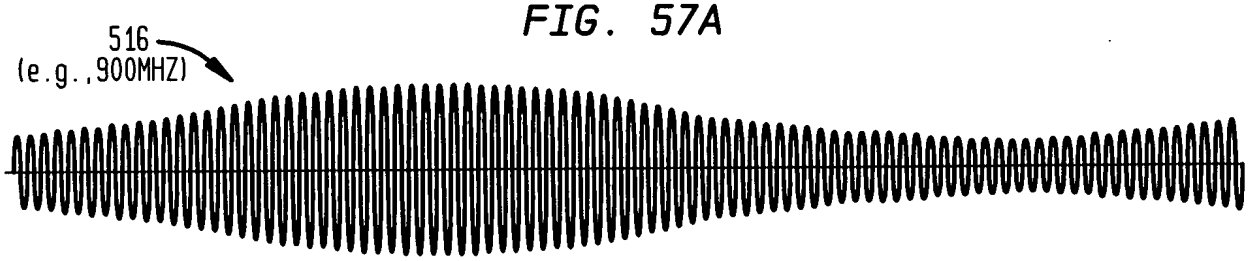


FIG. 57B

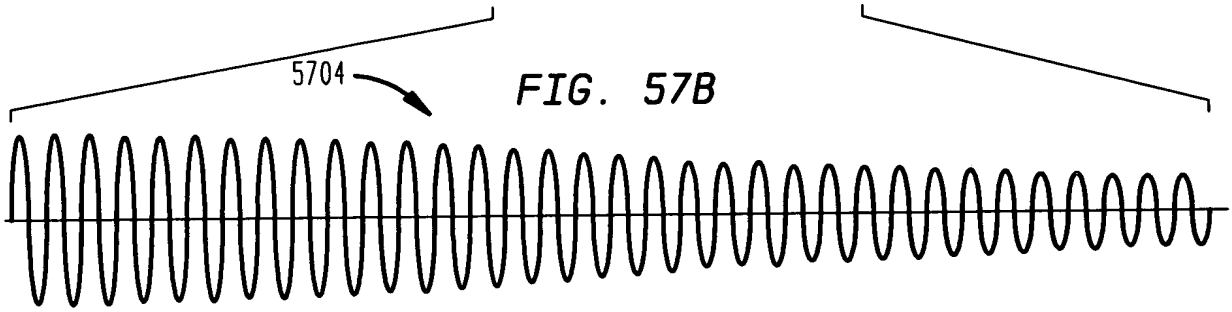


FIG. 57D

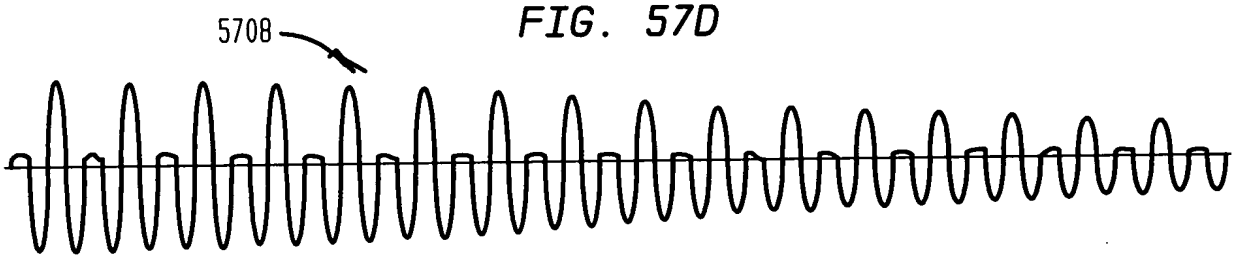


FIG. 57C

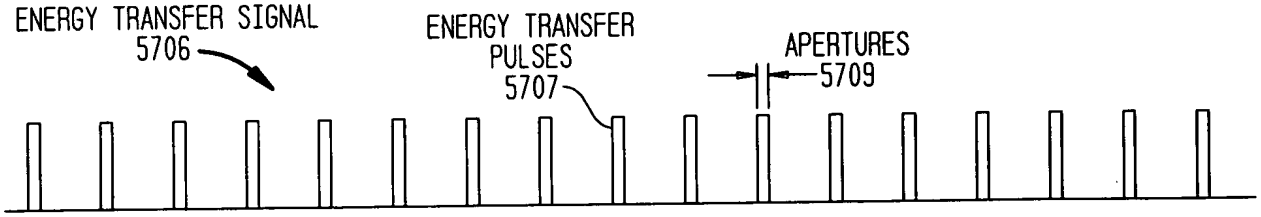


FIG. 57E

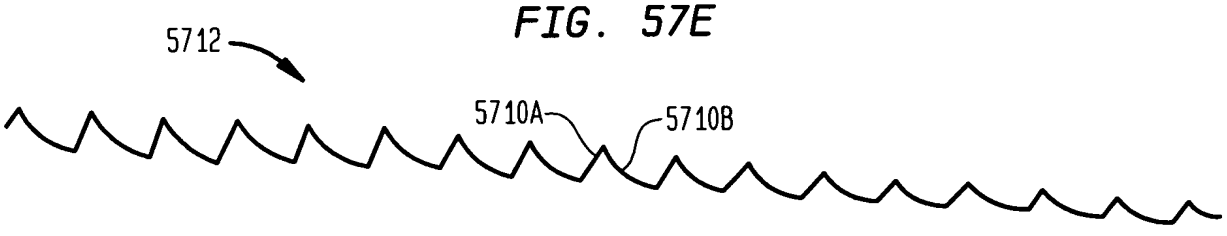


FIG. 57F

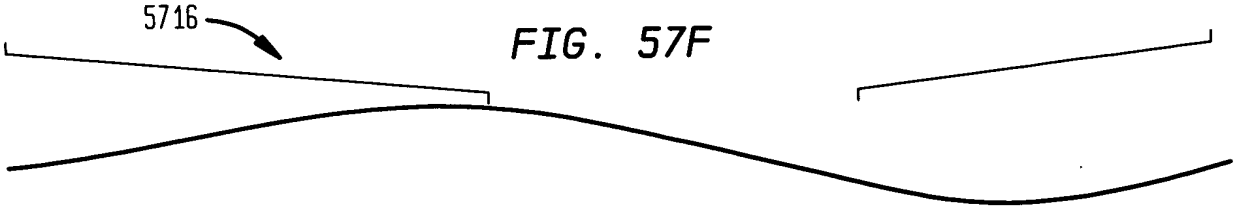

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FIG. 58A

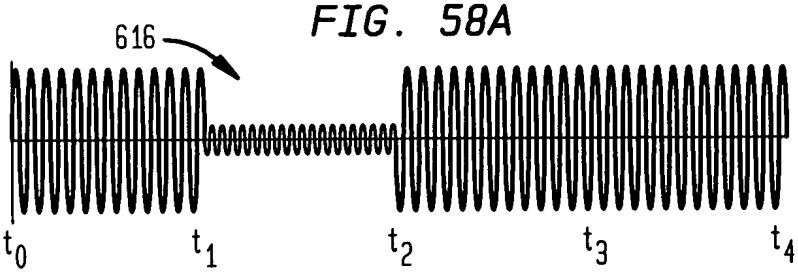


FIG. 58B

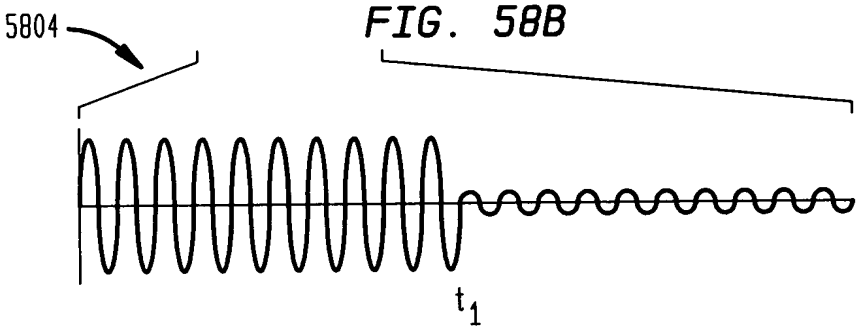


FIG. 58D

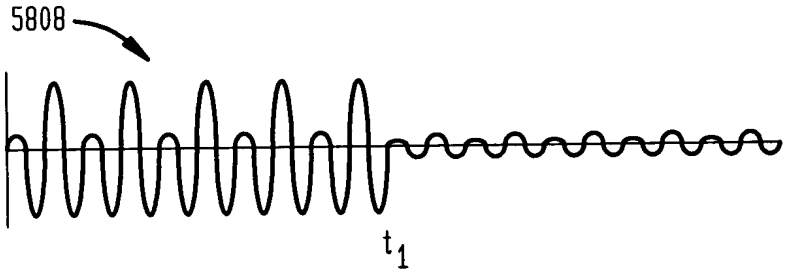


FIG. 58C

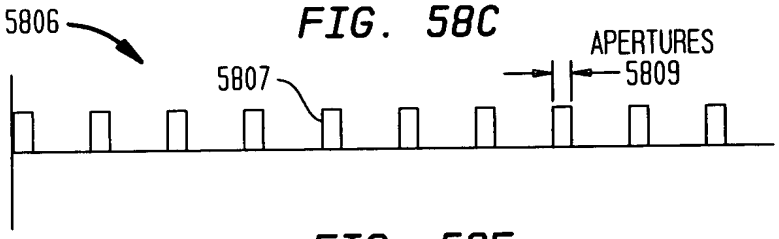


FIG. 58E

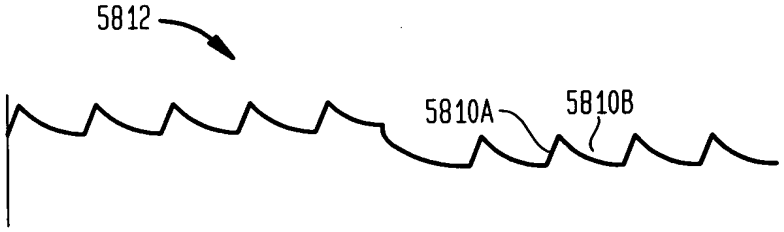


FIG. 58F

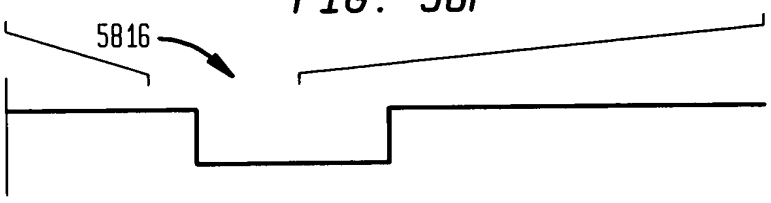

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FIG. 59A

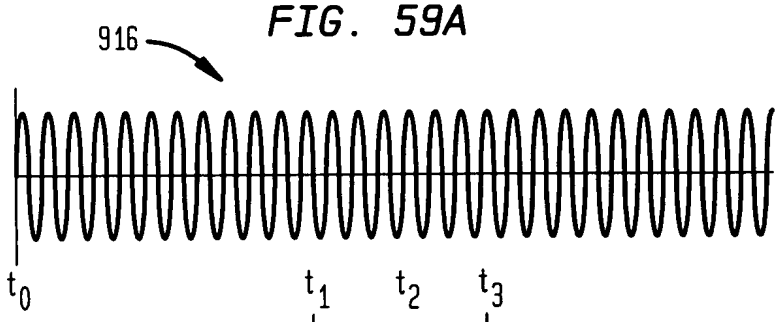


FIG. 59B

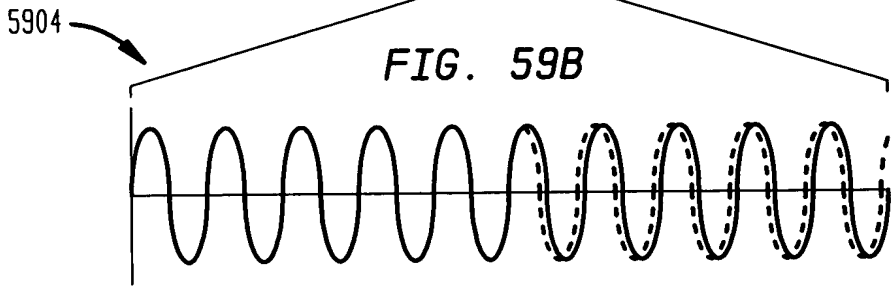


FIG. 59D

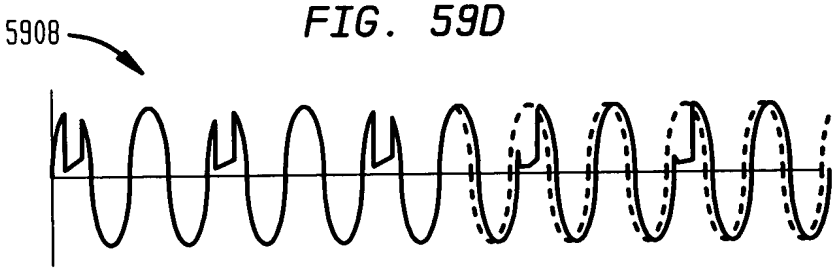


FIG. 59C

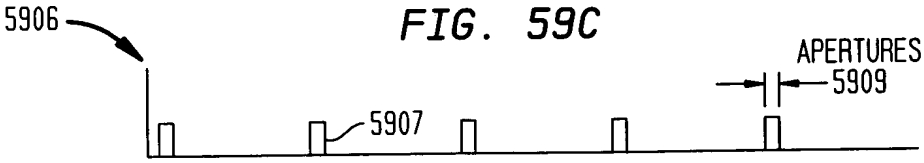


FIG. 59E

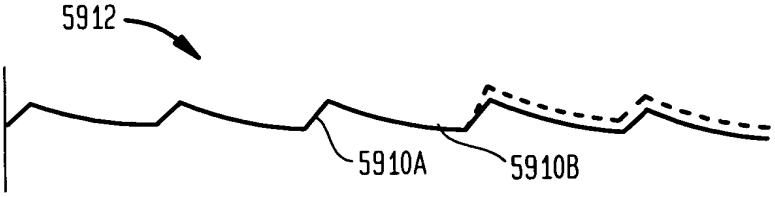


FIG. 59F

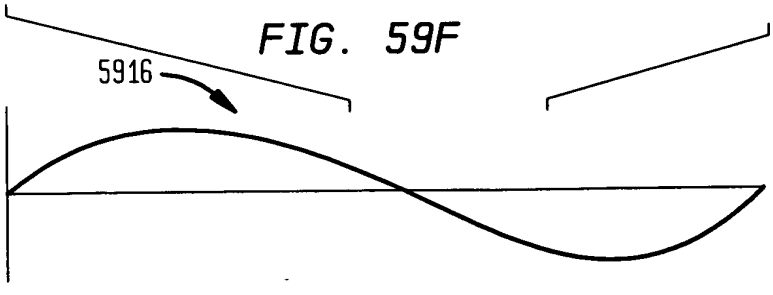

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FIG. 60A

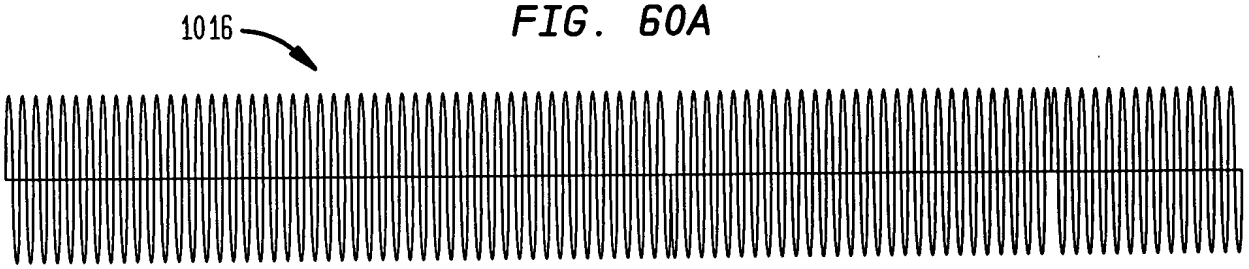



FIG. 60B

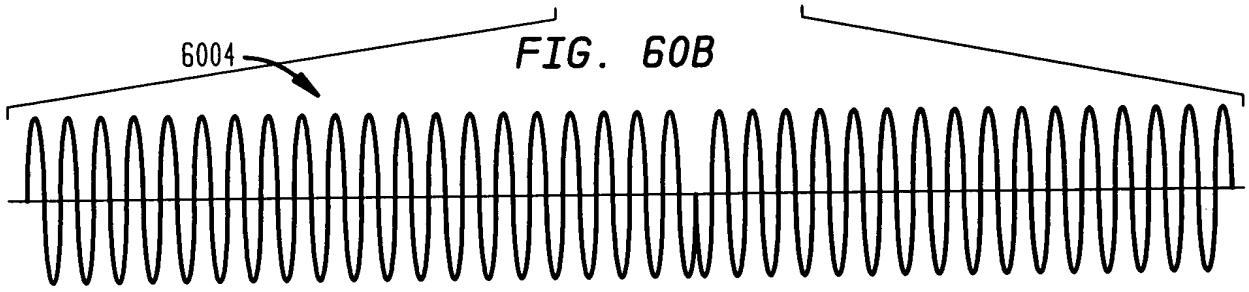



FIG. 60D

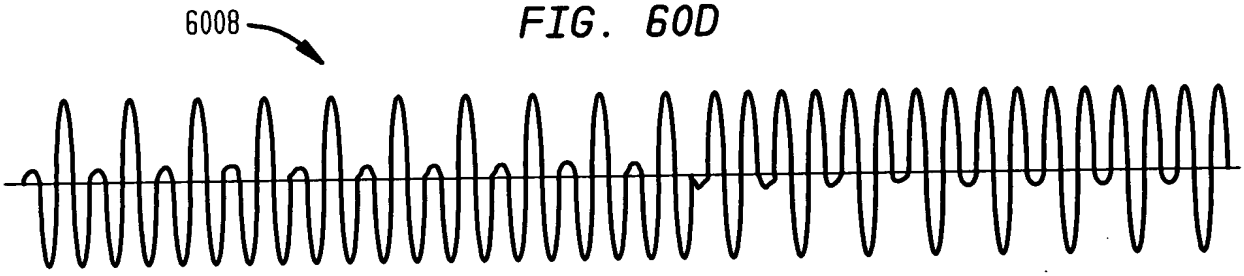



FIG. 60C

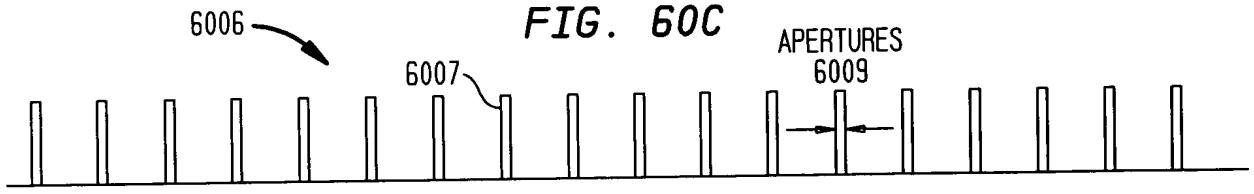
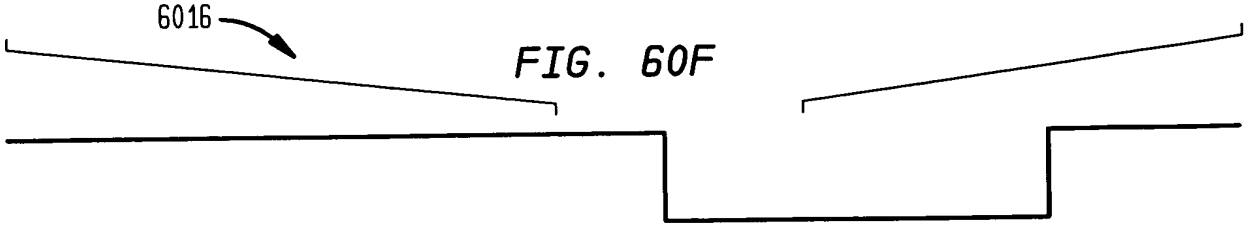



FIG. 60E


FIG. 60F



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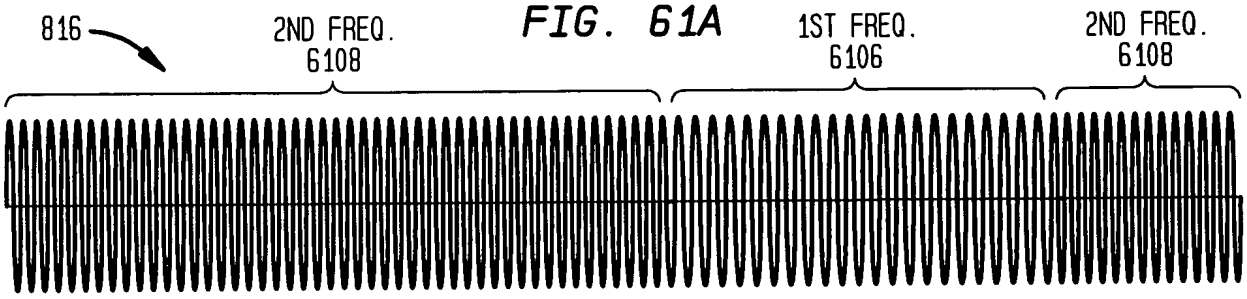


FIG. 61A

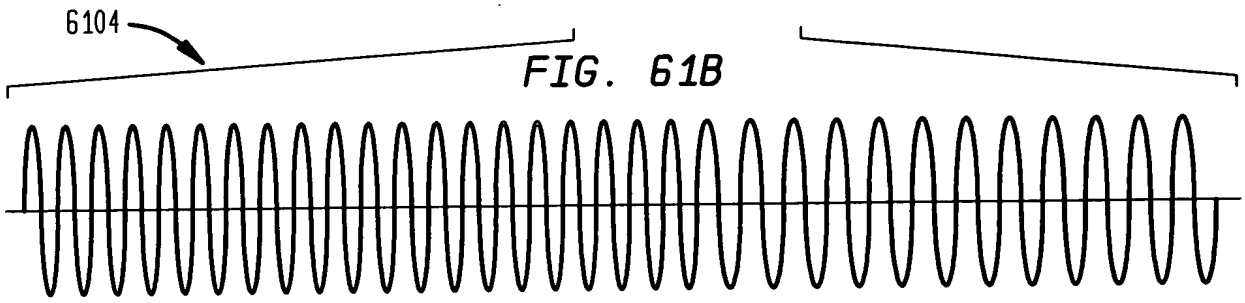


FIG. 61B

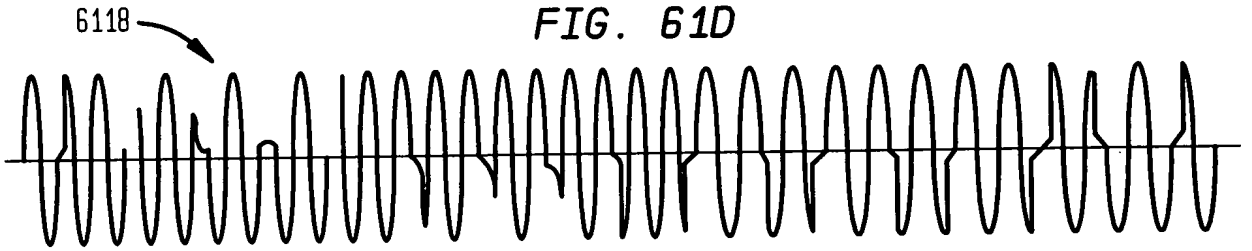


FIG. 61D

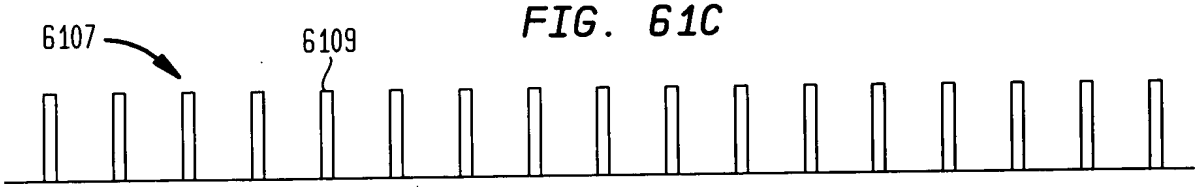


FIG. 61C

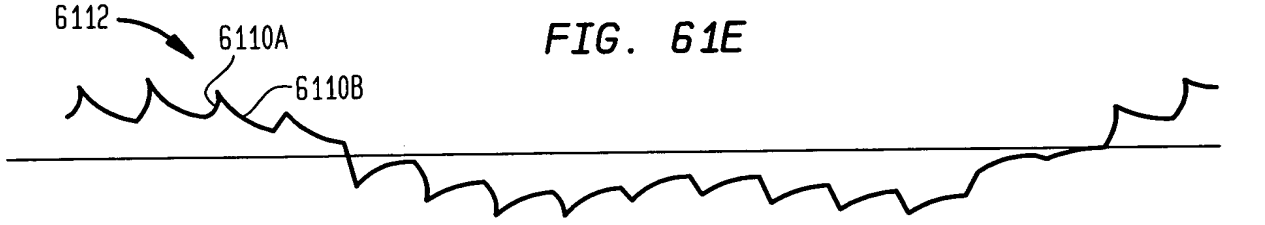


FIG. 61E

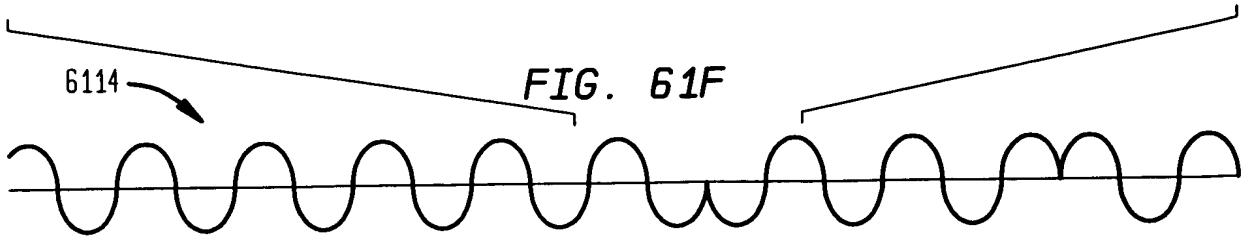


FIG. 61F

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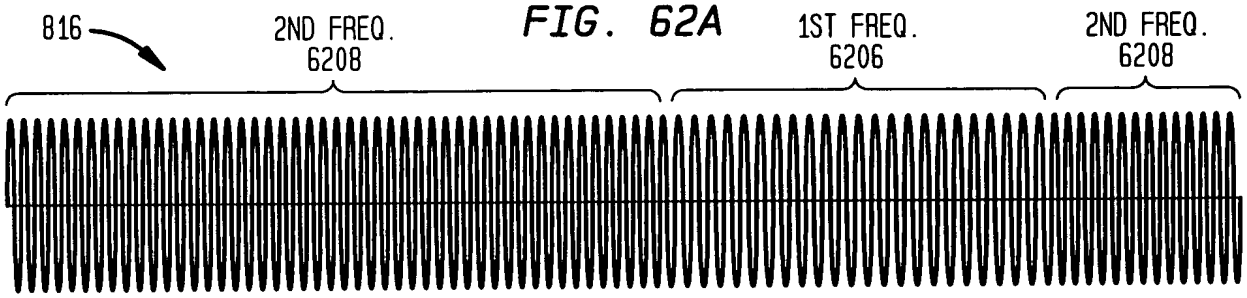



FIG. 62A

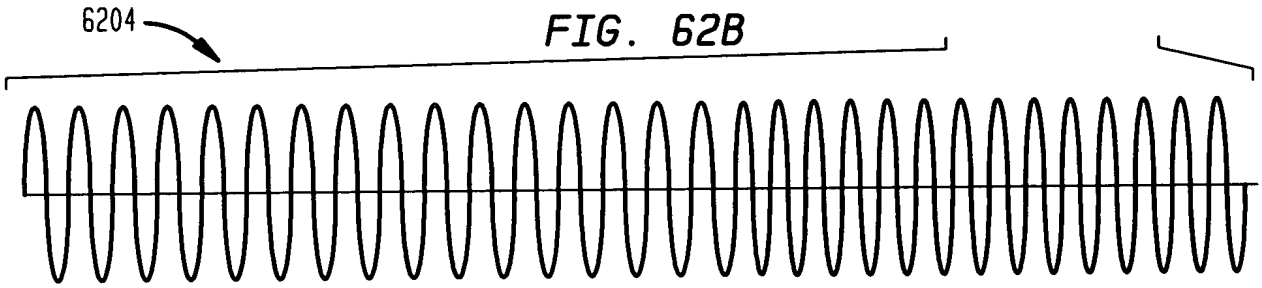



FIG. 62B

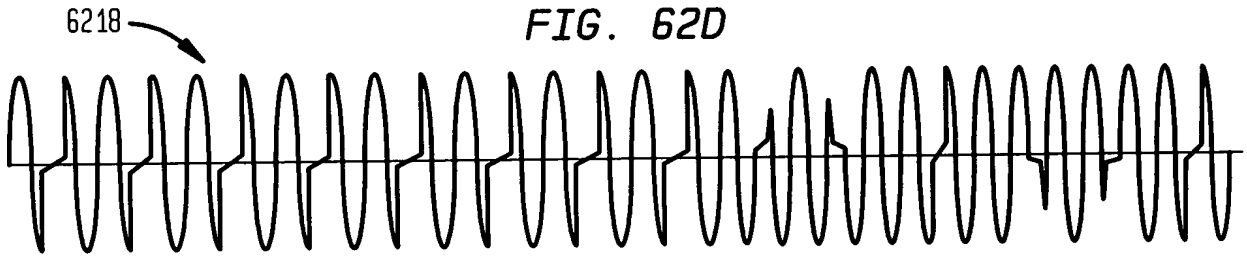



FIG. 62D

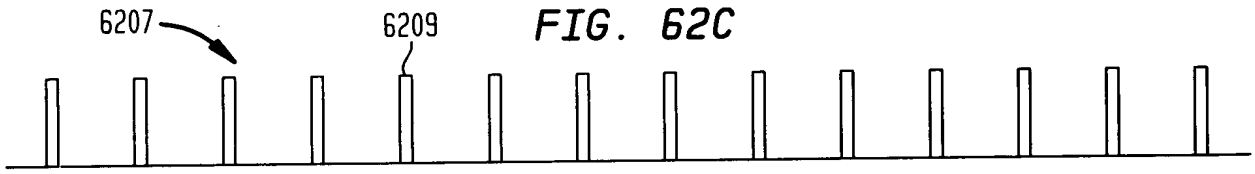



FIG. 62C

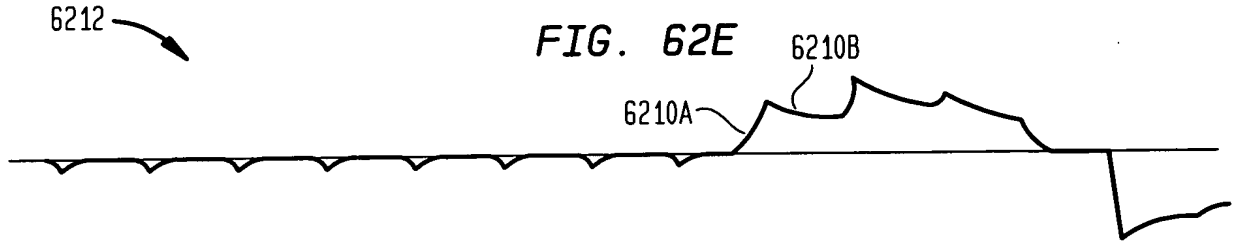



FIG. 62E

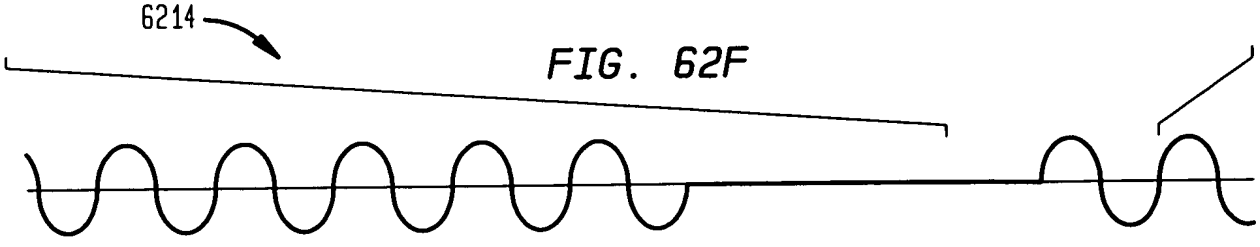



FIG. 62F

FIG. 63

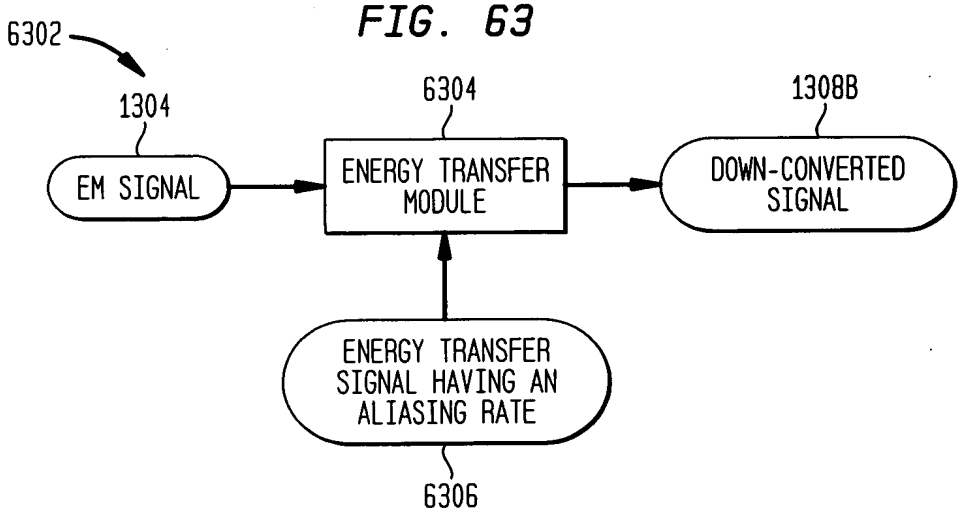



FIG. 64A

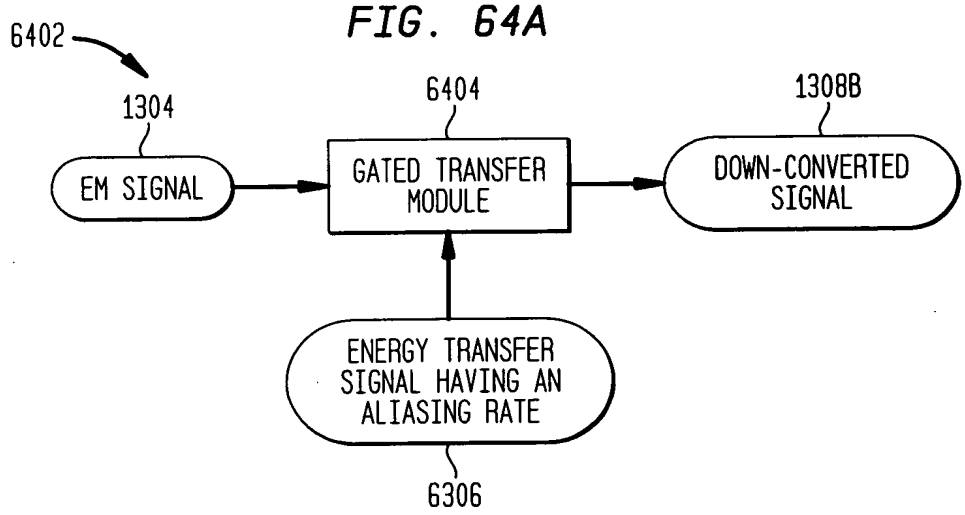



FIG. 64B

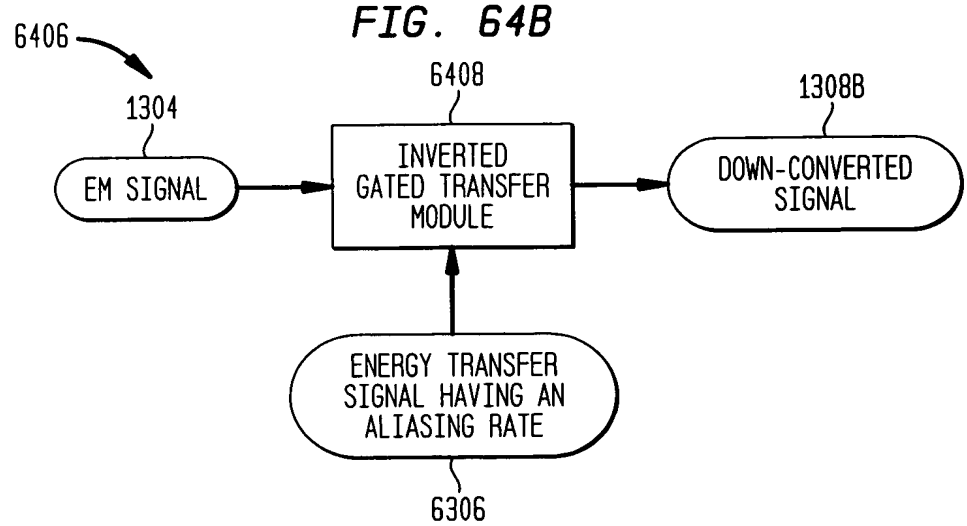


FIG. 65

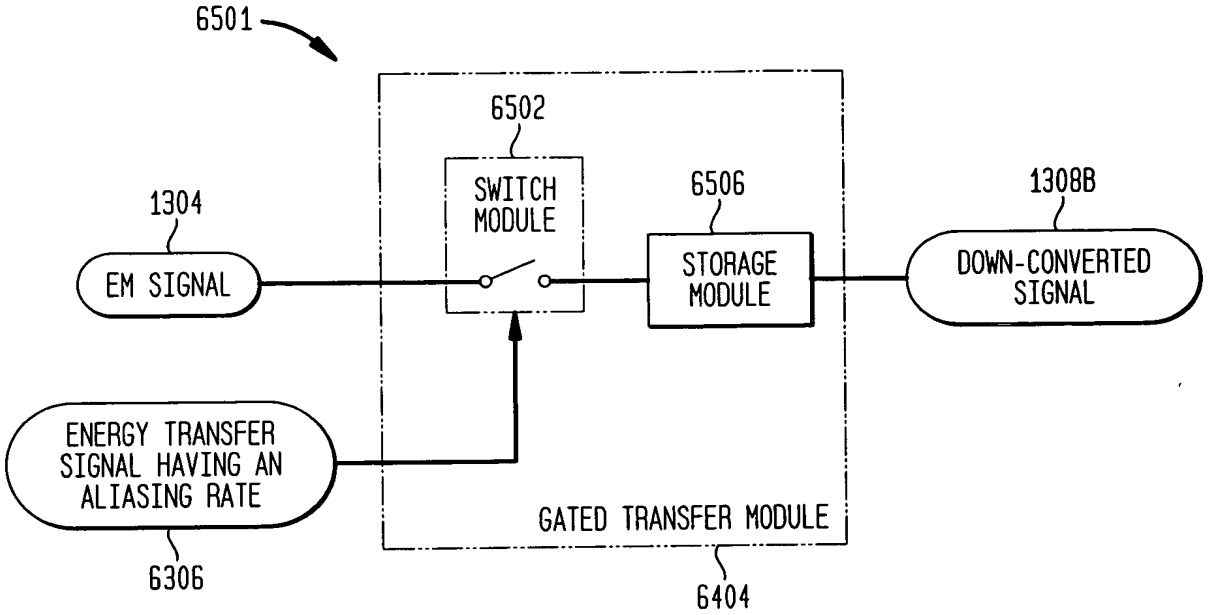



FIG. 66A

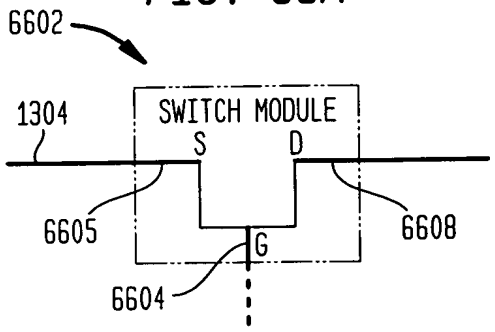



FIG. 66B

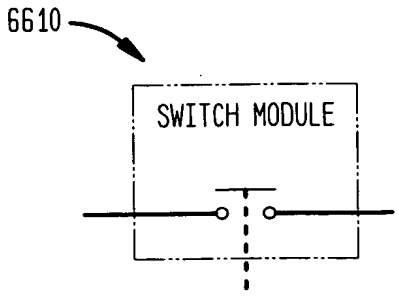


FIG. 66C

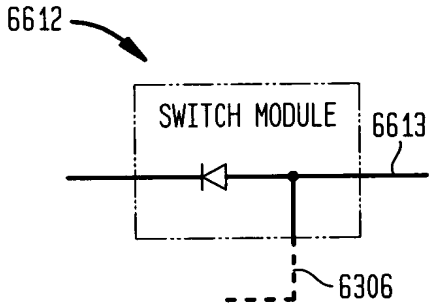



FIG. 66D

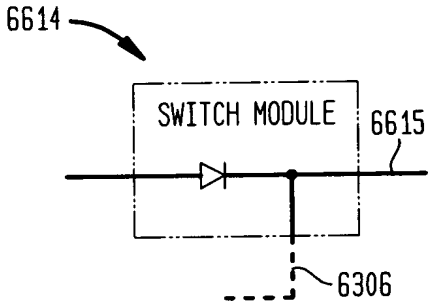


FIG. 67A

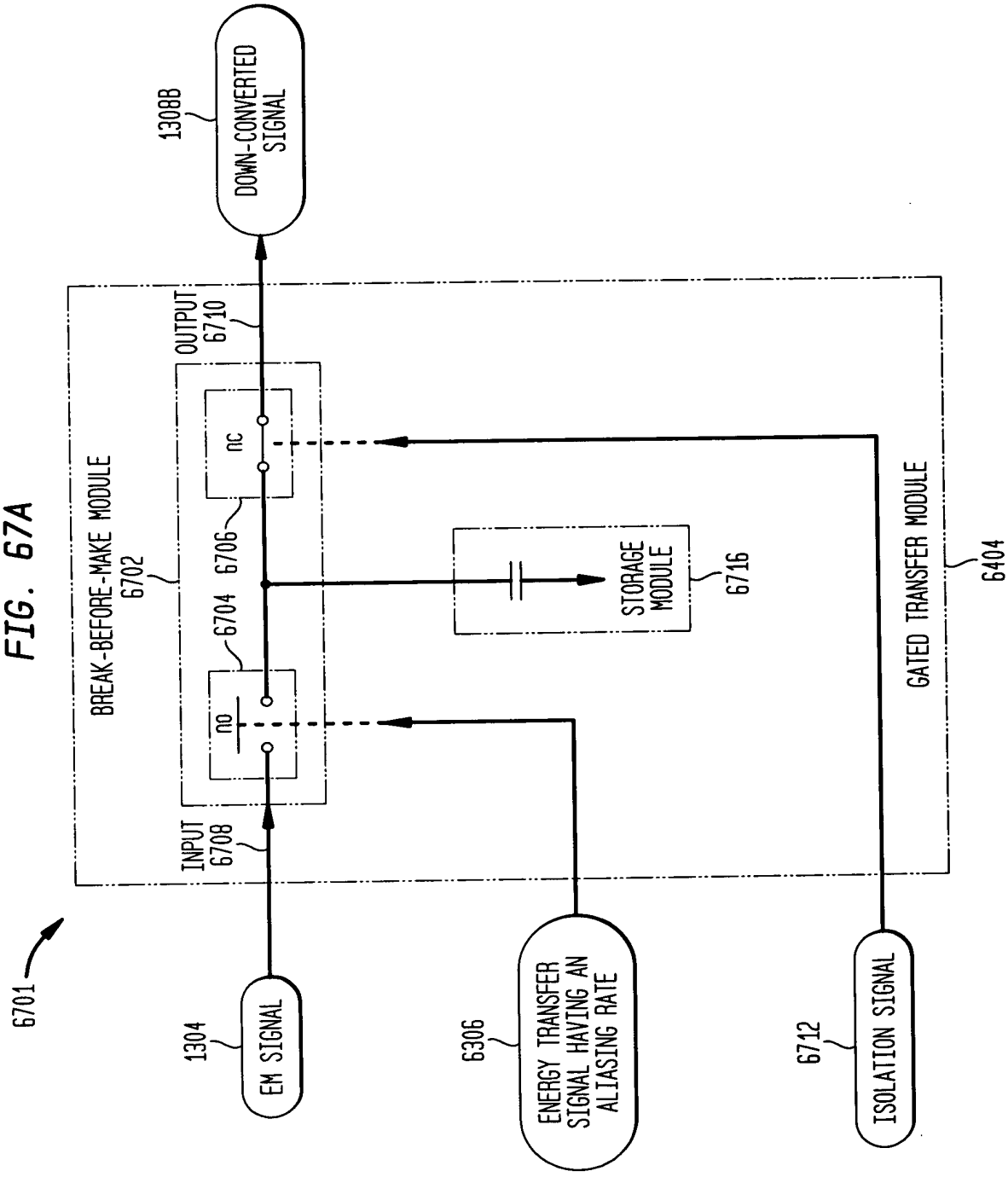

6701
BREAK-BEFORE-MAKE MODULE
6702
INPUT
6708
OUTPUT
6710
nc
no
6704
6706
STORAGE MODULE
6716
GATED TRANSFER MODULE
6404
1308B
DOWN-CONVERTED SIGNAL
1304
EM SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
6712
ISOLATION SIGNAL

FIG. 67B

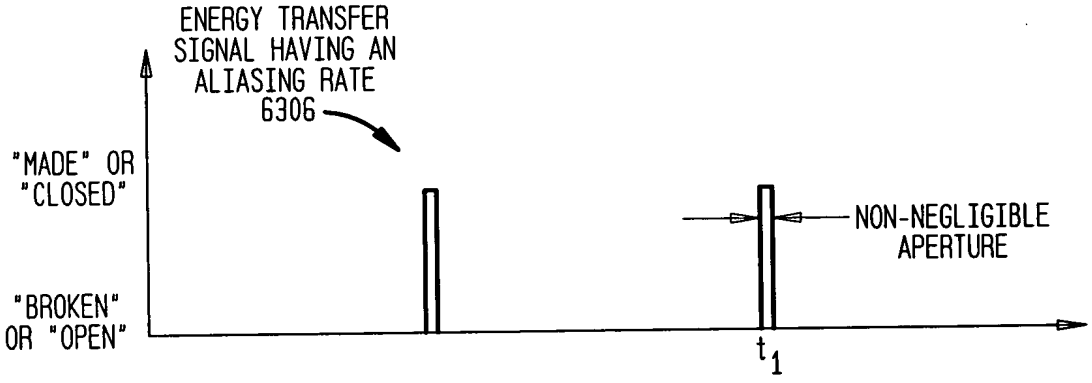



FIG. 67C

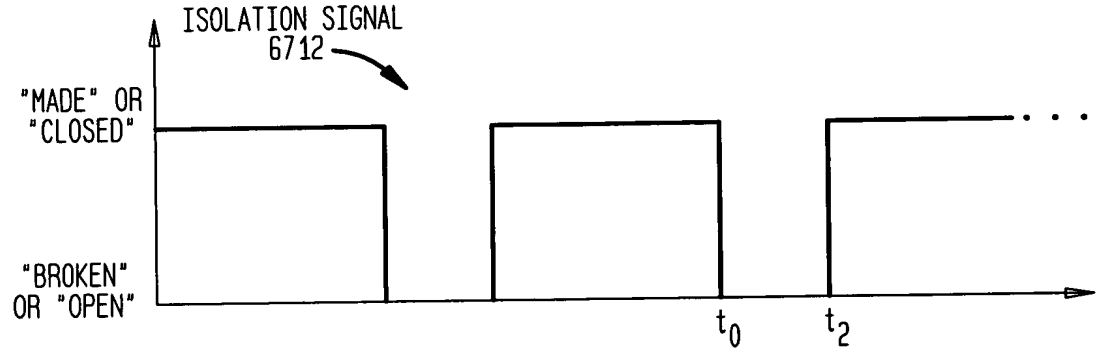


FIG. 68A

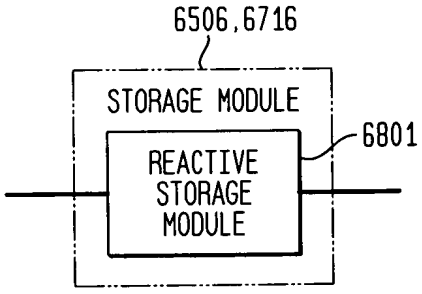



FIG. 68B

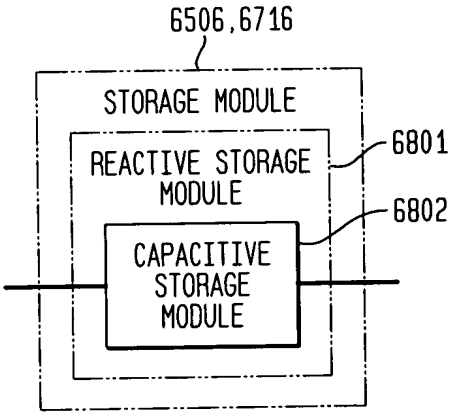



FIG. 68C

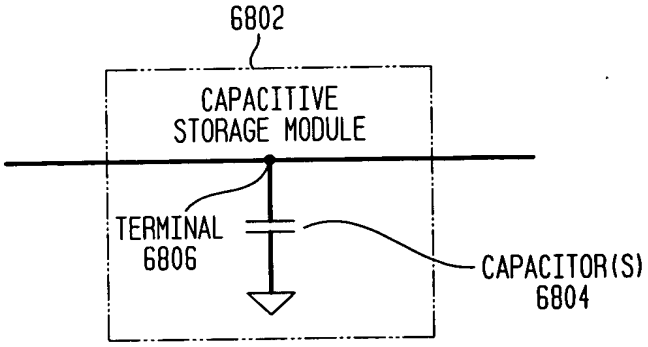


FIG. 68D

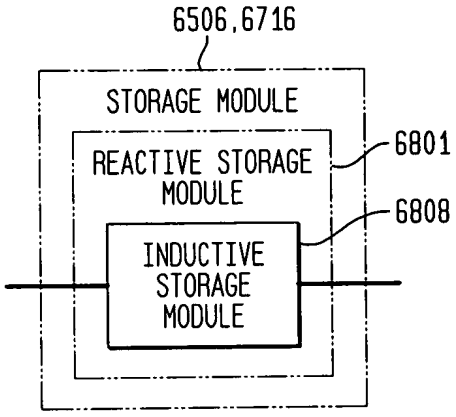



FIG. 68E

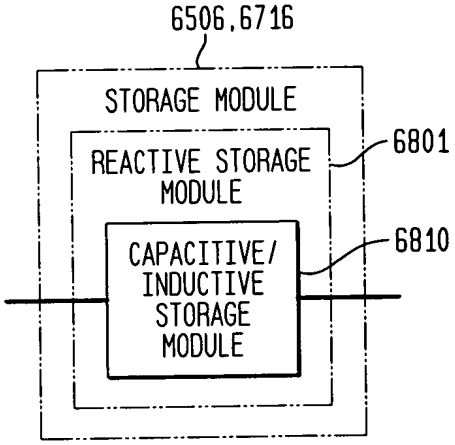



FIG. 68F

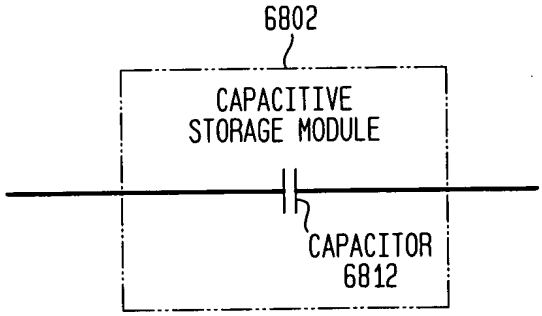


FIG. 68G

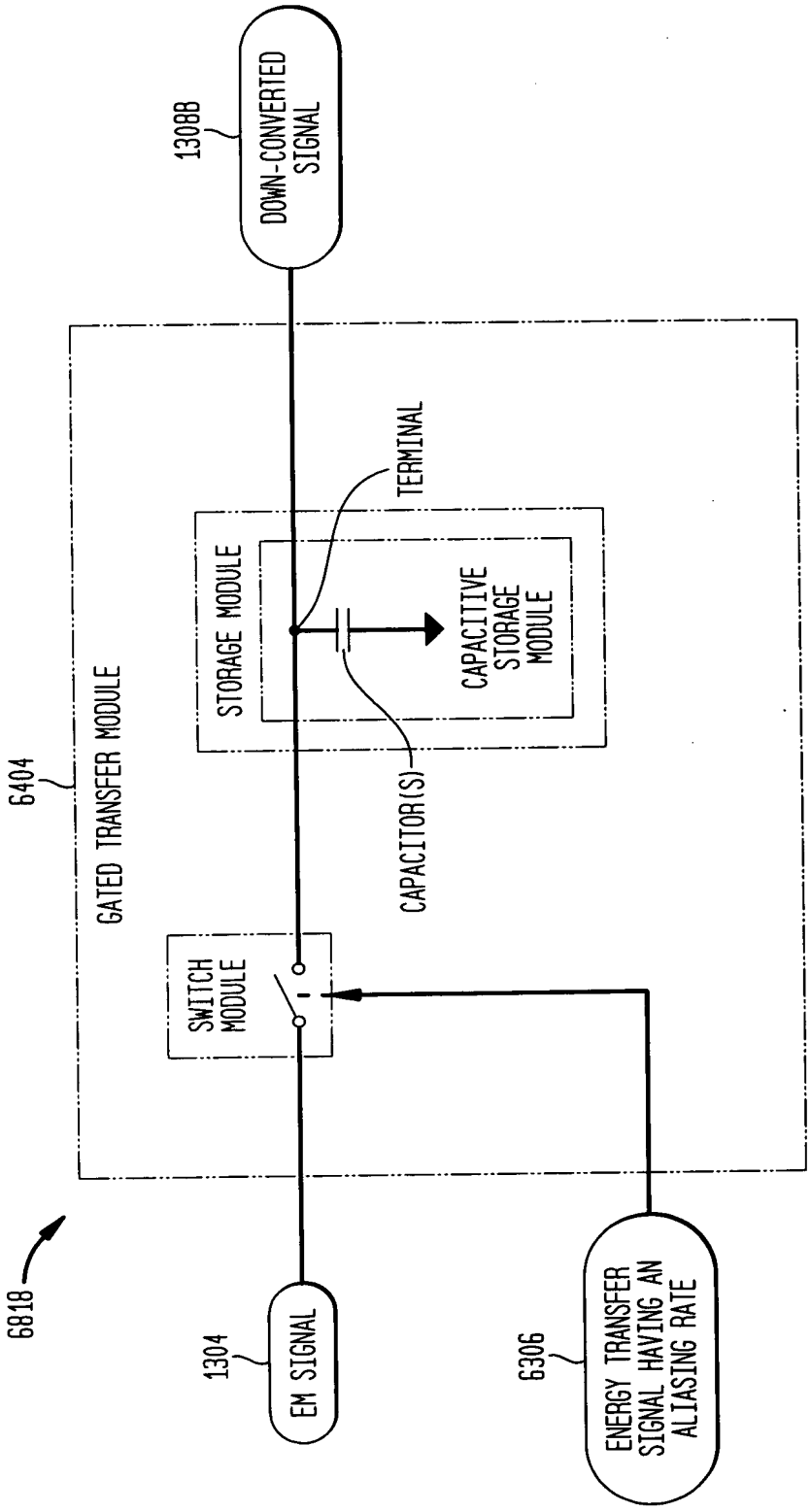
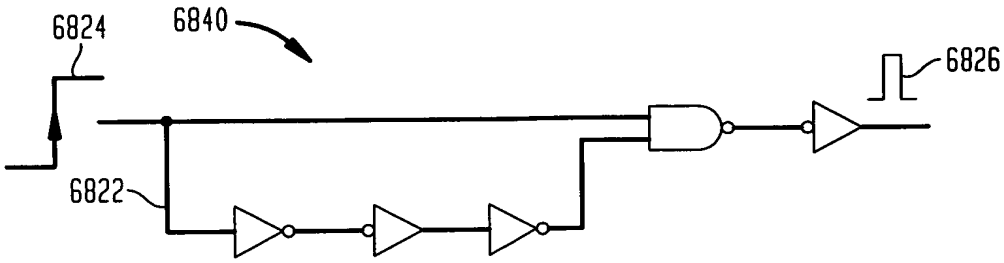
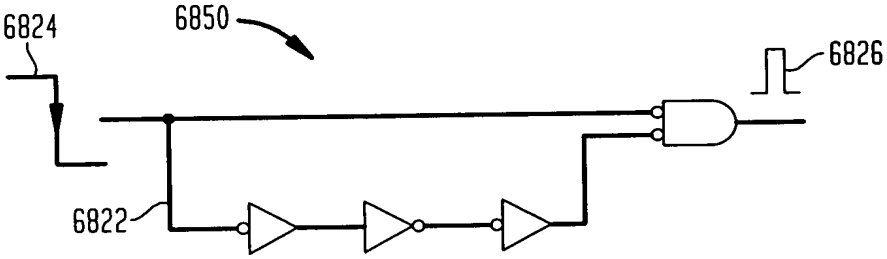

1308B
DOWN-CONVERTED SIGNAL
TERMINAL
STORAGE MODULE
CAPACITIVE STORAGE MODULE
CAPACITOR(S)
6404
GATED TRANSFER MODULE
SWITCH MODULE
6818
1304
EM SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE

FIG. 68H




A. RISING EDGE PULSE GENERATOR

FIG. 68I




B. FALLING-EDGE PULSE GENERATOR

FIG. 68J

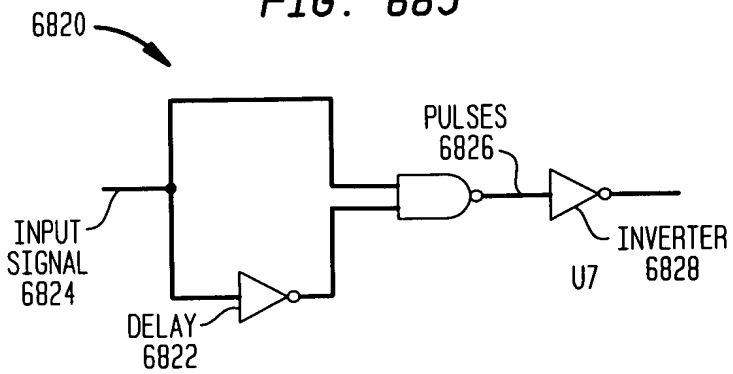


FIG. 68K

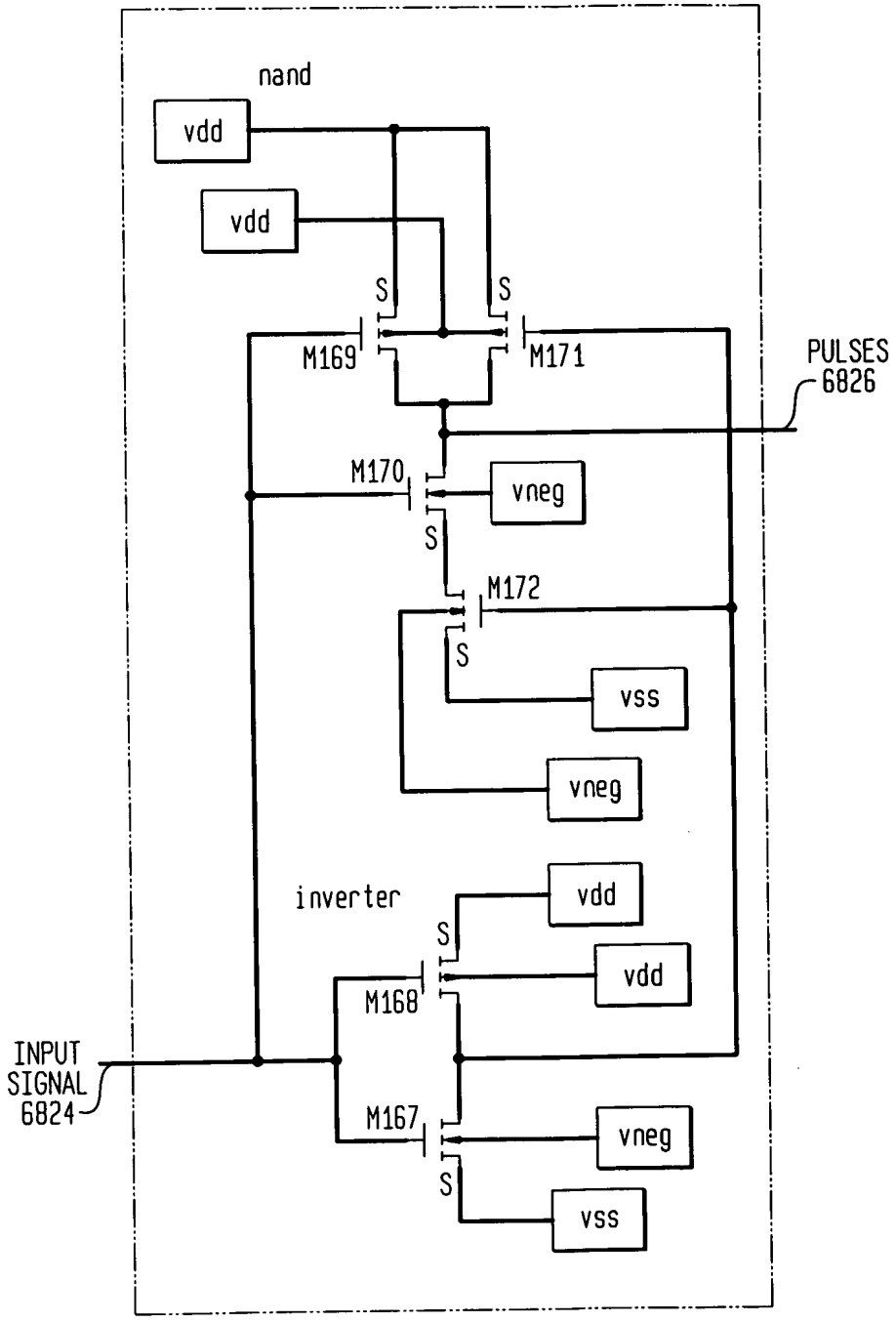



FIG. 68L

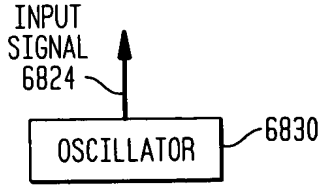


FIG. 69

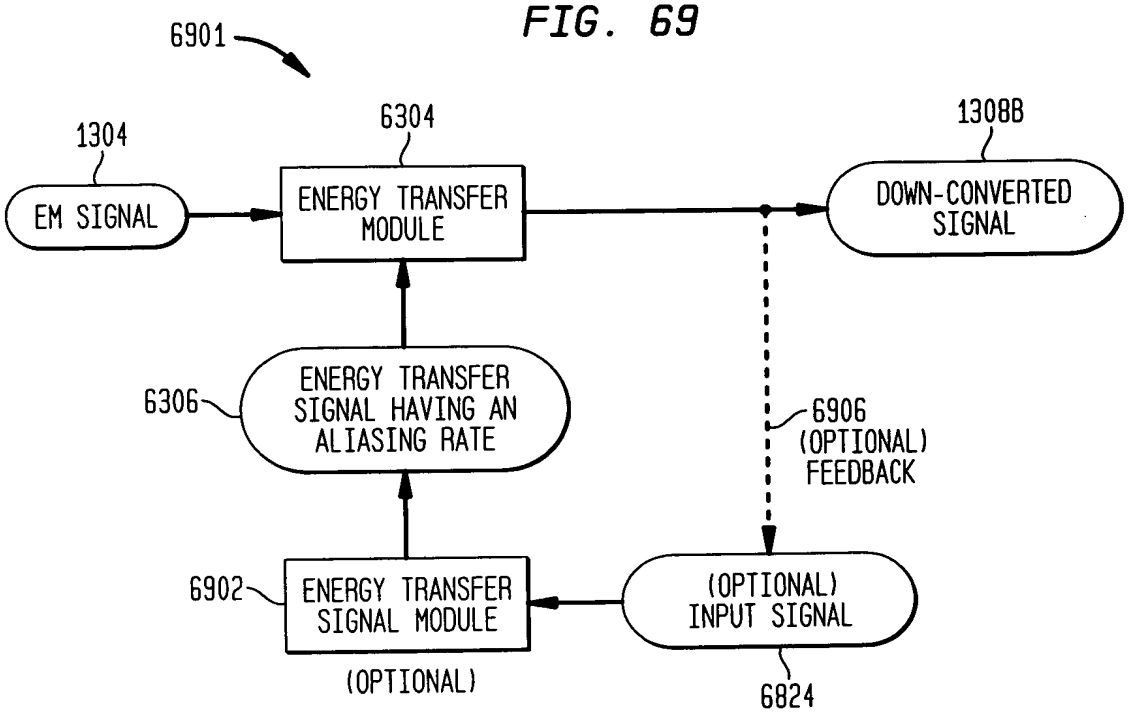

6901
1304
EM SIGNAL
6304
ENERGY TRANSFER MODULE
1308B
DOWN-CONVERTED SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
6906
(OPTIONAL)
FEEDBACK
6902
ENERGY TRANSFER SIGNAL MODULE
(OPTIONAL)
(OPTIONAL) INPUT SIGNAL
6824

FIG. 70

IMPEDANCE MATCHED ALIASING MODULE

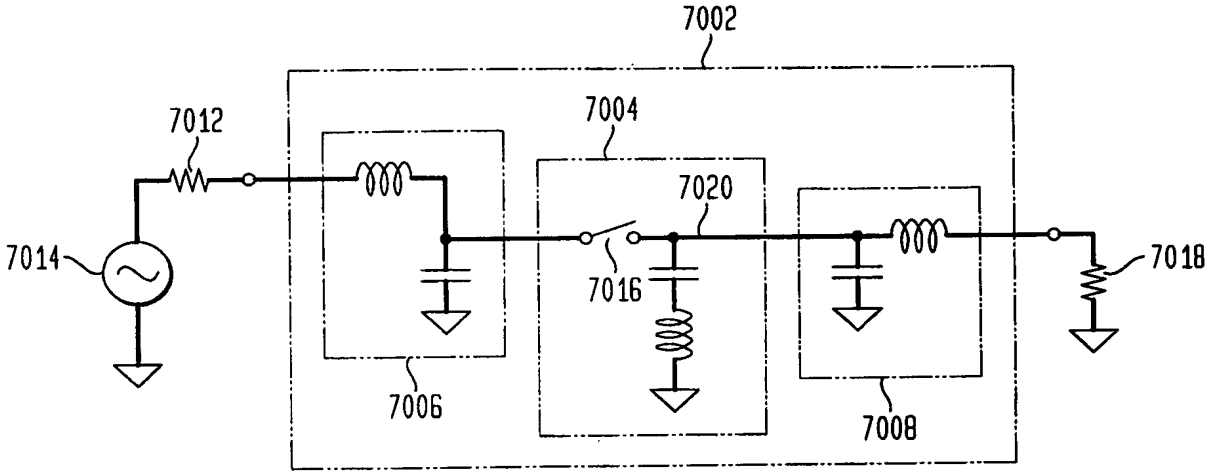
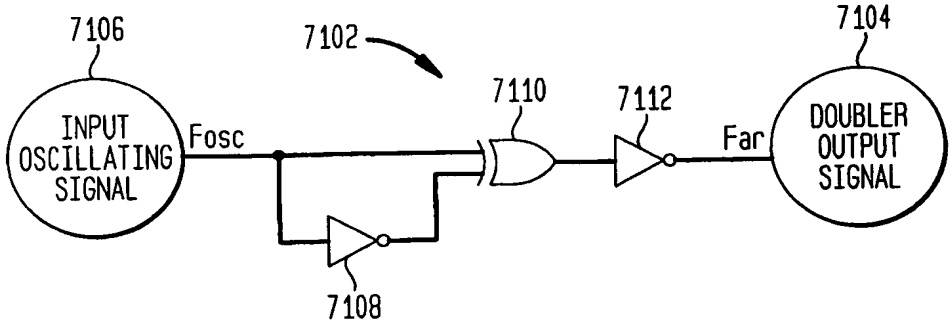



FIG. 71A



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For: Method and System for Down-Converting an
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FIG. 71B

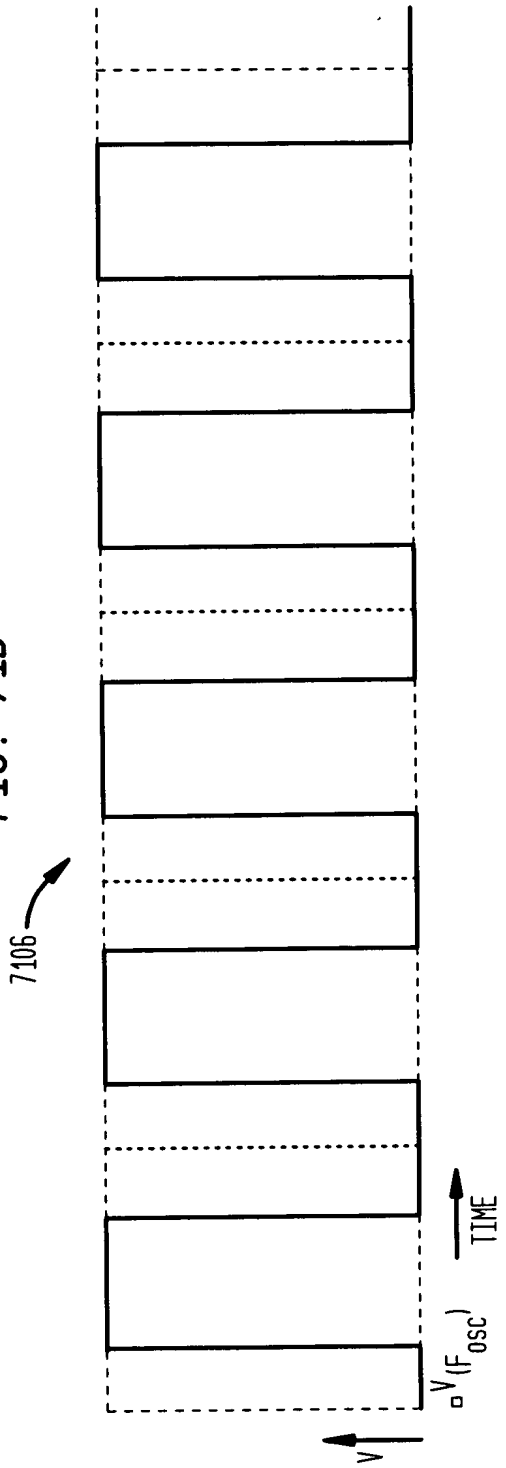


FIG. 71C

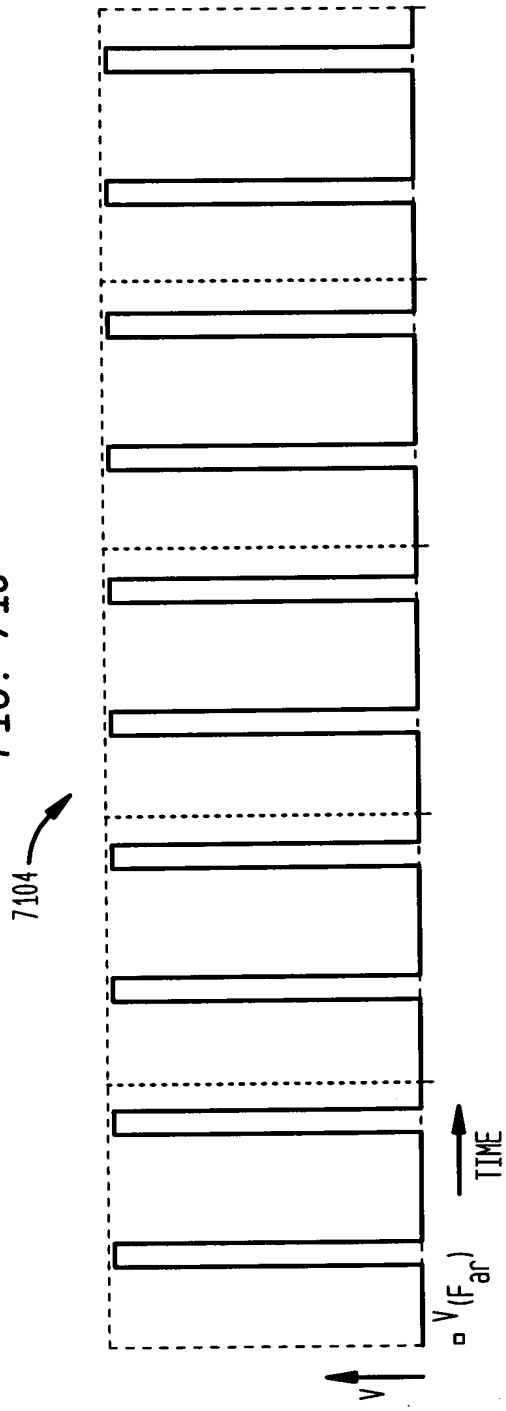

FIG. 72

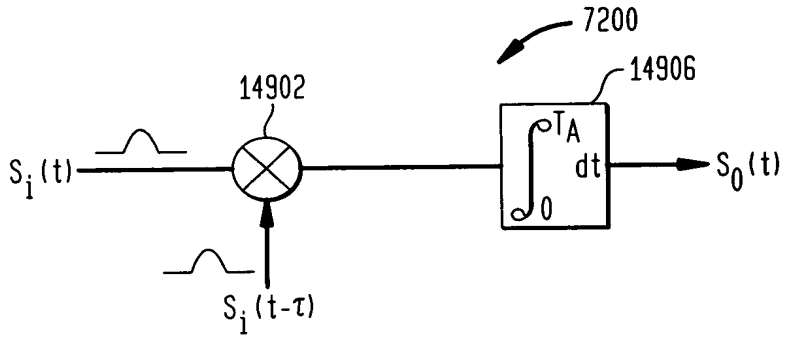

FIG. 73

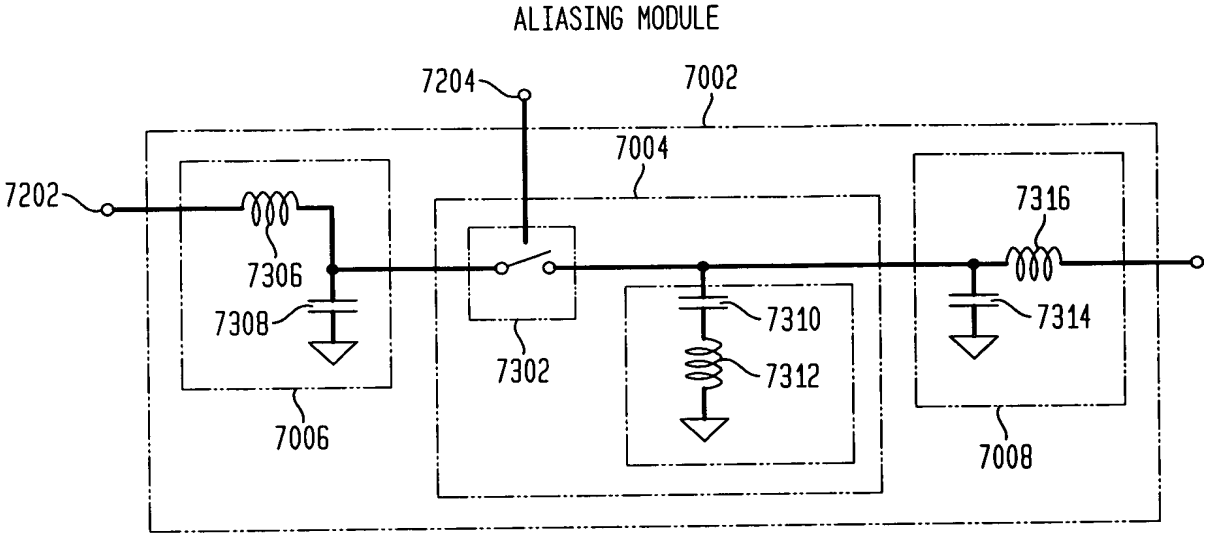
ALIASING MODULE
7204
7002
7004
7202
7306
7308
7006
7302
7310
7312
7316
7314
7008

FIG. 74

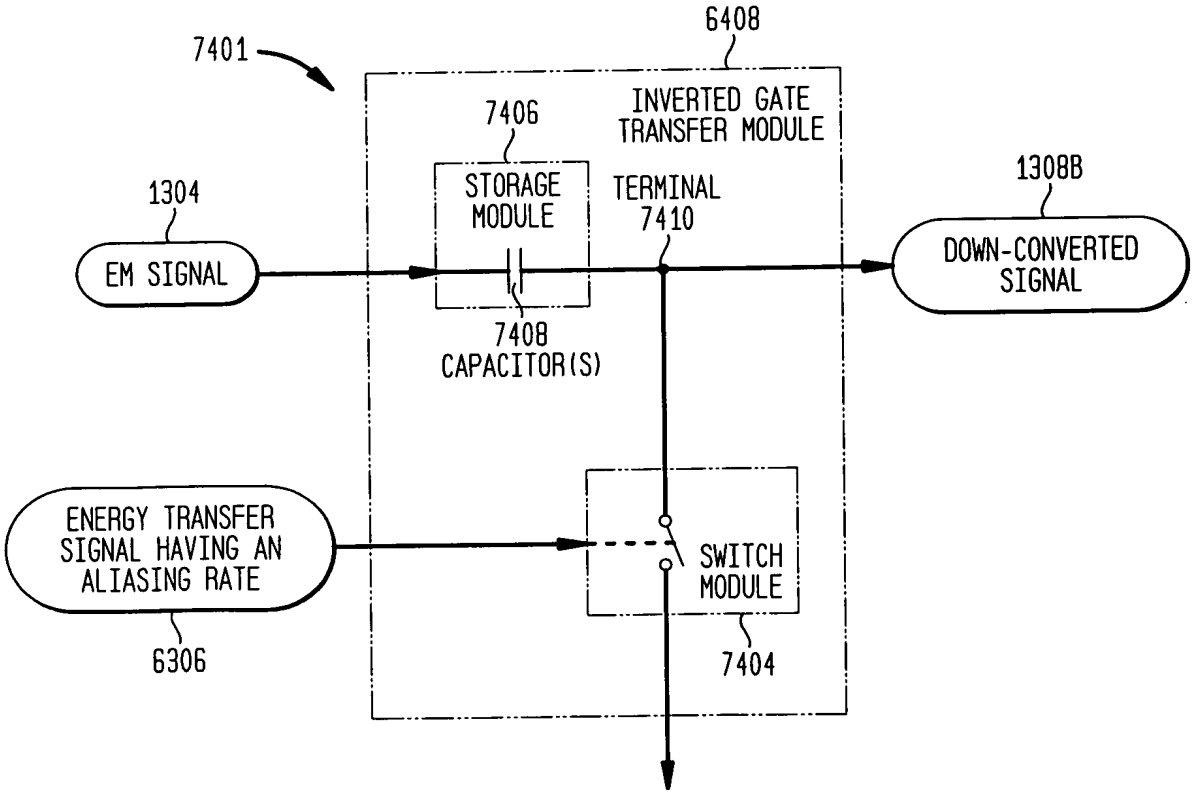
7401
6408
INVERTED GATE
TRANSFER MODULE
7406
STORAGE
MODULE
TERMINAL
7410
1304
EM SIGNAL
1308B
DOWN-CONVERTED
SIGNAL
7408
CAPACITOR(S)
ENERGY TRANSFER
SIGNAL HAVING AN
ALIASING RATE
SWITCH
MODULE
6306
7404

FIG. 75A

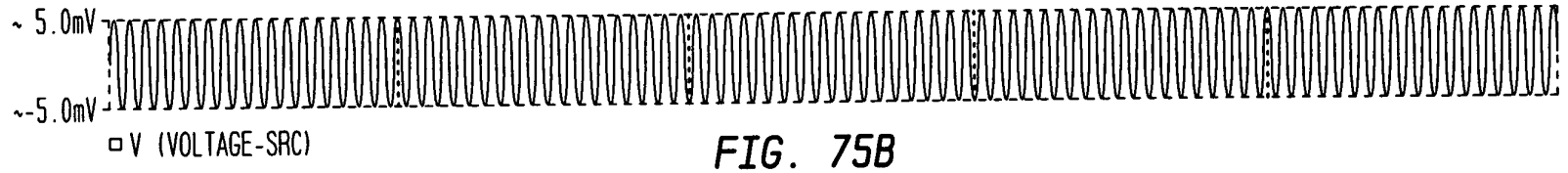


FIG. 75B

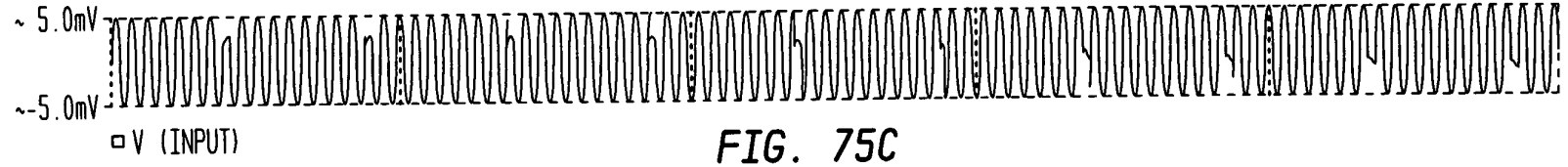


FIG. 75C


FIG. 75D

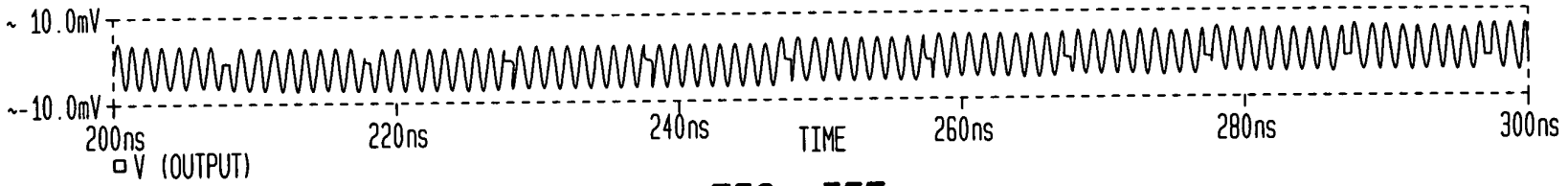


FIG. 75E

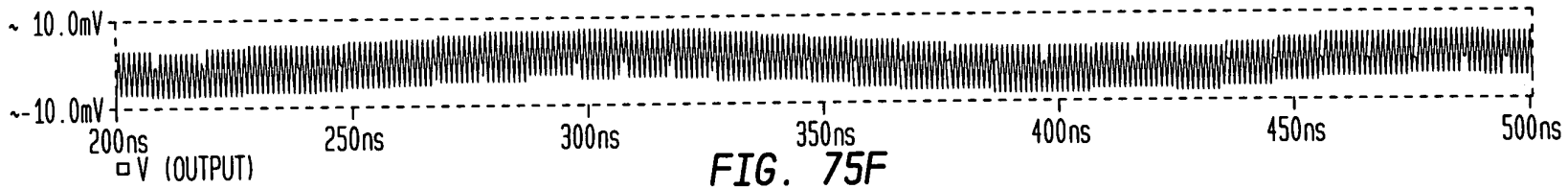


FIG. 75F

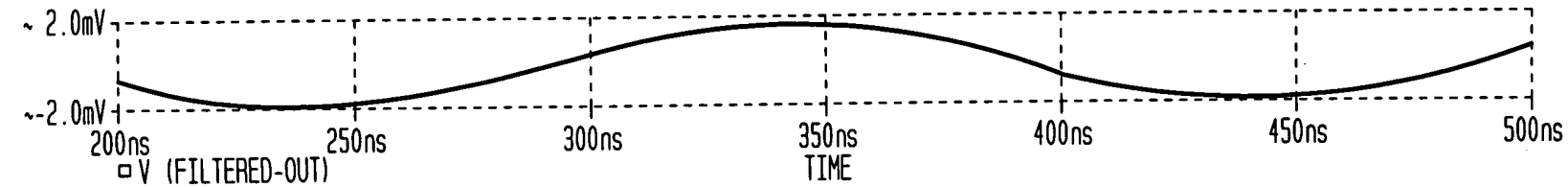

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FIG. 76A

DIFFERENTIAL ENERGY TRANSFER CONFIGURATION

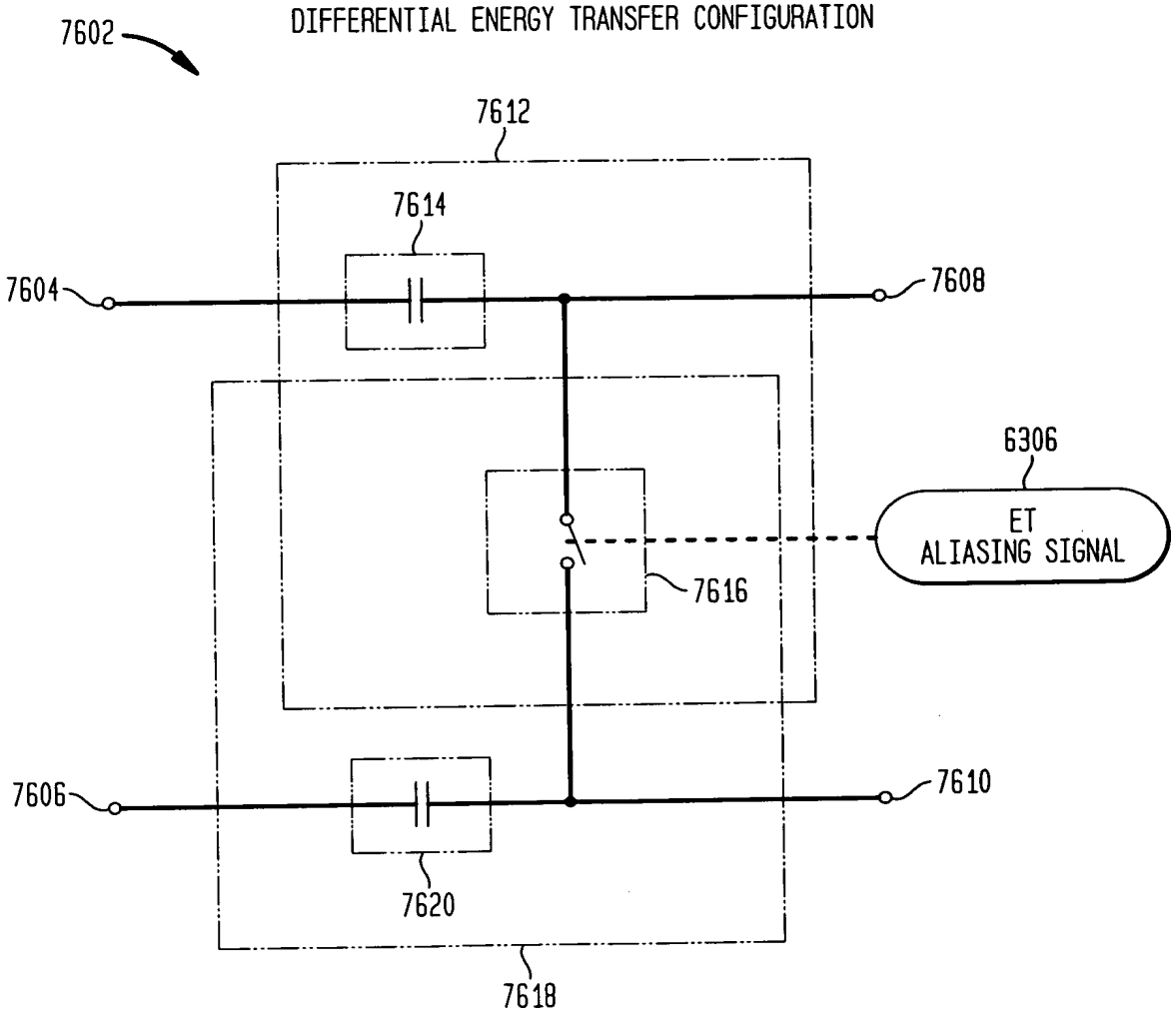

FIG. 76B

DIFFERENTIAL INPUT TO DIFFERENTIAL OUTPUT

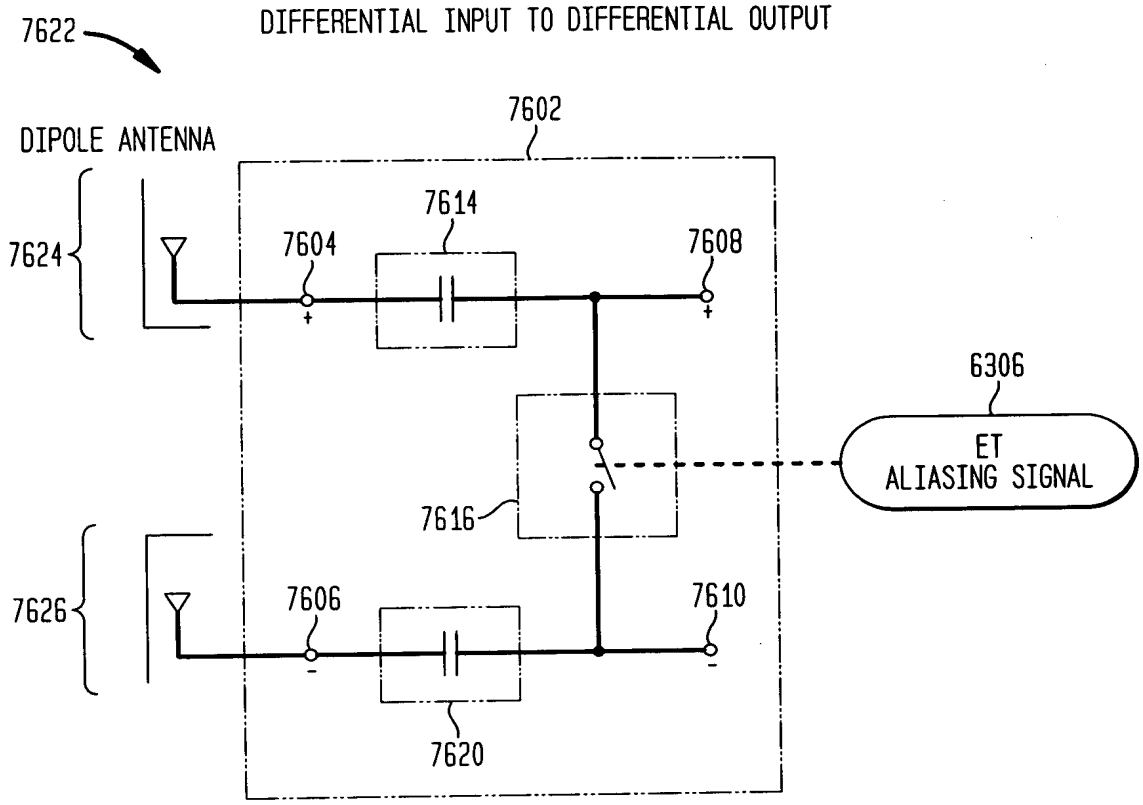


FIG. 76C

SINGLE INPUT TO DIFFERENTIAL OUTPUT

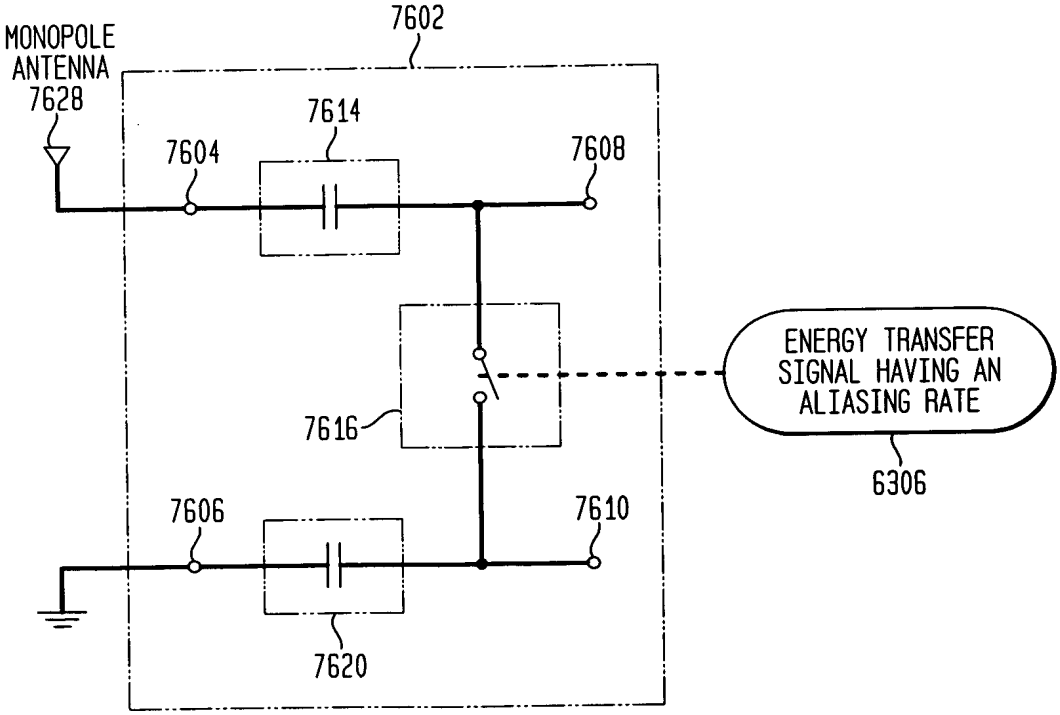

*FIG. 76D*

DIFFERENTIAL INPUT TO SINGLE OUTPUT

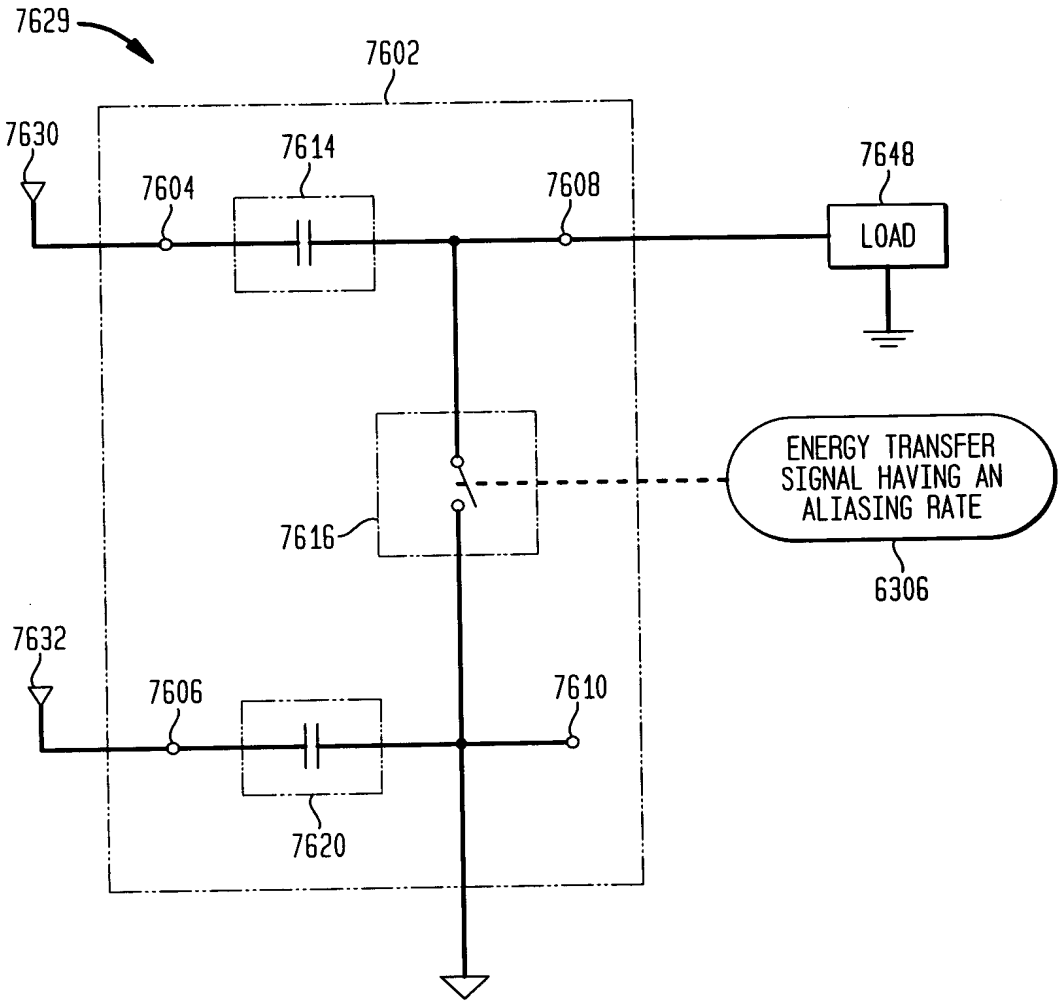

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*FIG. 76E*

EXAMPLE INPUT/OUTPUT CIRCUITRY

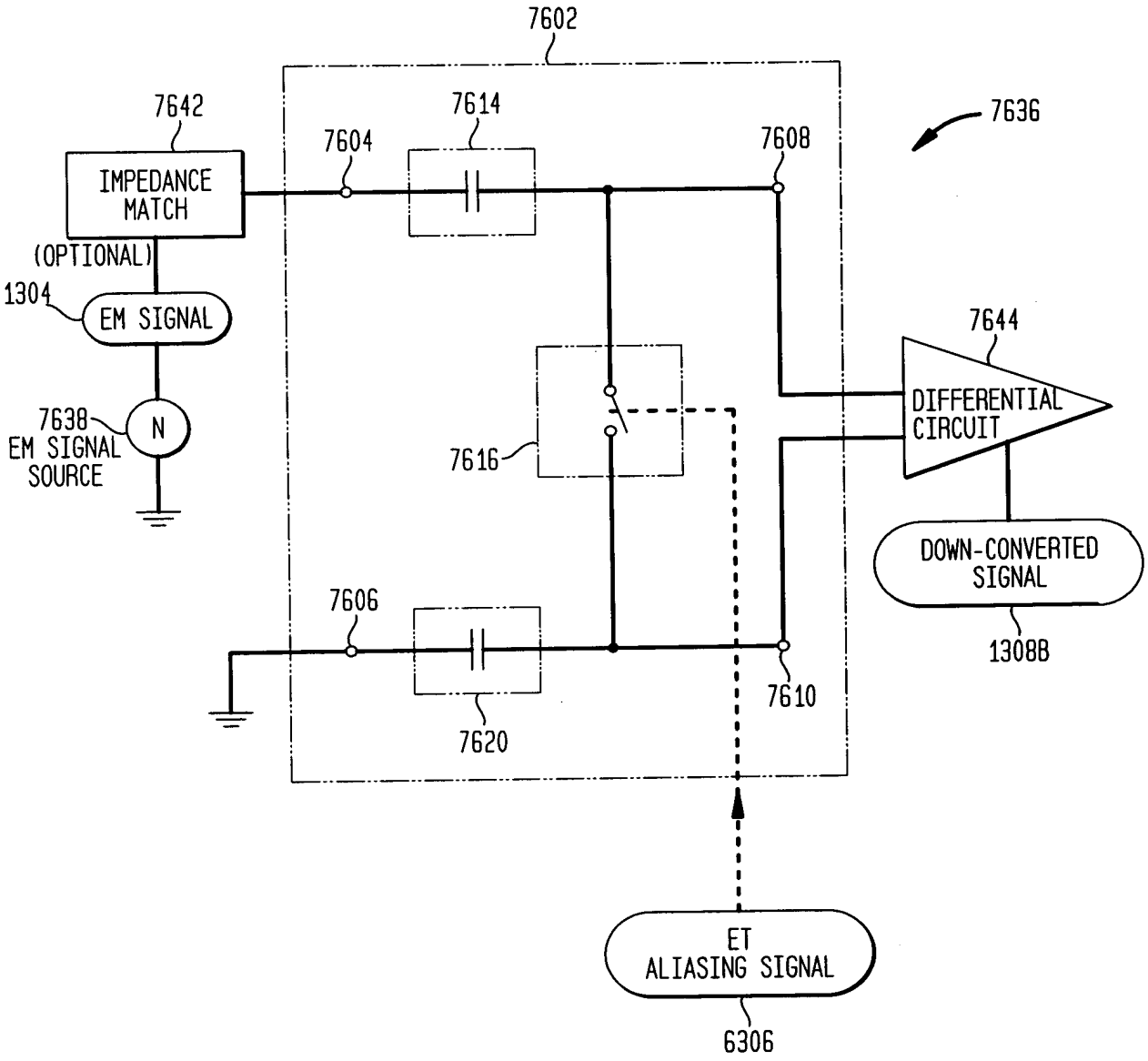

FIG. 77A

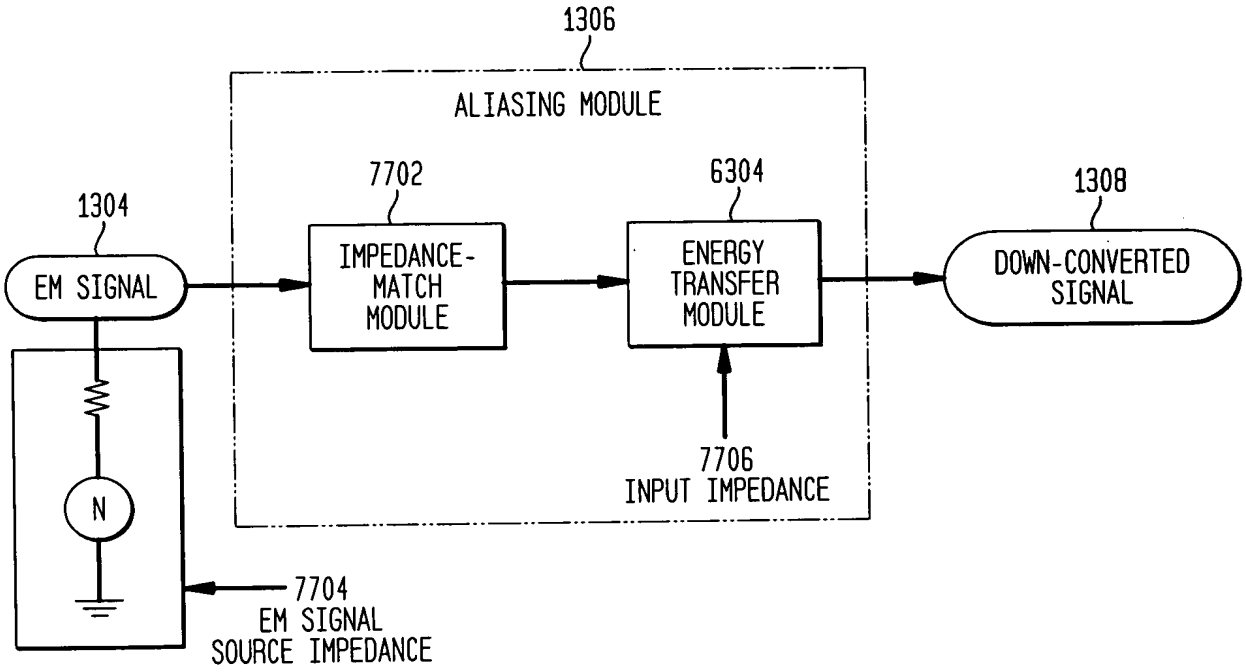


FIG. 77B

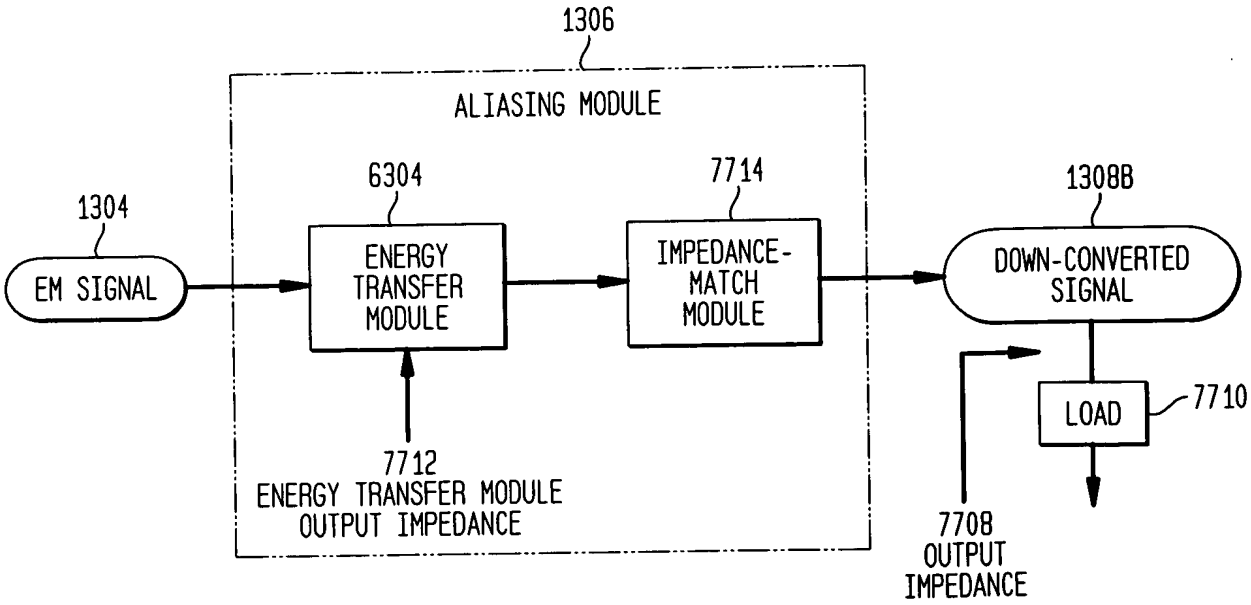

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FIG. 77C

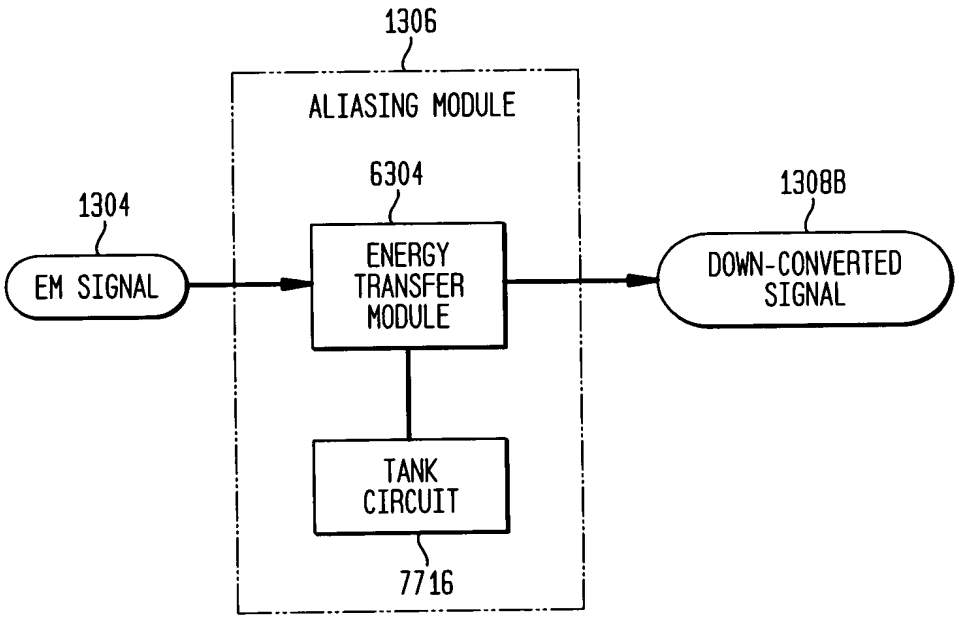


FIG. 78A

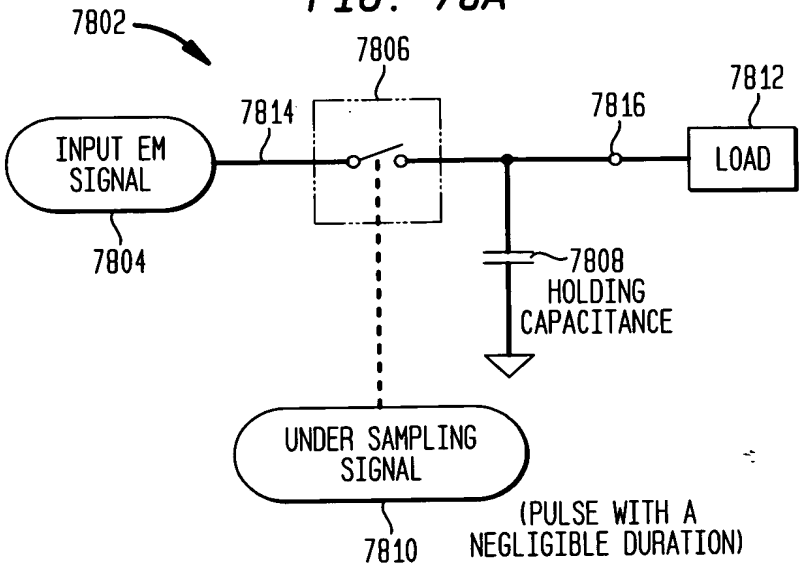



FIG. 78B

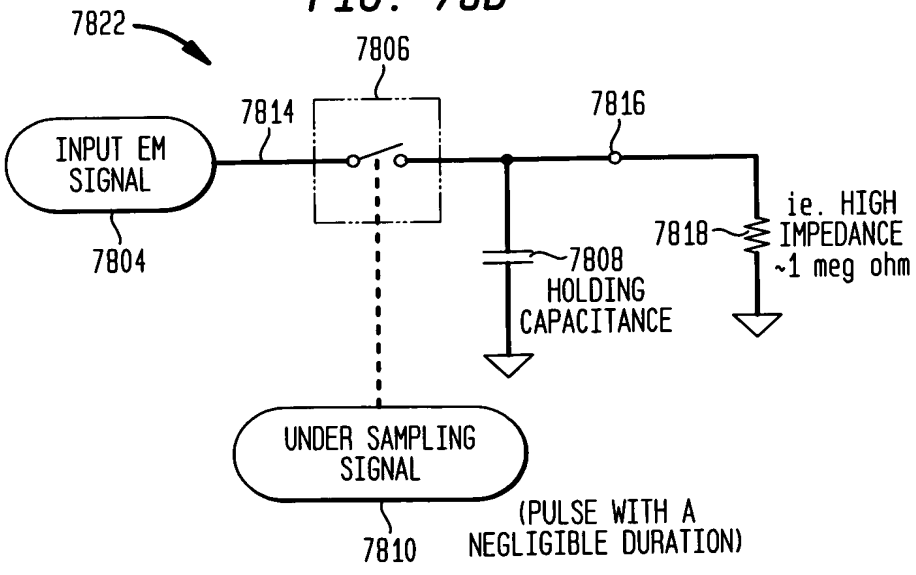


FIG. 79A

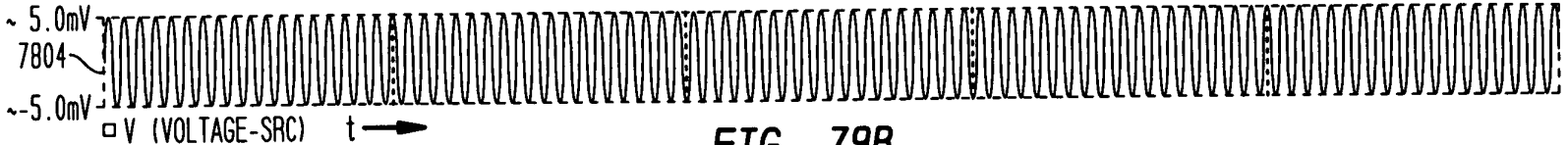



FIG. 79B

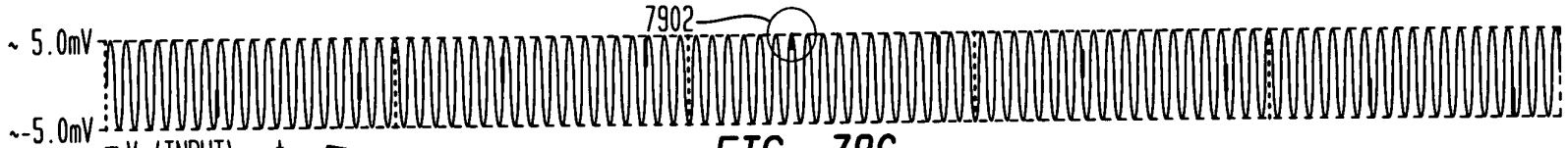



FIG. 79C

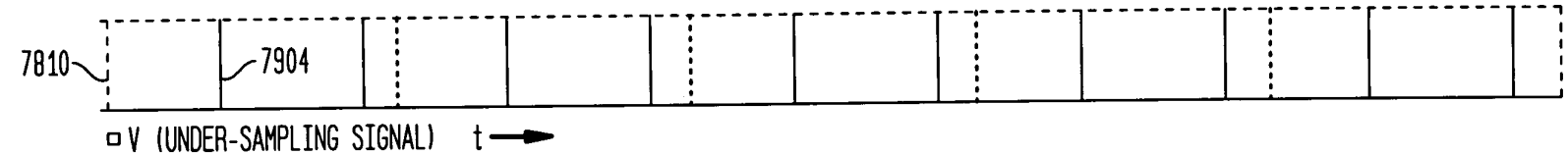



FIG. 79D

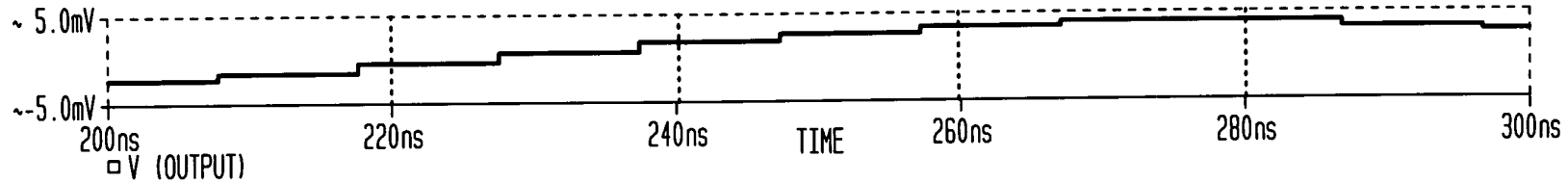



FIG. 79E

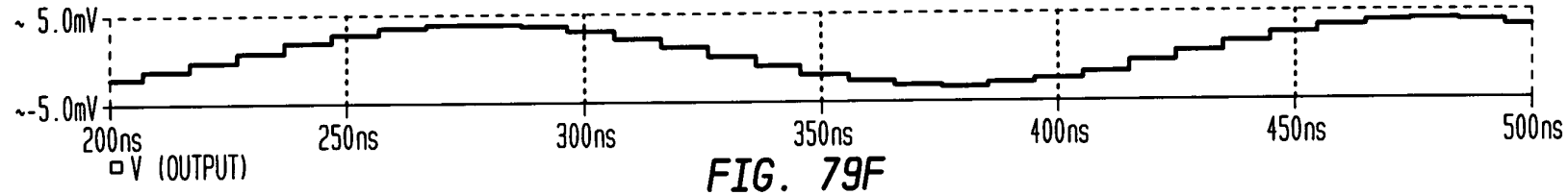
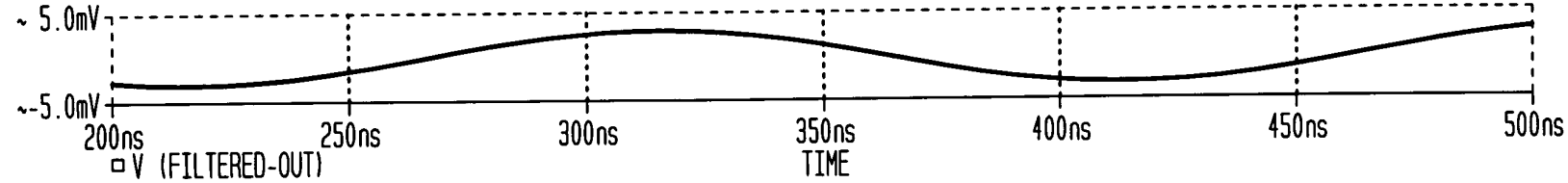



FIG. 79F

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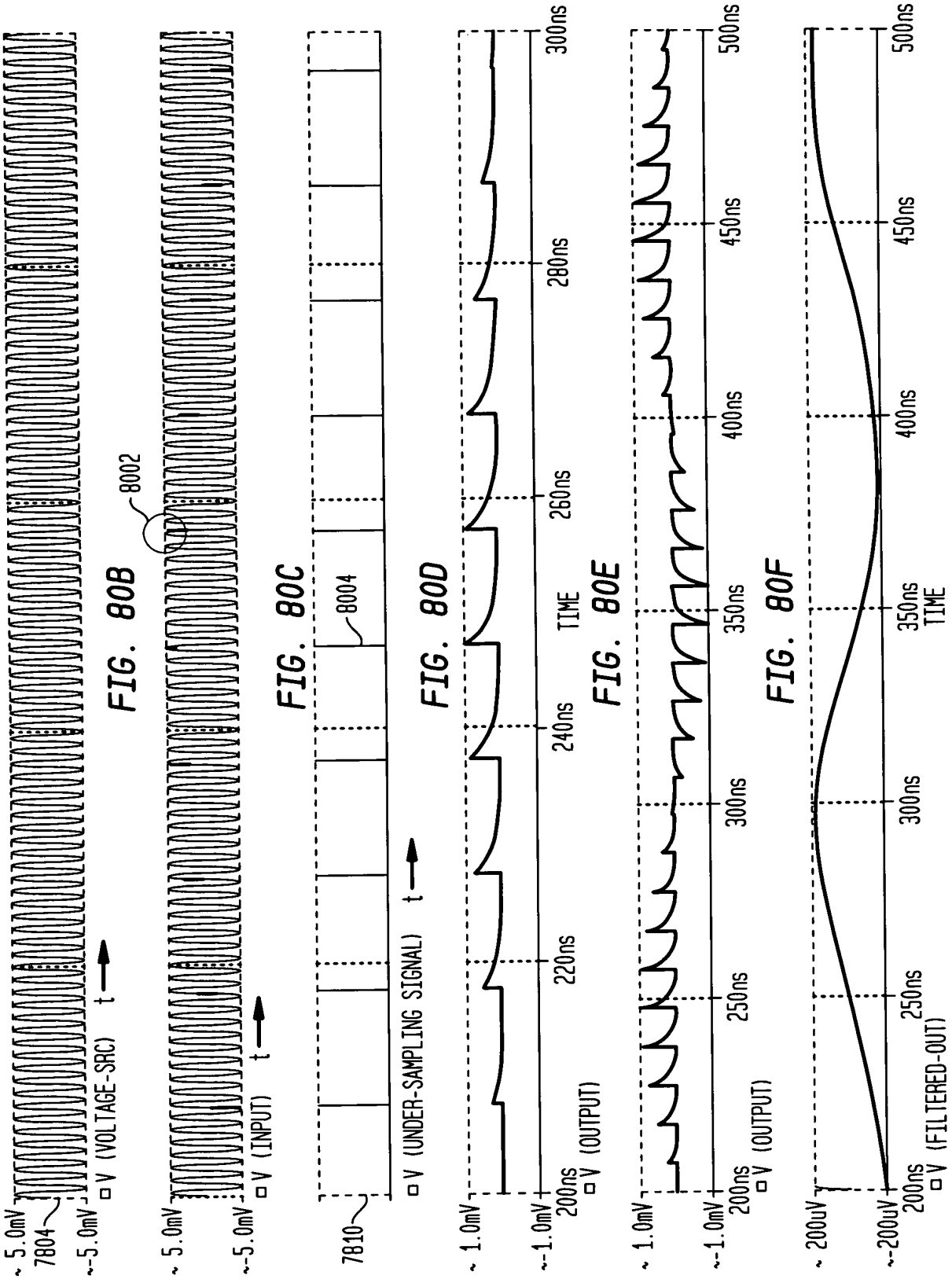
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same


~ 5.0mV
7804
~-5.0mV
V (VOLTAGE-SRC)
t
FIG. 80A
~ 5.0mV
8002
~-5.0mV
V (INPUT)
t
FIG. 80B
7810
8004
V (UNDER-SAMPLING SIGNAL)
t
FIG. 80C
~ 1.0mV
~-1.0mV
200ns
220ns
240ns
260ns
280ns
300ns
V (OUTPUT)
TIME
FIG. 80D
~ 1.0mV
~-1.0mV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
V (OUTPUT)
FIG. 80E
~ 200uV
~-200uV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
V (FILTERED-OUT)
TIME
FIG. 80F

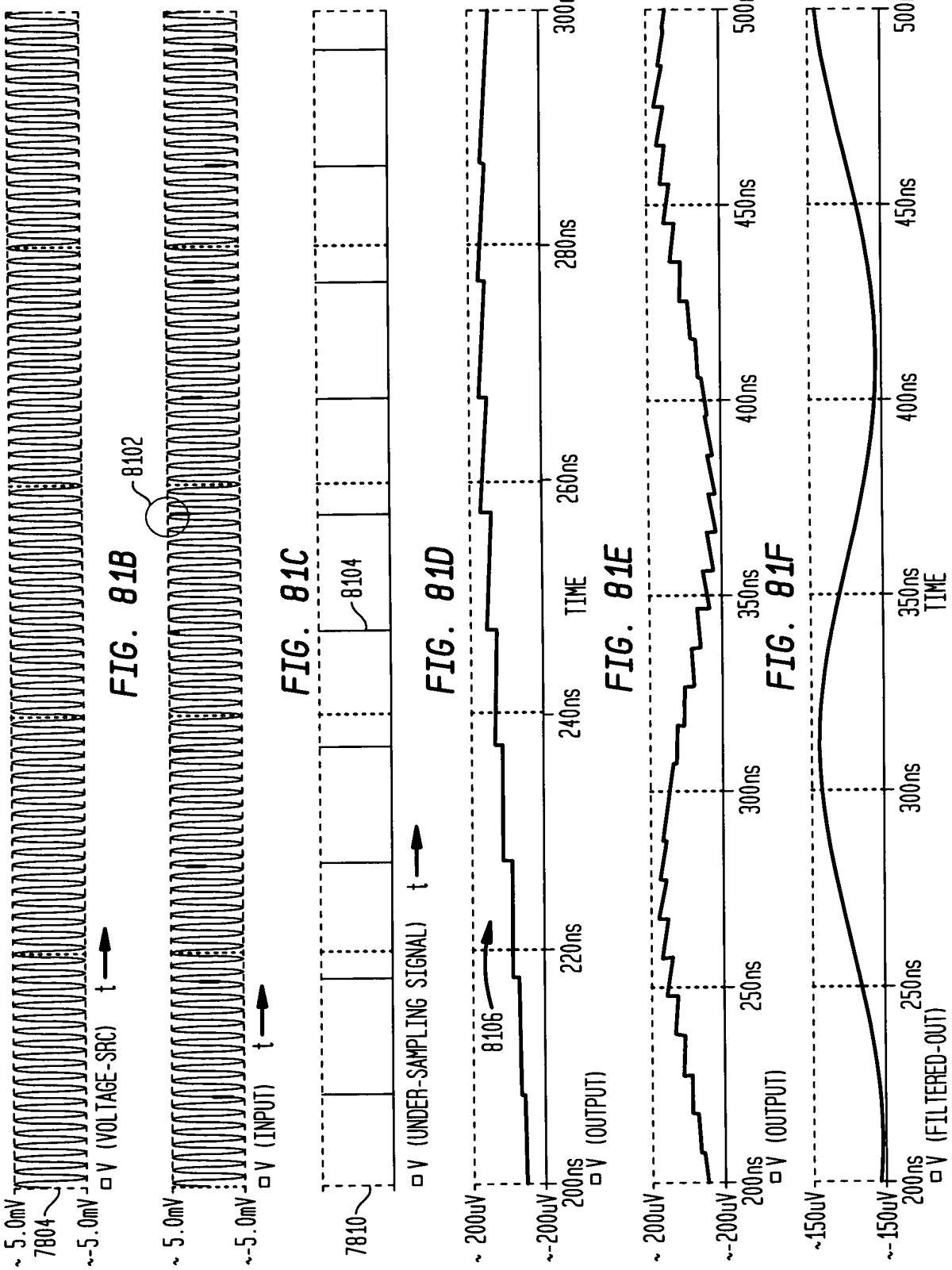

~ 5.0mV
7804
~-5.0mV
V (VOLTAGE-SRC)
t
FIG. 81A
~ 5.0mV
~-5.0mV
V (INPUT)
t
8102
FIG. 81B
7810
8104
V (UNDER-SAMPLING SIGNAL)
t
FIG. 81C
~ 200uV
~-200uV
200ns
V (OUTPUT)
8106
220ns
240ns
260ns
280ns
300ns
TIME
FIG. 81D
~ 200uV
~-200uV
200ns
V (OUTPUT)
250ns
300ns
350ns
400ns
450ns
500ns
FIG. 81E
~150uV
~-150uV
200ns
V (FILTERED-OUT)
250ns
300ns
350ns
400ns
450ns
500ns
TIME
FIG. 81F

FIG. 82A

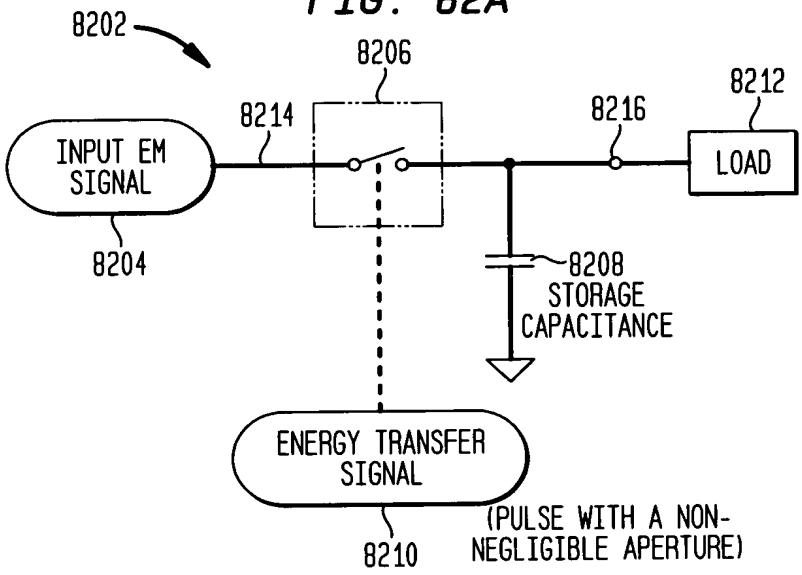



FIG. 82B

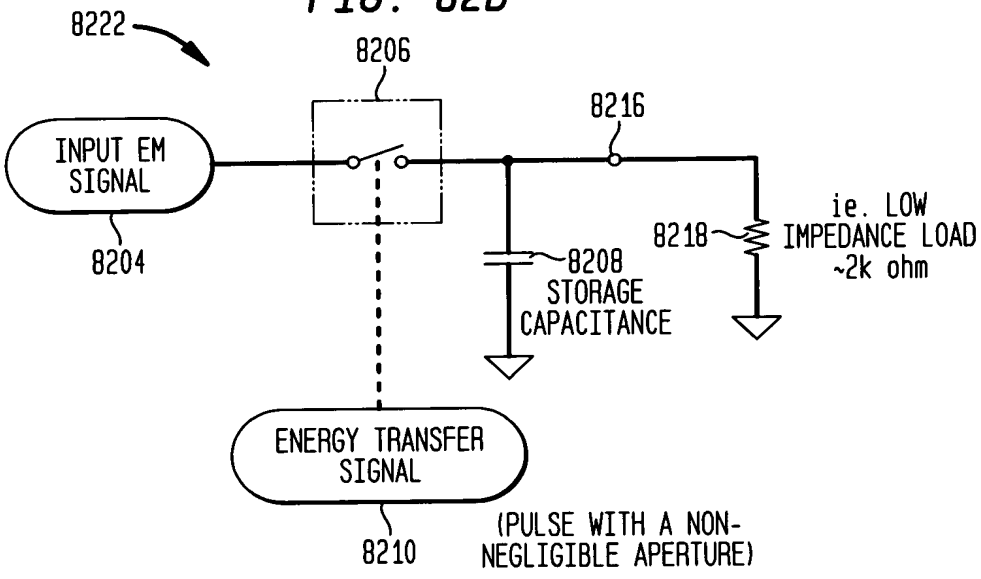


FIG. 83A


FIG. 83B

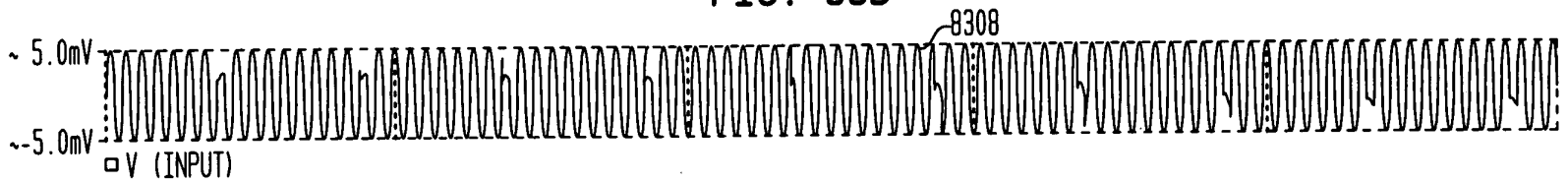



FIG. 83C

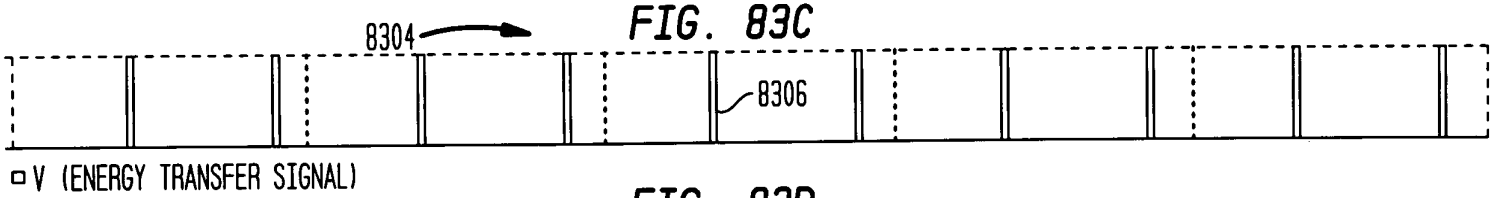



FIG. 83D

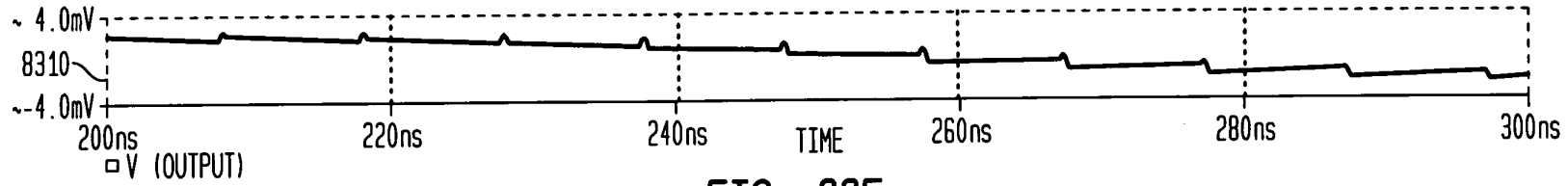



FIG. 83E

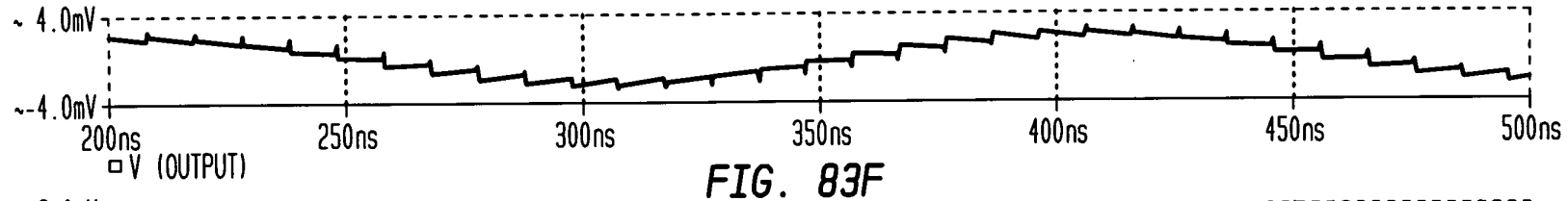
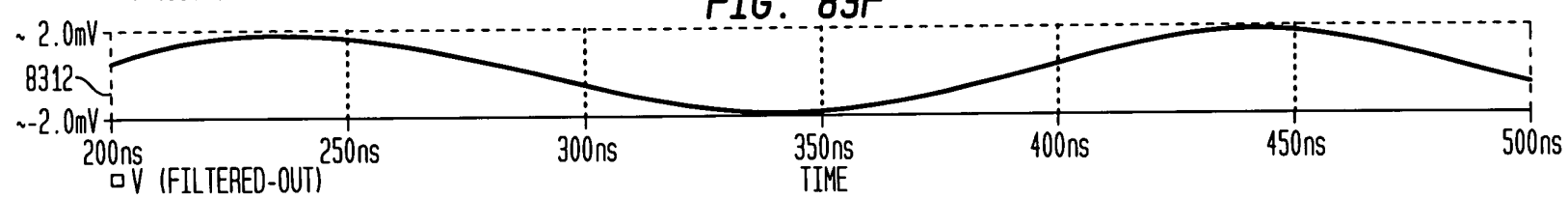



FIG. 83F

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Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.092000I; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

Replacement Sheet
Sheet 103 of 284
Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 84A

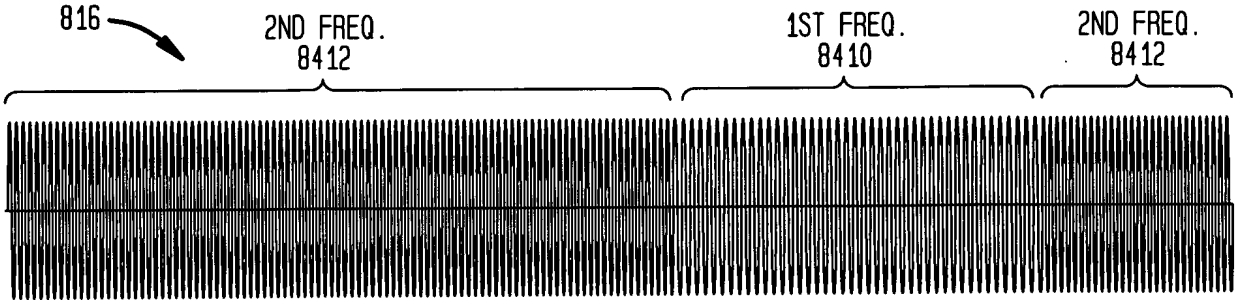
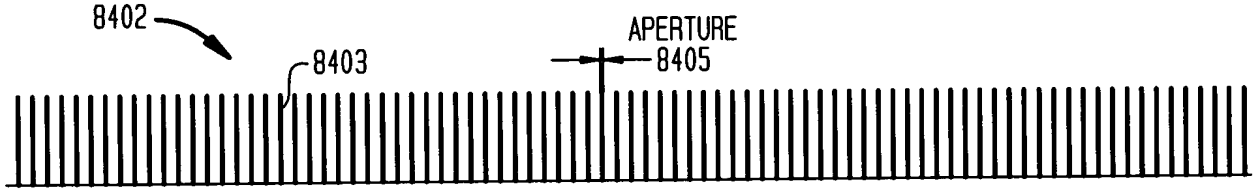



FIG. 84B



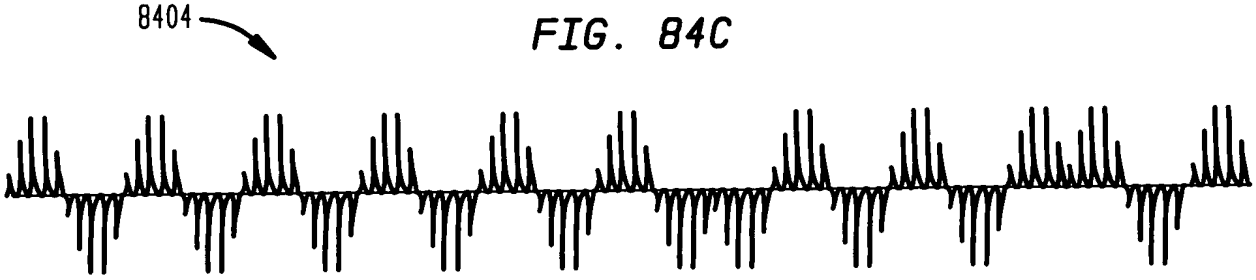




FIG. 84C

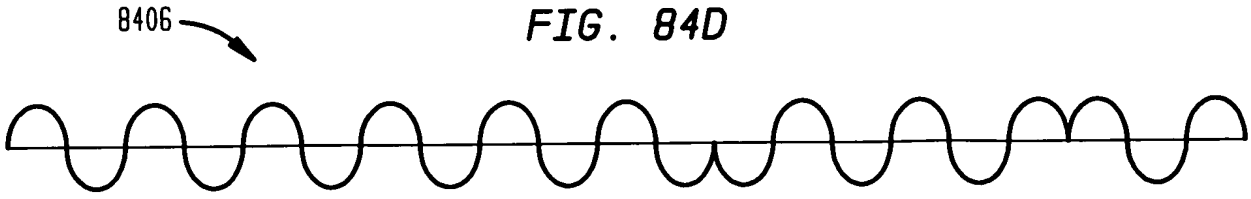
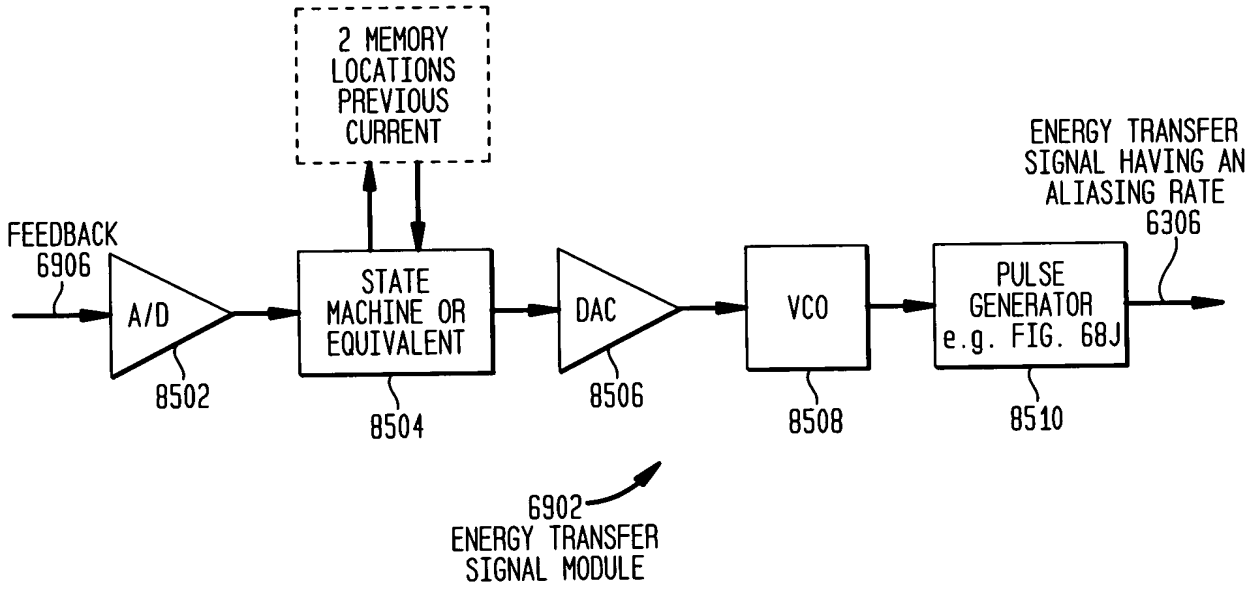



FIG. 84D

FIG. 85A


2 MEMORY LOCATIONS PREVIOUS CURRENT
FEEDBACK 6906
A/D
8502
STATE MACHINE OR EQUIVALENT
8504
DAC
8506
VCO
8508
PULSE GENERATOR e.g. FIG. 68J
8510
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE 6306
6902
ENERGY TRANSFER SIGNAL MODULE

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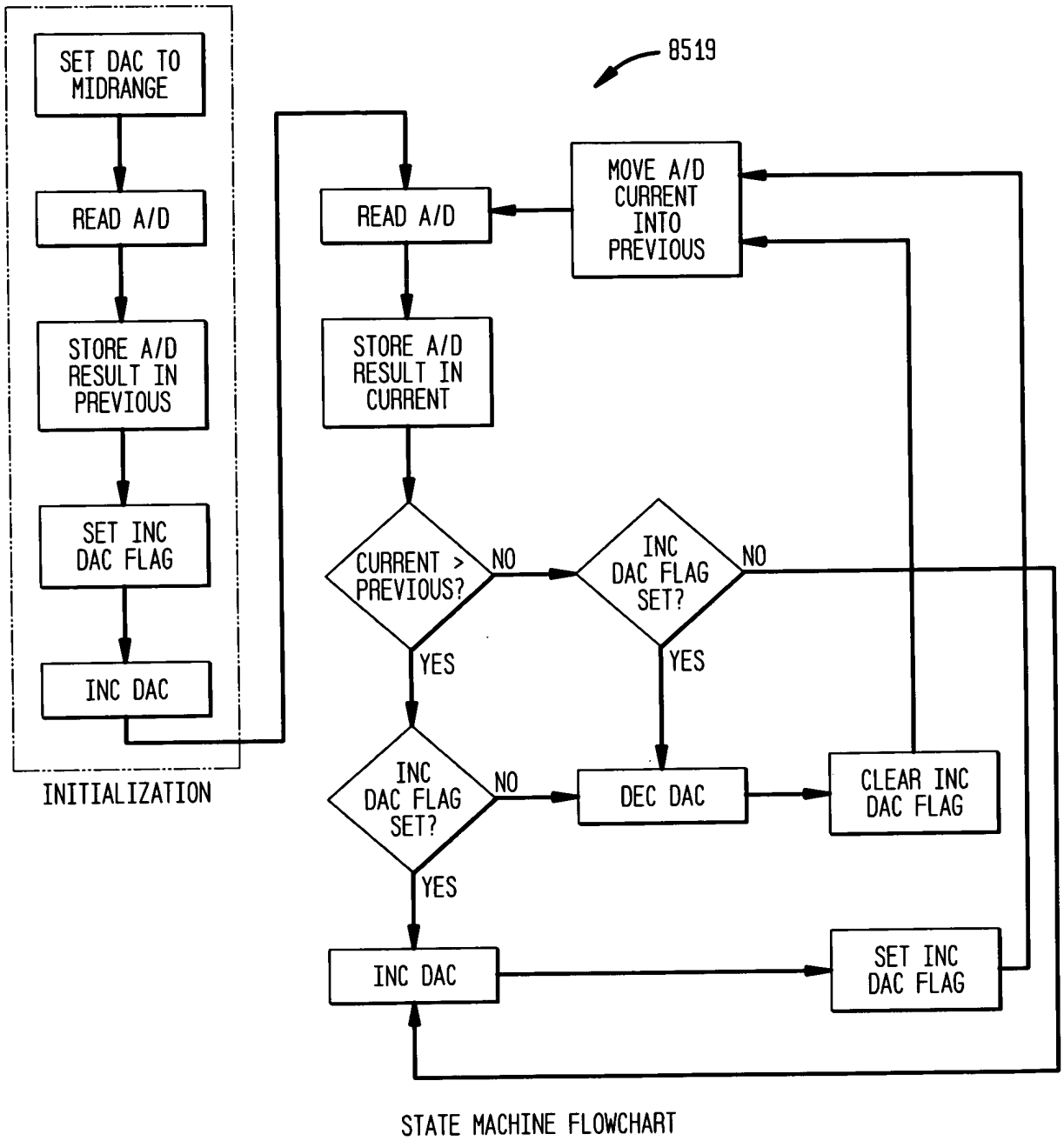
Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

FIG. 85B



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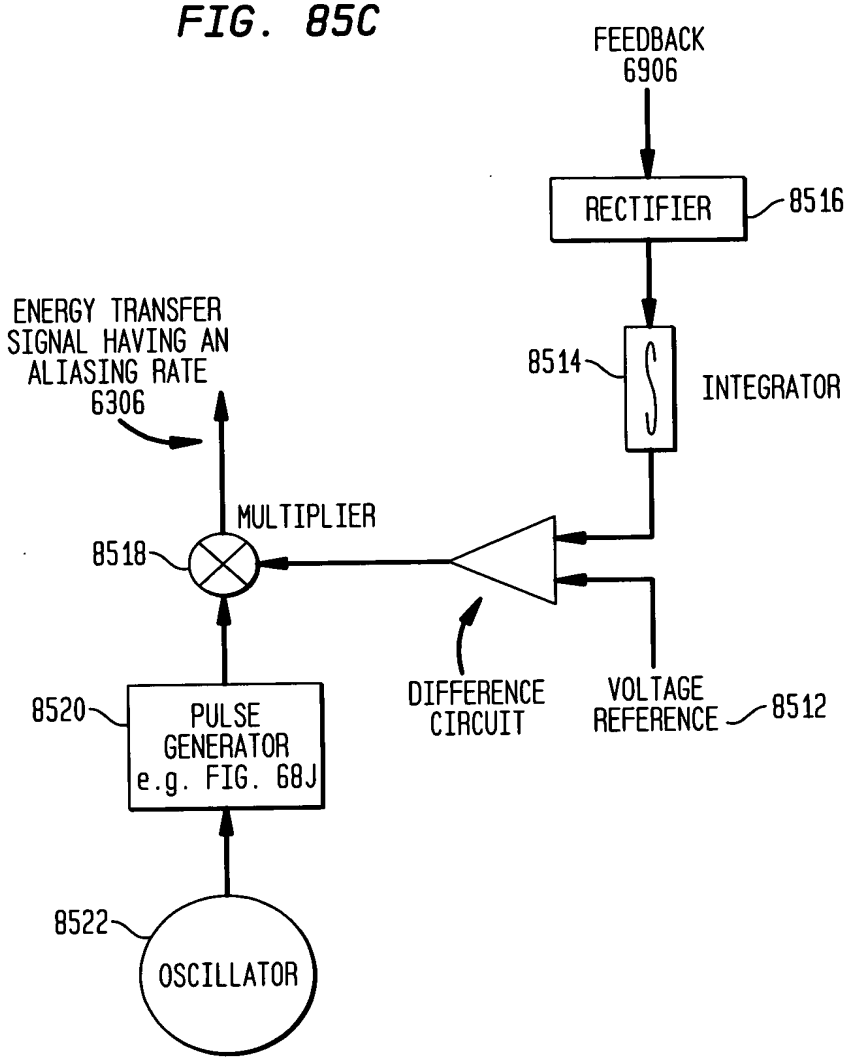
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

FIG. 85C




ENERGY TRANSFER SIGNAL MODULE 6902

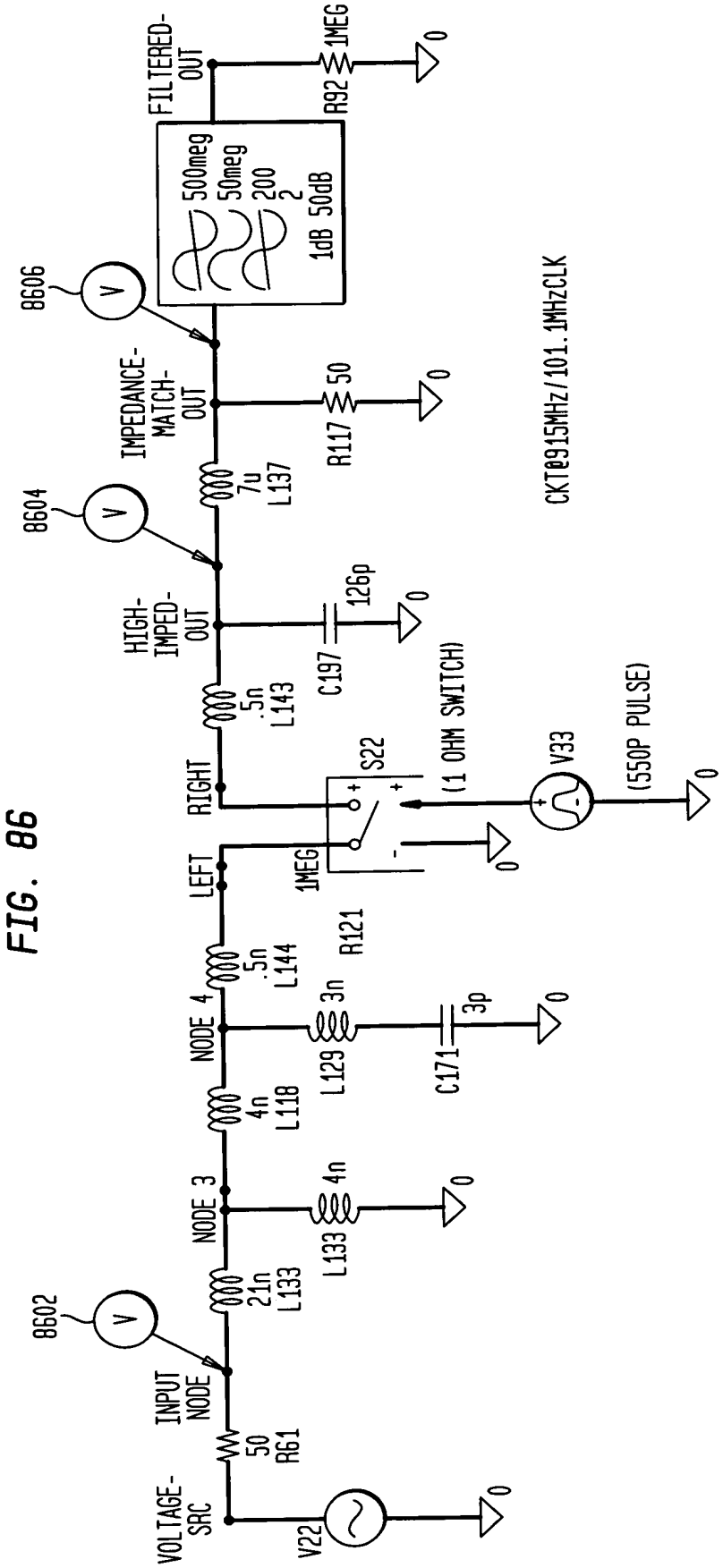
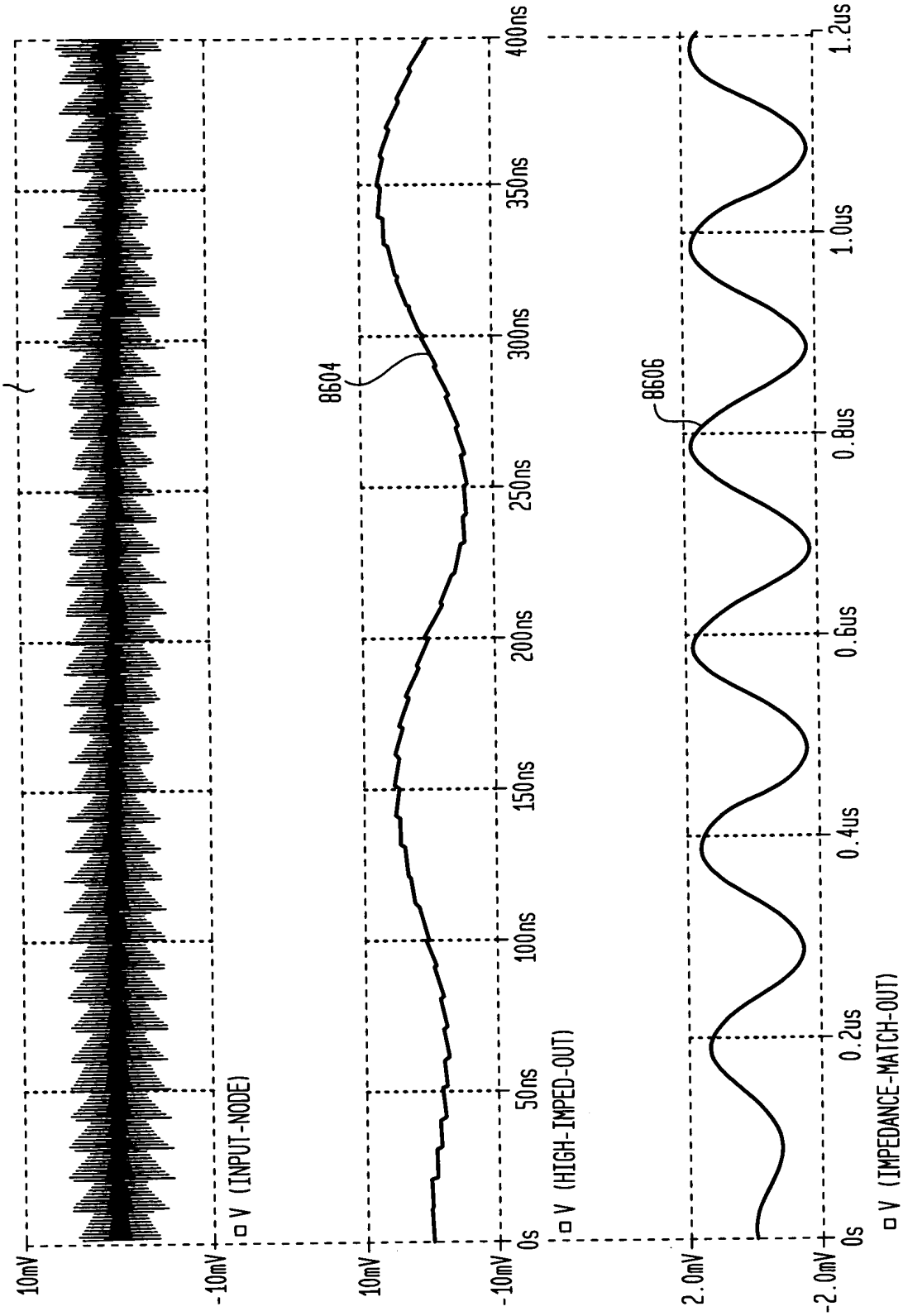

FILTERED-OUT
R92
1MEG
0
500meg
50meg
200
2
1dB 50dB
8606
IMPEDANCE-MATCH-OUT
R117
50
8604
7u
L137
HIGH-IMPED-OUT
C197
126p
.5n
L143
RIGHT
S22
(1 OHM SWITCH)
V33
(550P PULSE)
CKT@915MHz/101.1MHzCLK
LEFT
1MEG
R121
.5n
L144
NODE 4
3n
L129
C171
3p
4n
L118
NODE 3
4n
L133
8602
21n
L133
INPUT NODE
50
R61
VOLTAGE-SRC
V22

FIG. 86

FIG. 87


8602
8604
8606
10mV
-10mV
10mV
-10mV
2.0mV
-2.0mV
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
V (INPUT-NODE)
V (HIGH-IMPED-OUT)
V (IMPEDANCE-MATCH-OUT)

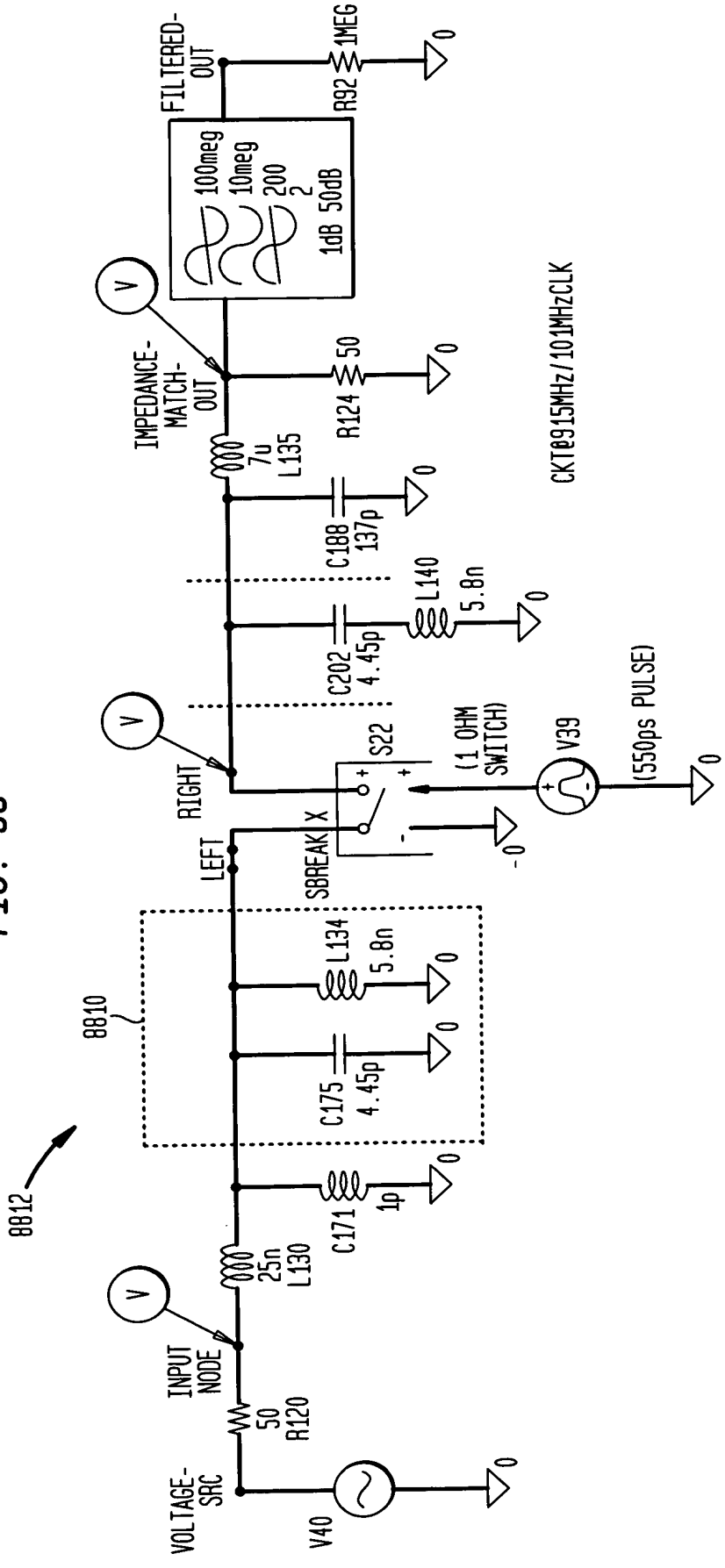

FILTERED-OUT
R92
1MEG
100meg
10meg
200
2
1dB 50dB
IMPEDANCE-MATCH-OUT
R124
50
7u
L135
C188
137p
L140
5.8n
C202
4.45p
RIGHT
S22
(1 OHM SWITCH)
V39
(550ps PULSE)
CKT@915MHz/101MHzCLK
LEFT
SBREAK
X
8810
L134
5.8n
C175
4.45p
8812
C171
1p
25n
L130
INPUT NODE
50
R120
VOLTAGE-SRC
V40
0

FIG. 88

FIG. 89

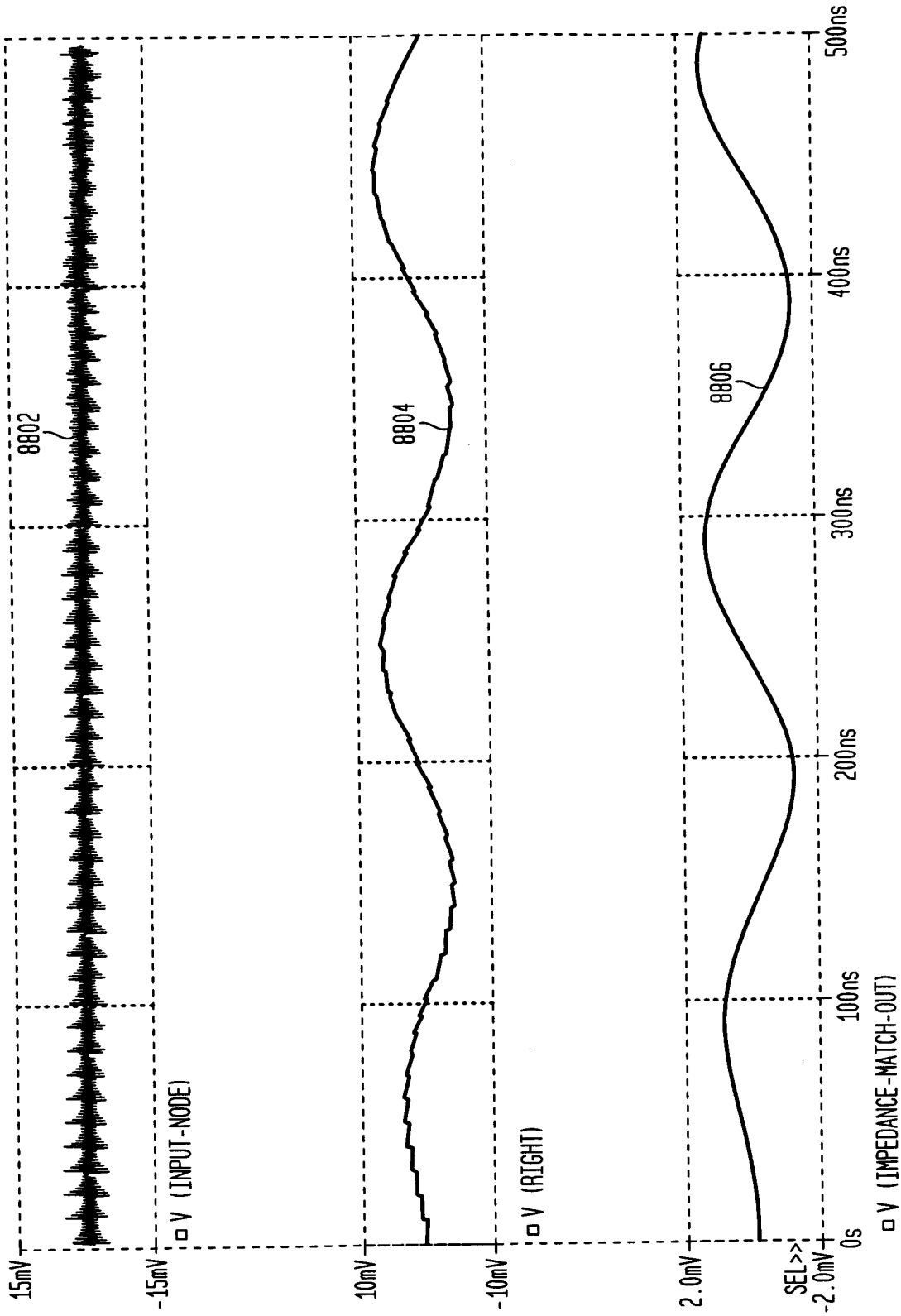
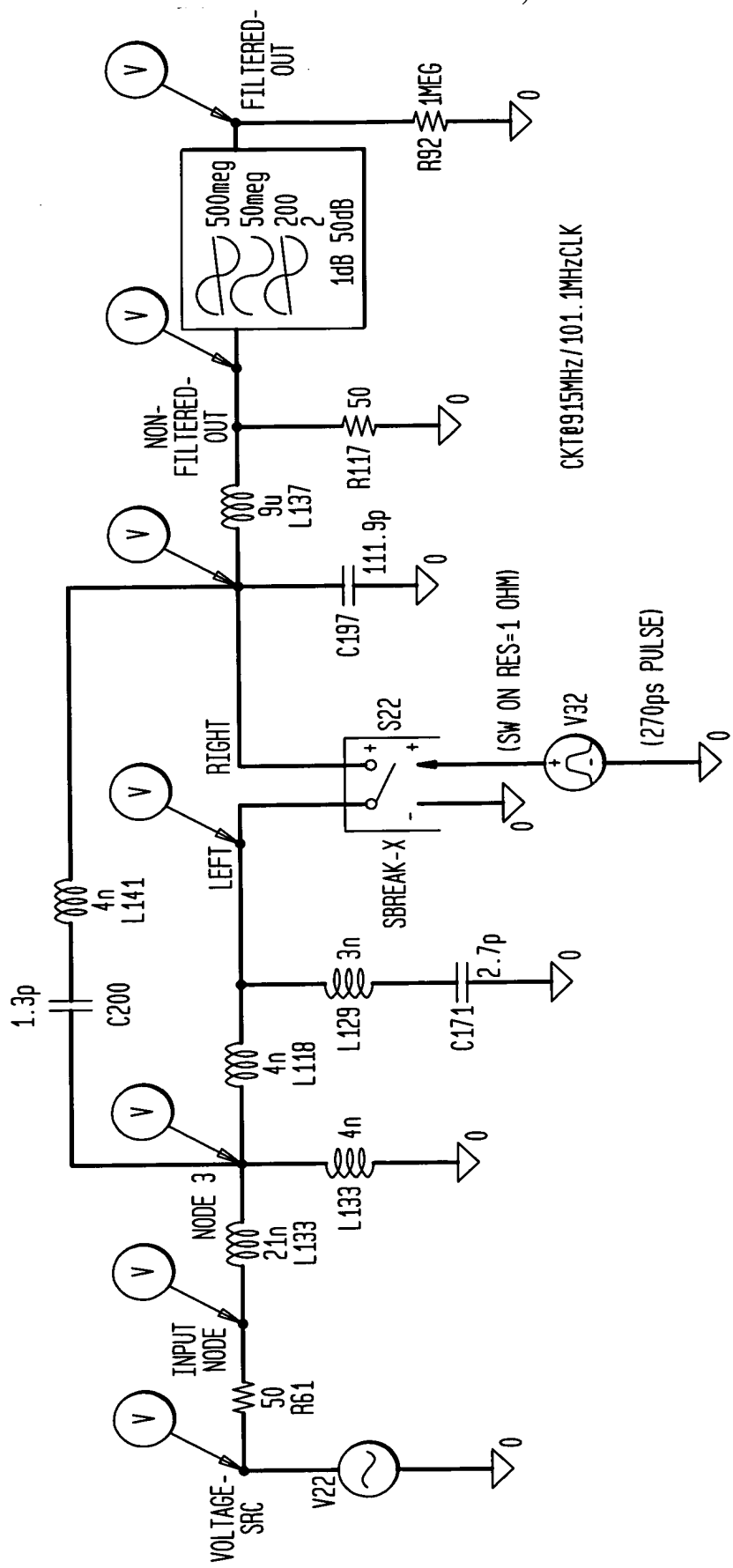

8802
8804
8806
15mV
-15mV
10mV
-10mV
2.0mV
SEL>>
-2.0mV
0s
100ns
200ns
300ns
400ns
500ns
V (INPUT-NODE)
V (RIGHT)
V (IMPEDANCE-MATCH-OUT)

FIG. 90


FILTERED-OUT
R92
1MEG
500meg
50meg
200
2
1dB 50dB
NON-FILTERED-OUT
R117
50
9u
L137
111.9p
C197
CKT@915MHz/101.1MHzCLK
RIGHT
S22
(SW ON RES=1 OHM)
V32
(270ps PULSE)
LEFT
SBREAK-X
4n
L141
1.3p
C200
3n
L129
2.7p
C171
4n
L118
4n
L133
NODE 3
21n
L133
INPUT NODE
50
R61
VOLTAGE-SRC
V22
0

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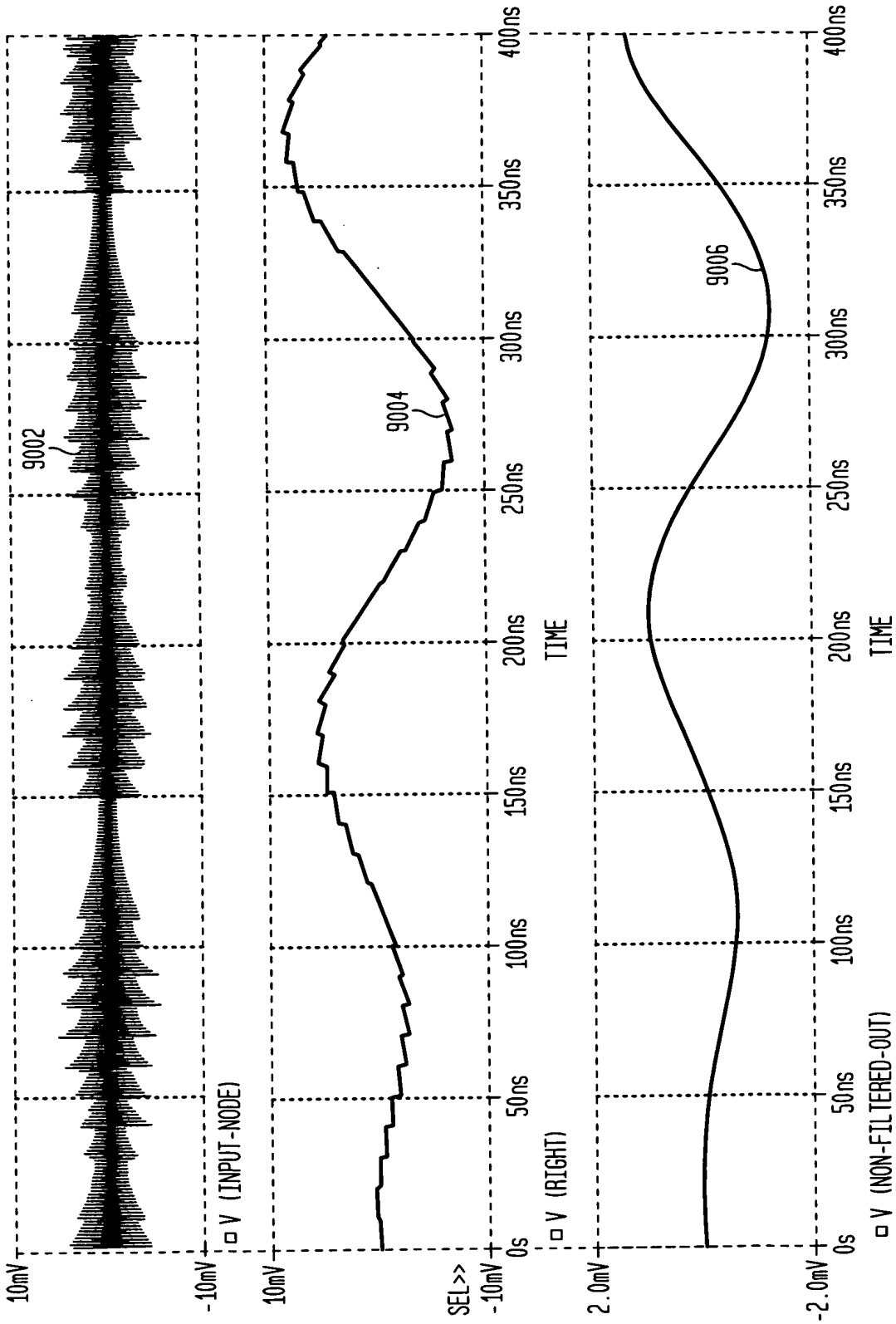
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 91



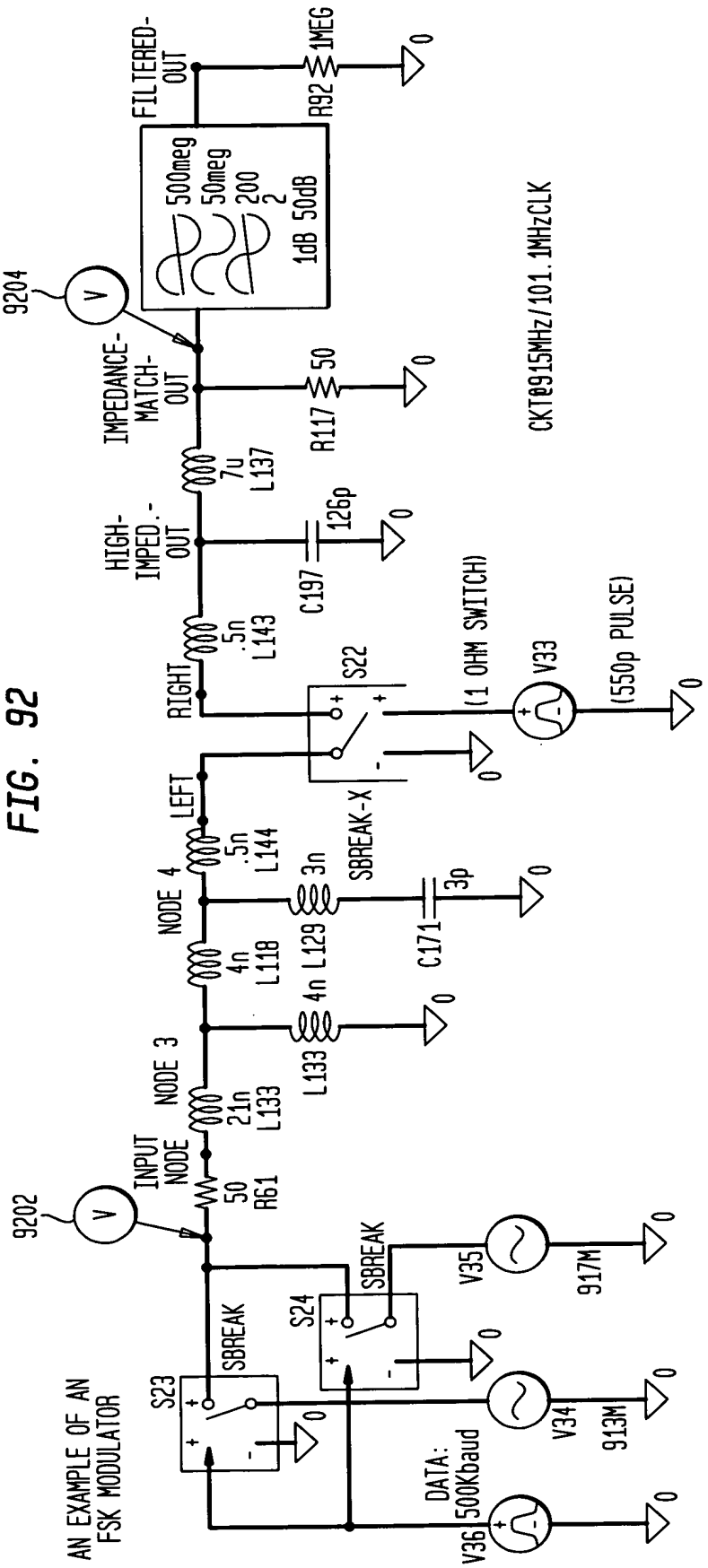

AN EXAMPLE OF AN FSK MODULATOR
9202
9204
INPUT NODE
50 R61
21n L133
NODE 3
4n L118
4n L129
L133
NODE 4
.5n L144
3n
C171
3p
SBREAK-X
LEFT
RIGHT
.5n L143
HIGH-IMPED.-OUT
C197
126p
7u L137
IMPEDANCE-MATCH-OUT
R117
50
FILTERED-OUT
R92
1MEG
500meg
50meg
200
2
1dB 50dB
S22
S23
S24
SBREAK
SBREAK
(1 OHM SWITCH)
(550p PULSE)
V33
V34
913M
V35
917M
V36
DATA: 500Kbaud
CKT@915MHz/101.1MHzCLK
0

FIG. 92

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Inventors: SORRELLS et al.
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FIG. 93

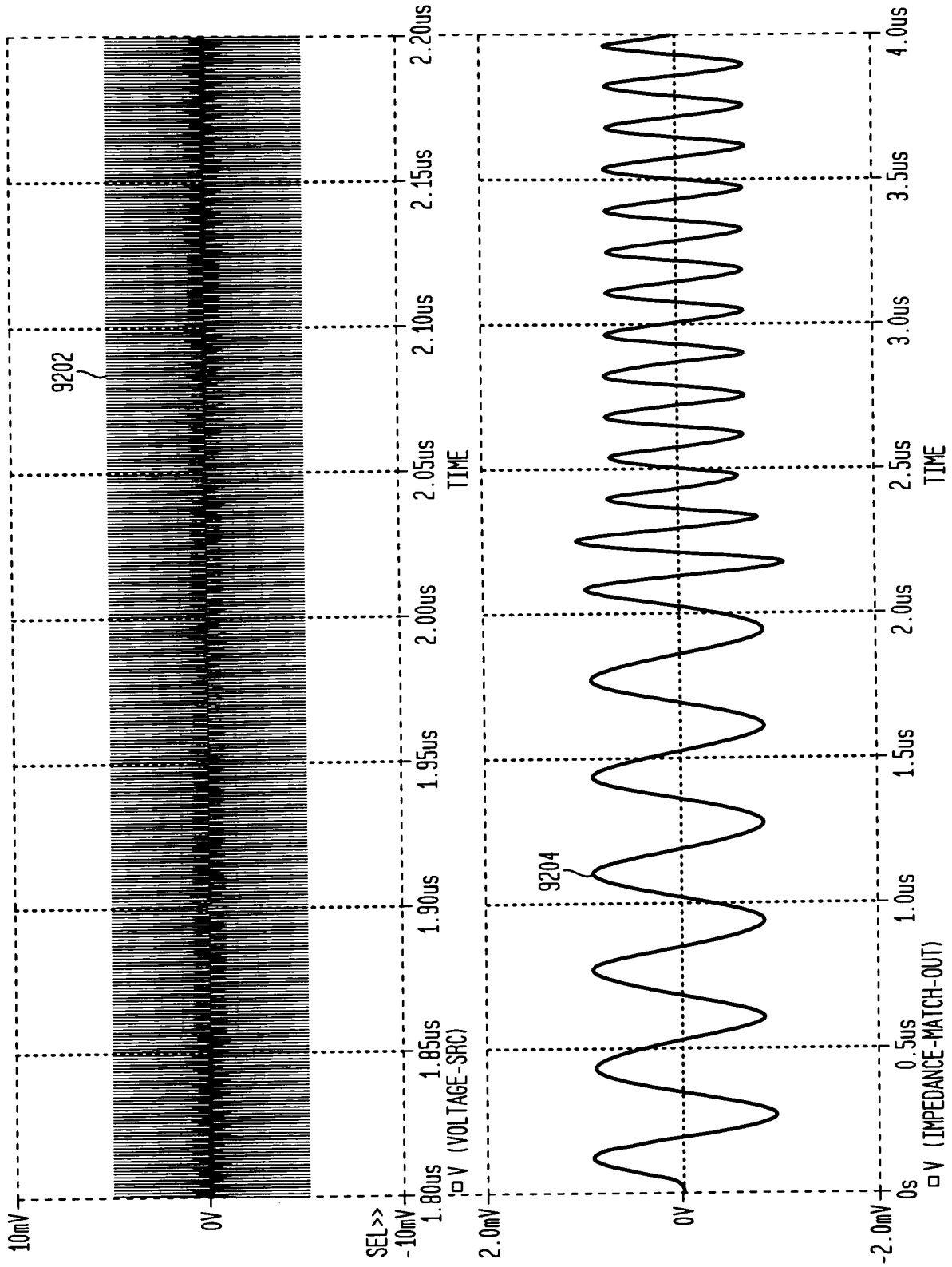
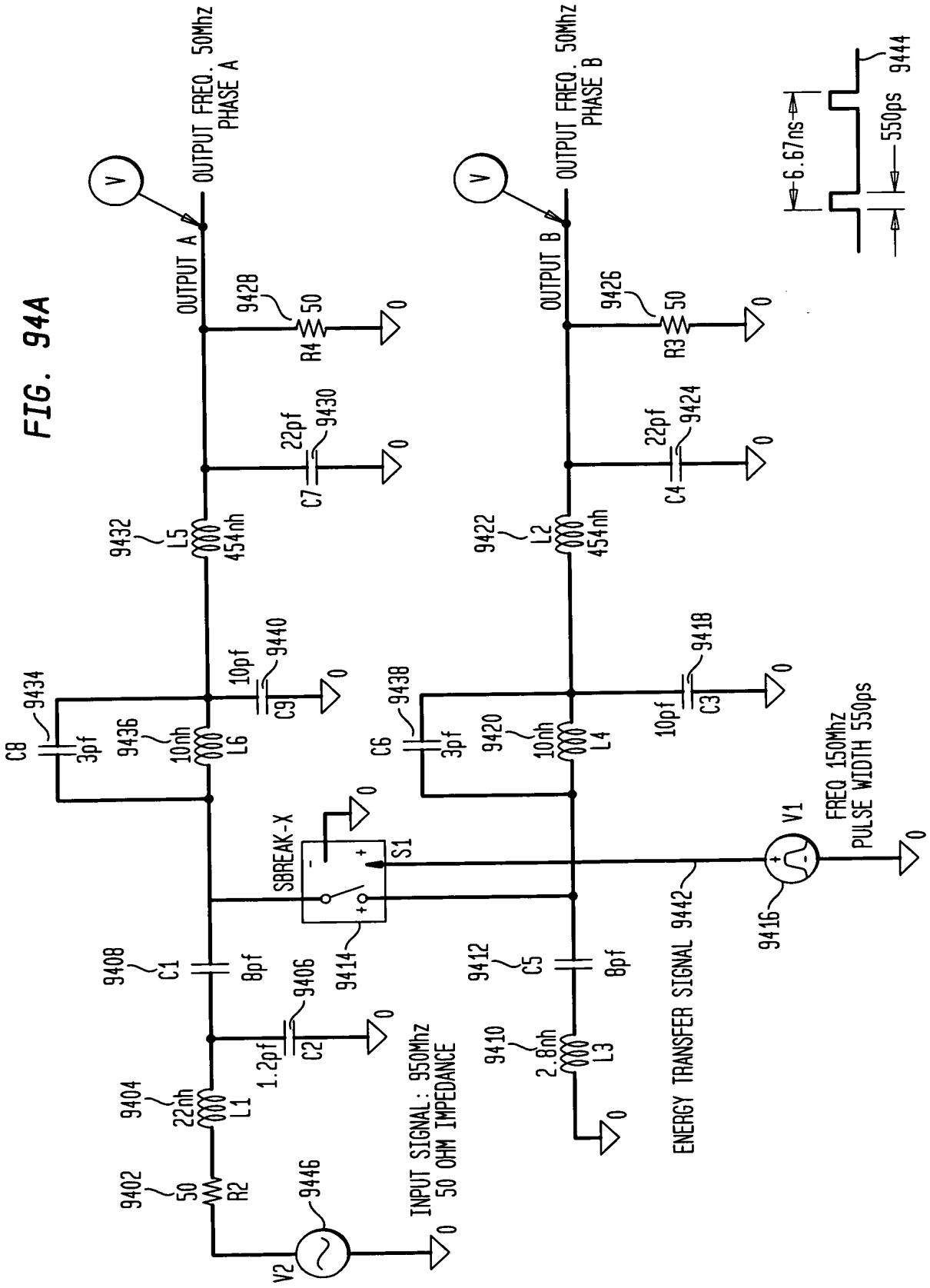


FIG. 94A


OUTPUT FREQ. 50Mhz
PHASE A
OUTPUT A
9428
R4
50
0
22pf
9430
C7
9432
L5
454nh
10pf
9440
C9
9434
C8
3pf
9436
10nh
L6
SBREAK-X
S1
9408
C1
8pf
9406
1.2pf
C2
9414
9404
22nh
L1
9402
50
R2
9446
V2
INPUT SIGNAL: 950Mhz
50 OHM IMPEDANCE
OUTPUT FREQ. 50Mhz
PHASE B
OUTPUT B
9426
R3
50
22pf
9424
C4
9422
L2
454nh
9418
10pf
C3
9438
C6
3pf
9420
10nh
L4
9412
C5
8pf
9410
2.8nh
L3
ENERGY TRANSFER SIGNAL 9442
V1
9416
FREQ 150Mhz
PULSE WIDTH 550ps
6.67ns
550ps
9444

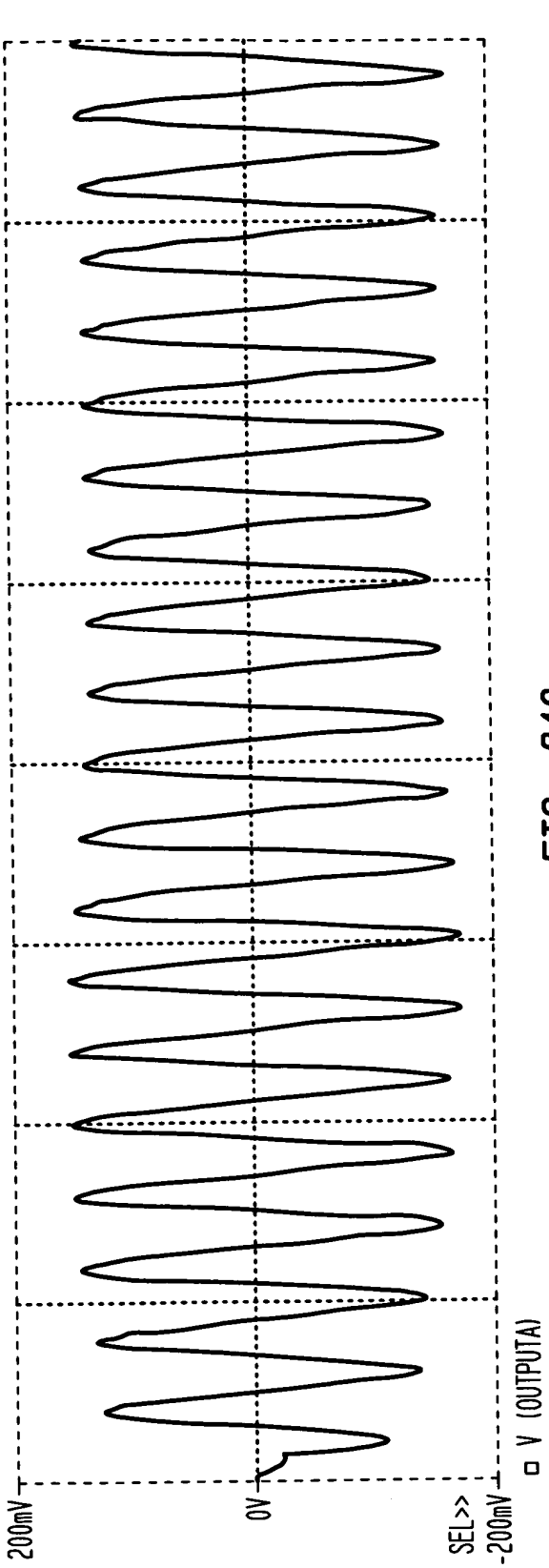



FIG. 94B

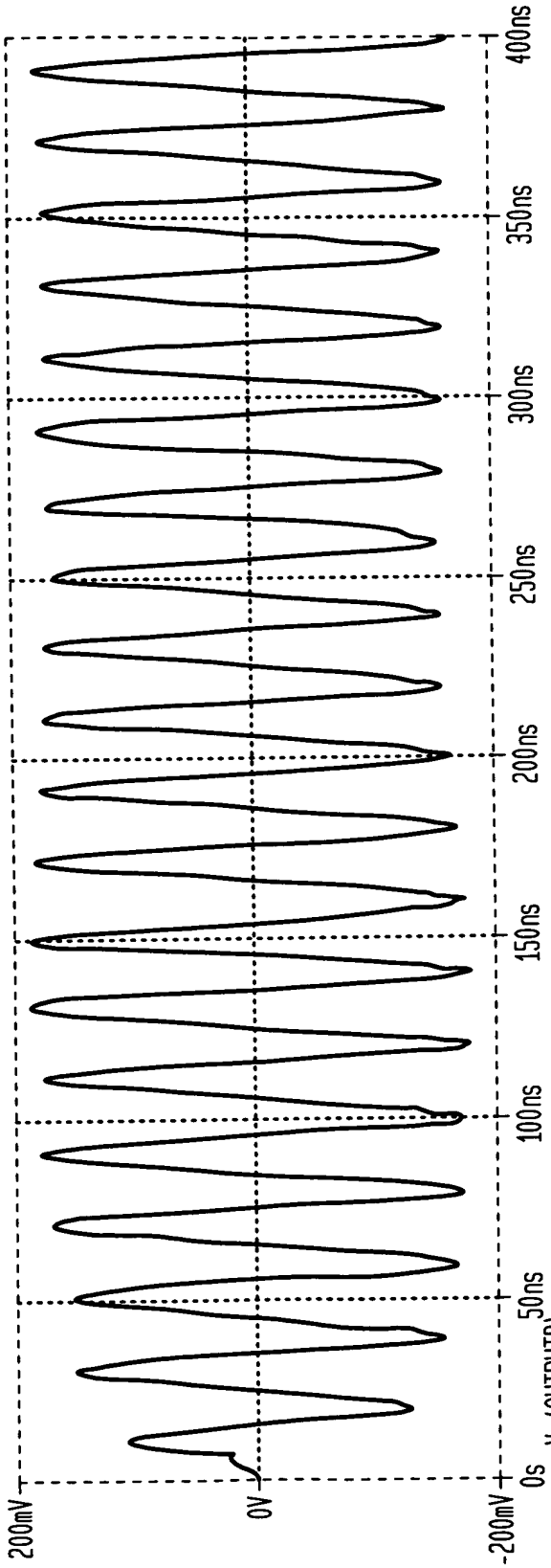



FIG. 94C

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Inventors: SORRELLS et al.
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For: Method and System for Down-Converting an
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FIG. 95

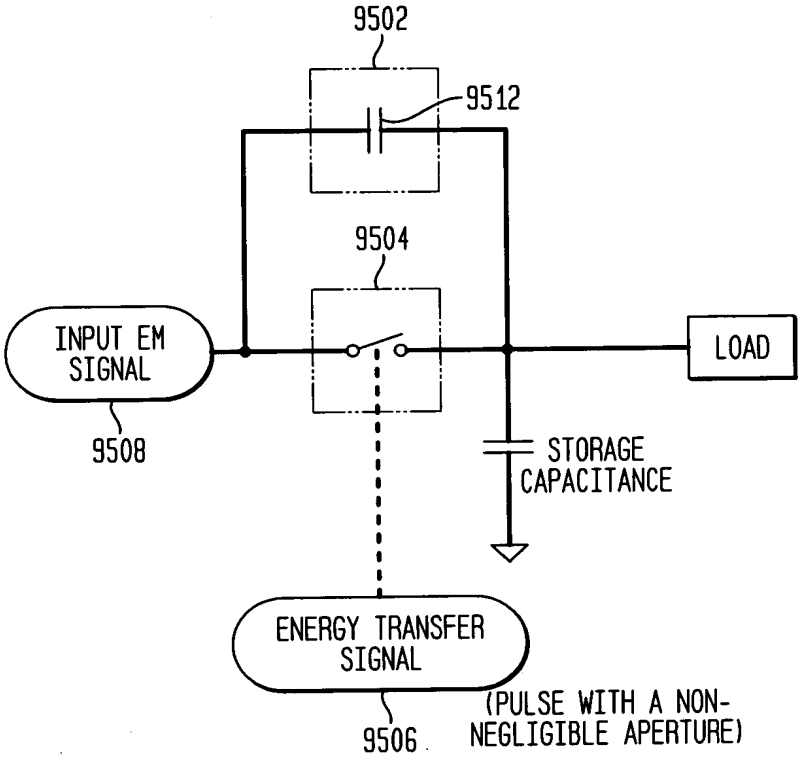


FIG. 96

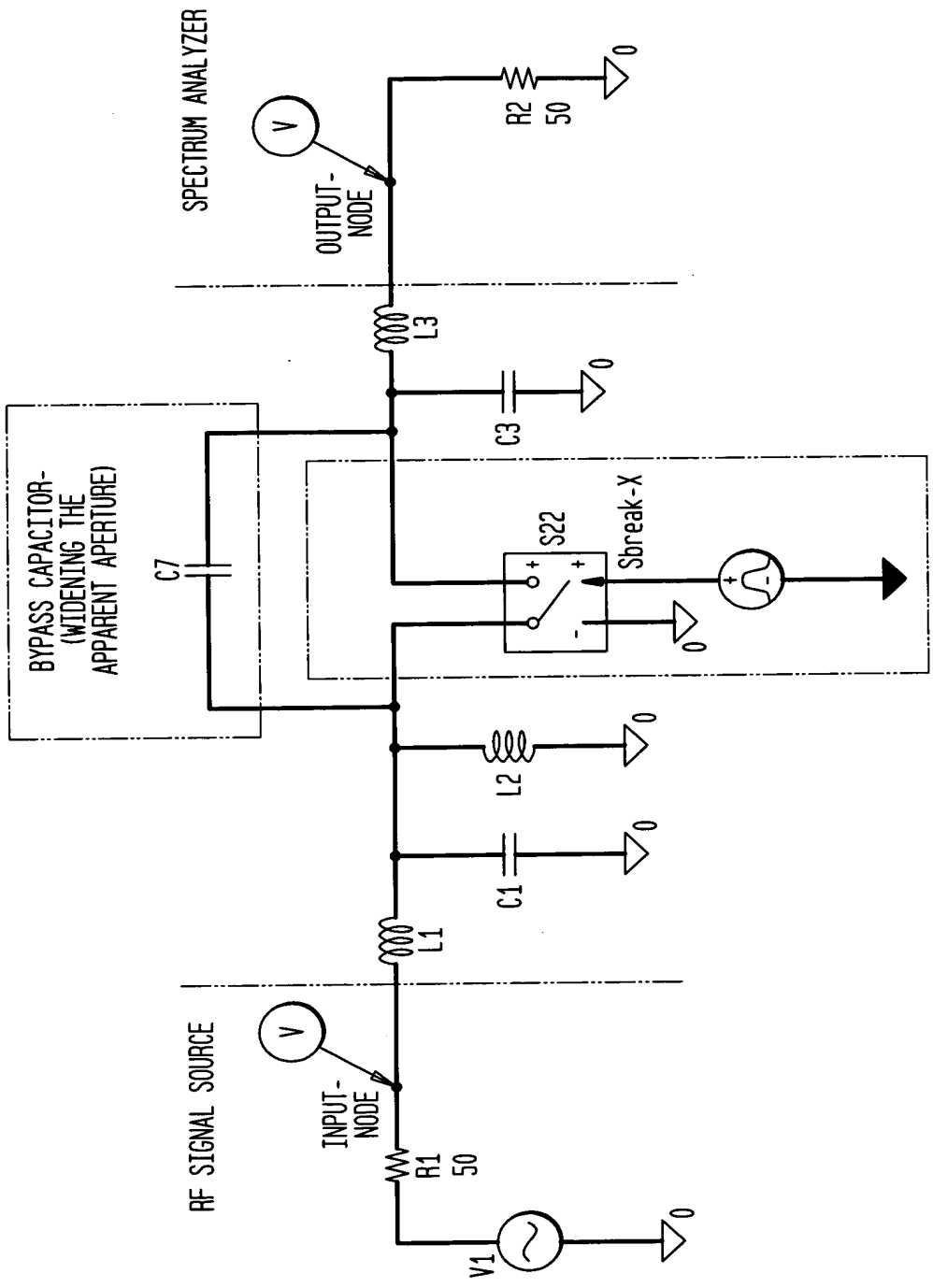
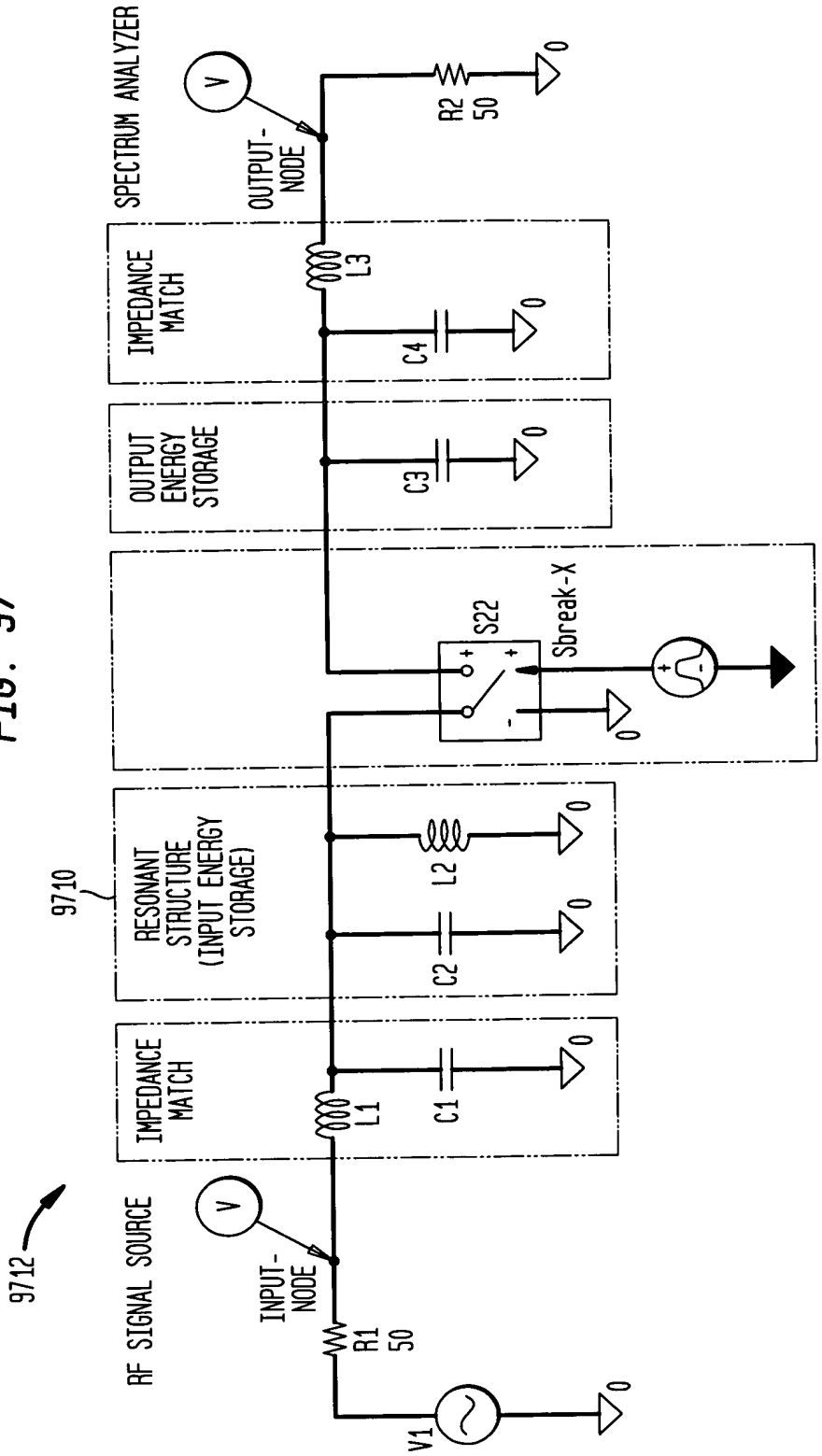

SPECTRUM ANALYZER
OUTPUT-NODE
V
R2
50
0
L3
C3
BYPASS CAPACITOR-(WIDENING THE APPARENT APERTURE)
C7
S22
Sbreak-X
L2
C1
L1
RF SIGNAL SOURCE
INPUT-NODE
R1
50
V1

FIG. 97


9712
RF SIGNAL SOURCE
INPUT-NODE
R1
50
V1
9710
IMPEDANCE MATCH
L1
C1
RESONANT STRUCTURE (INPUT ENERGY STORAGE)
L2
C2
S22
Sbreak-X
OUTPUT ENERGY STORAGE
C3
IMPEDANCE MATCH
L3
C4
OUTPUT-NODE
SPECTRUM ANALYZER
R2
50
0

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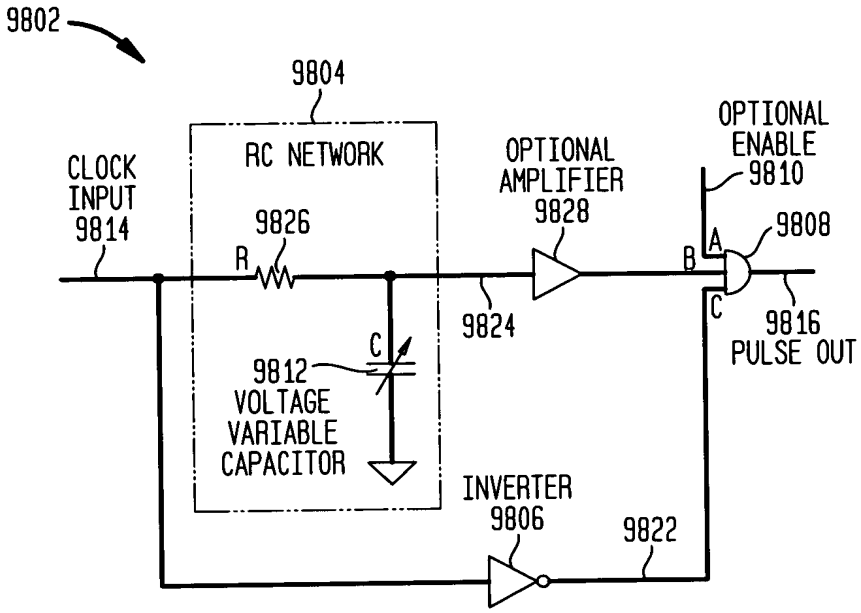
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 98A



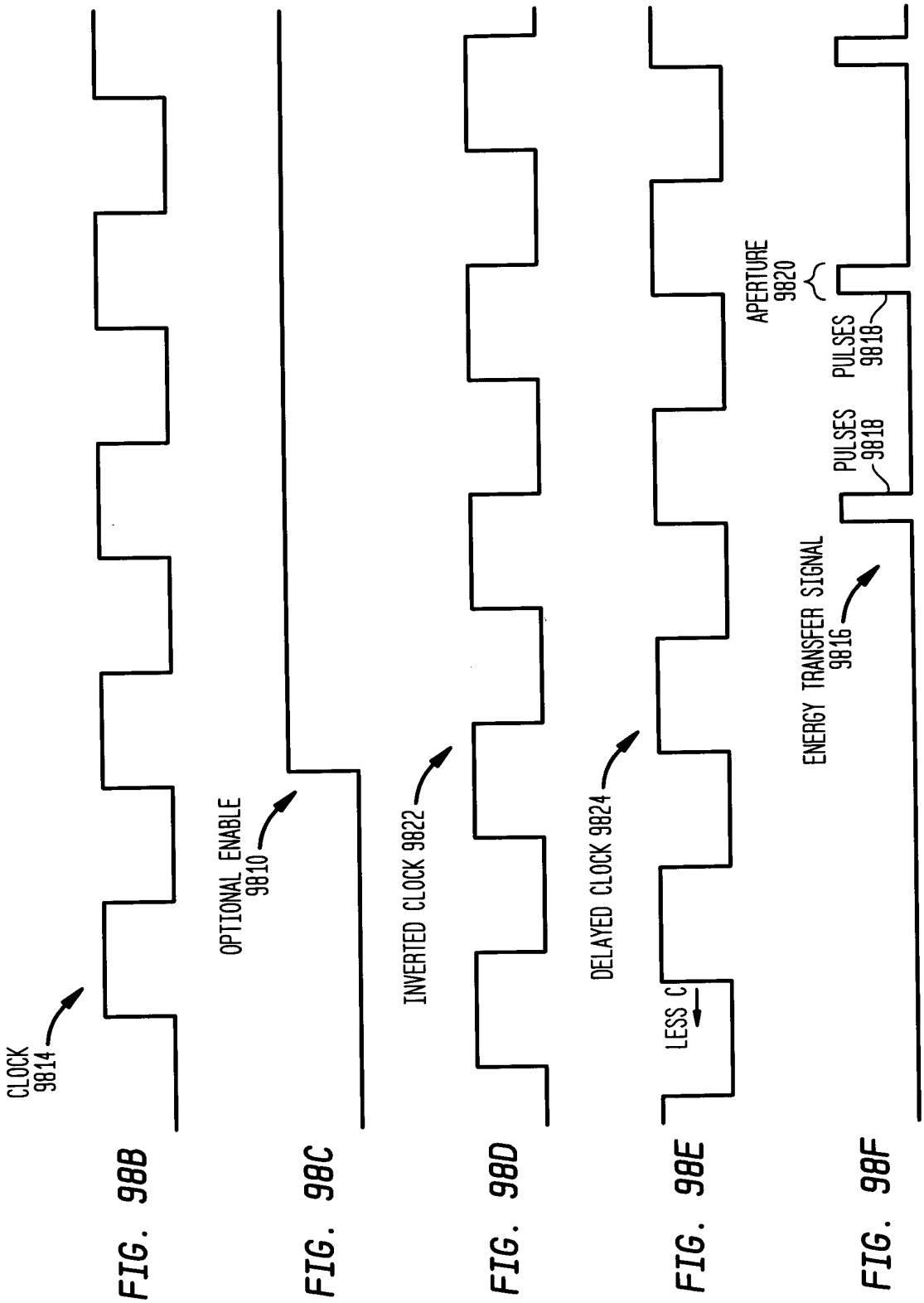



FIG. 98B

FIG. 98C

FIG. 98D

FIG. 98E

FIG. 98F

FIG. 99

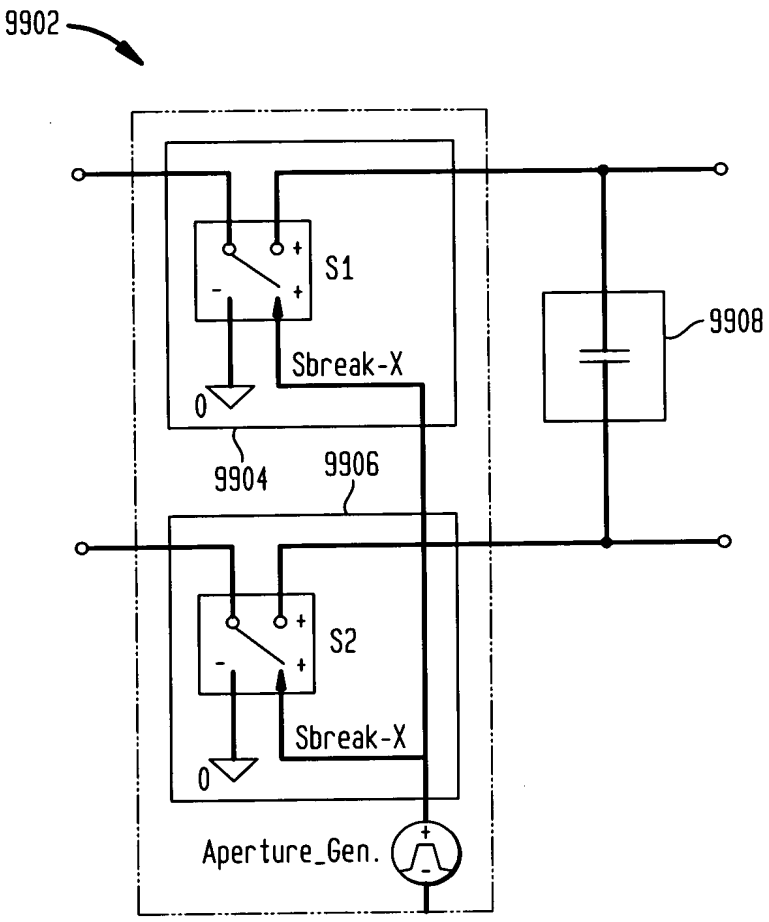


FIG. 100

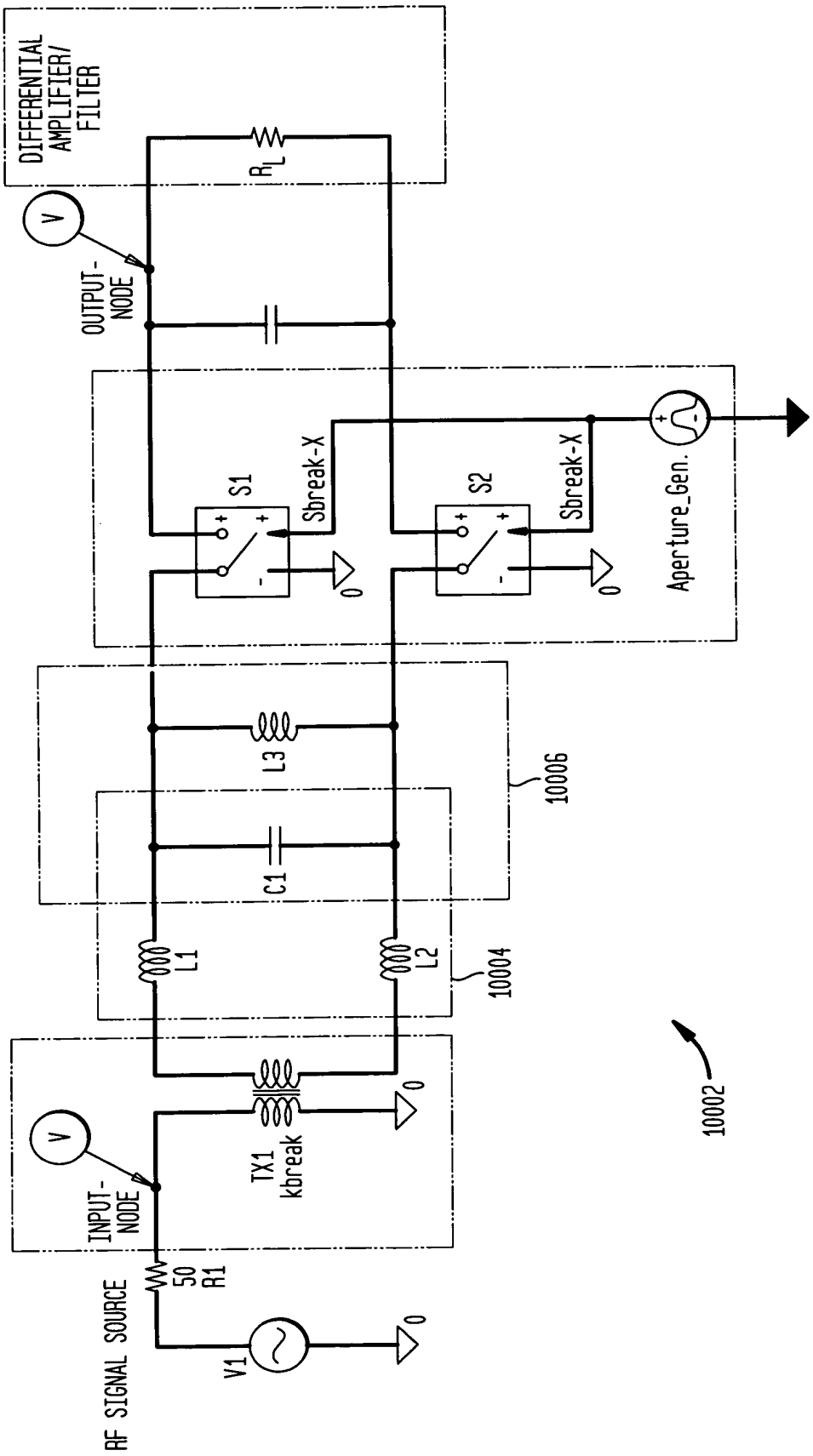

DIFFERENTIAL AMPLIFIER/ FILTER
$R_L$
V
OUTPUT-NODE
S1
Sbreak-X
S2
Sbreak-X
Aperture_Gen.
0
L3
C1
10006
L1
L2
10004
TX1
kbreak
INPUT-NODE
50
R1
RF SIGNAL SOURCE
V1
10002

FIG. 101

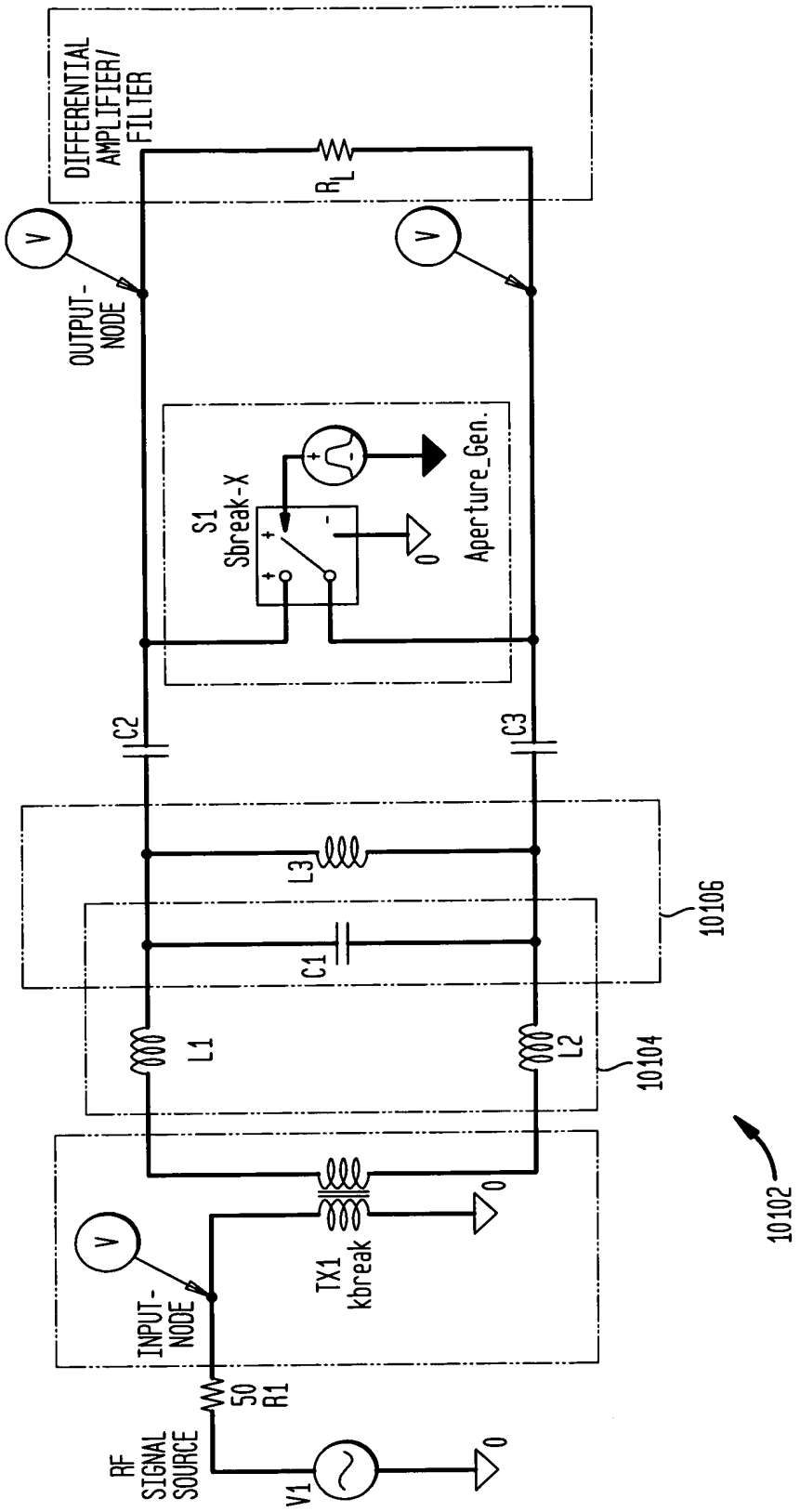

DIFFERENTIAL AMPLIFIER/ FILTER
$R_L$
V
OUTPUT-NODE
S1
Sbreak-X
Aperture_Gen.
0
C2
C3
L3
C1
10106
L1
L2
10104
TX1
Kbreak
INPUT-NODE
50
R1
RF SIGNAL SOURCE
V1
10102

FIG. 102

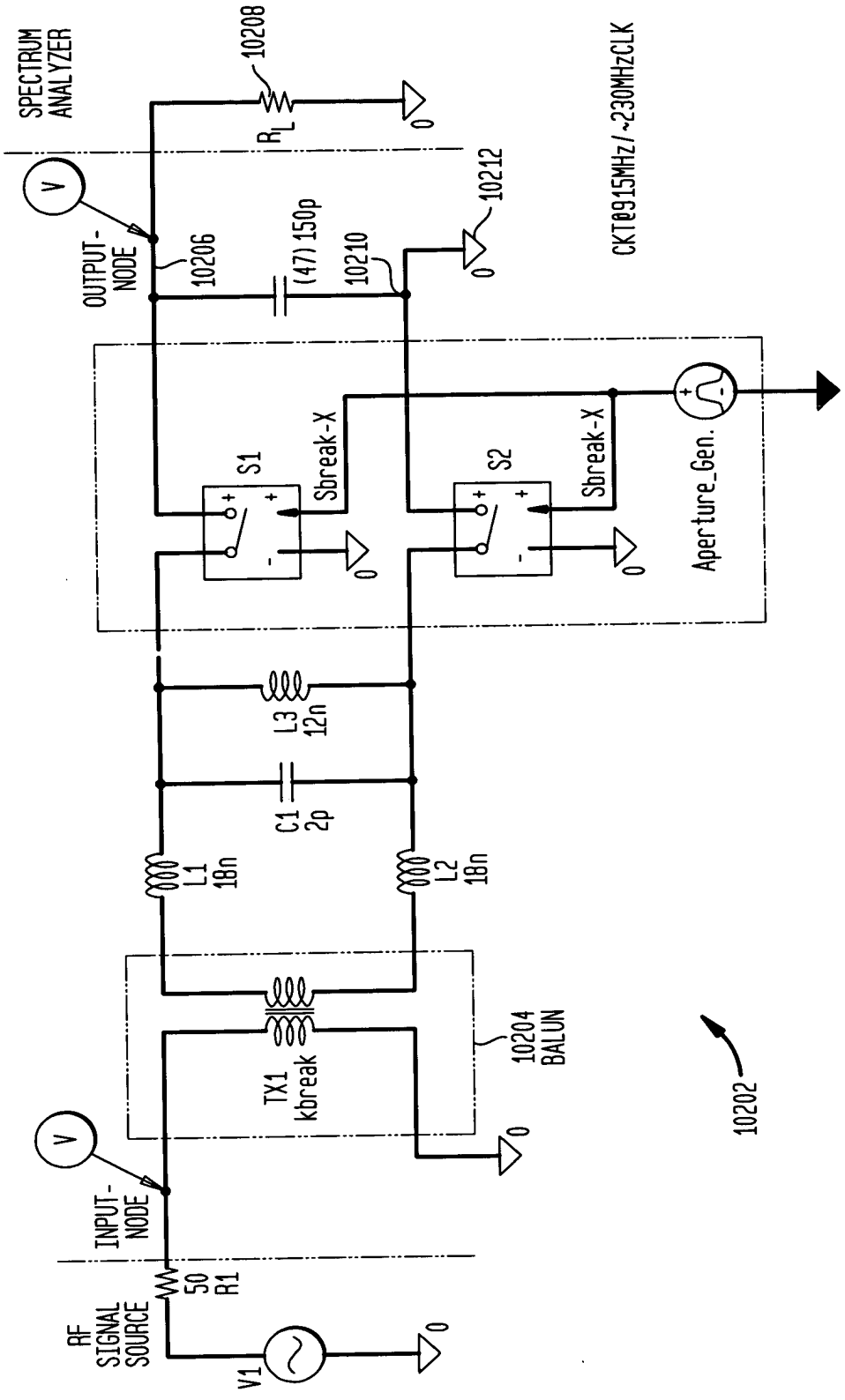

SPECTRUM ANALYZER
10208
$R_L$
0
V
OUTPUT-NODE
10206
(47) 150p
10210
10212
0
CKT@915MHz/~230MHzCLK
S1
Sbreak-X
S2
Sbreak-X
Aperture_Gen.
L3 12n
C1 2p
L1 18n
L2 18n
TX1 kbreak
10204 BALUN
10202
V
INPUT-NODE
50 R1
RF SIGNAL SOURCE
V1
0

FIG. 103

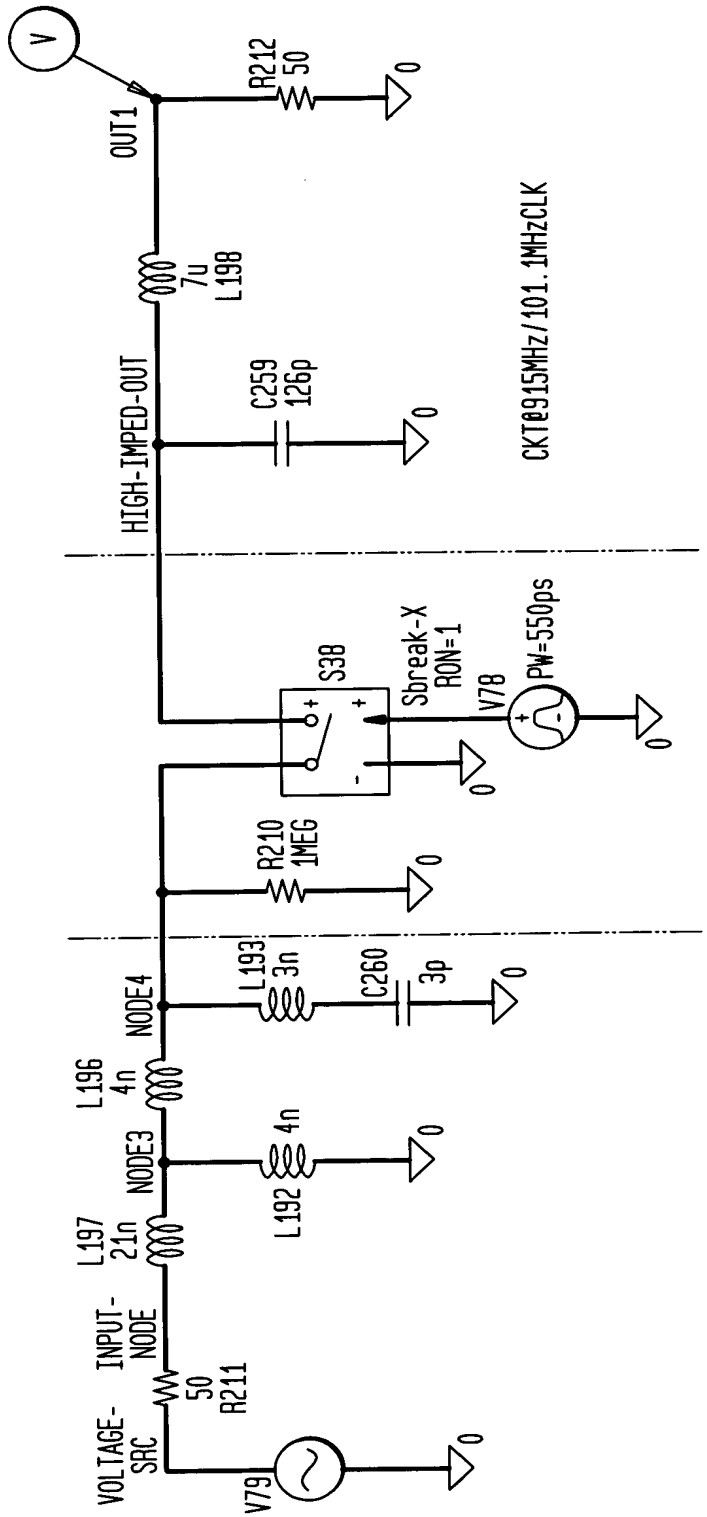
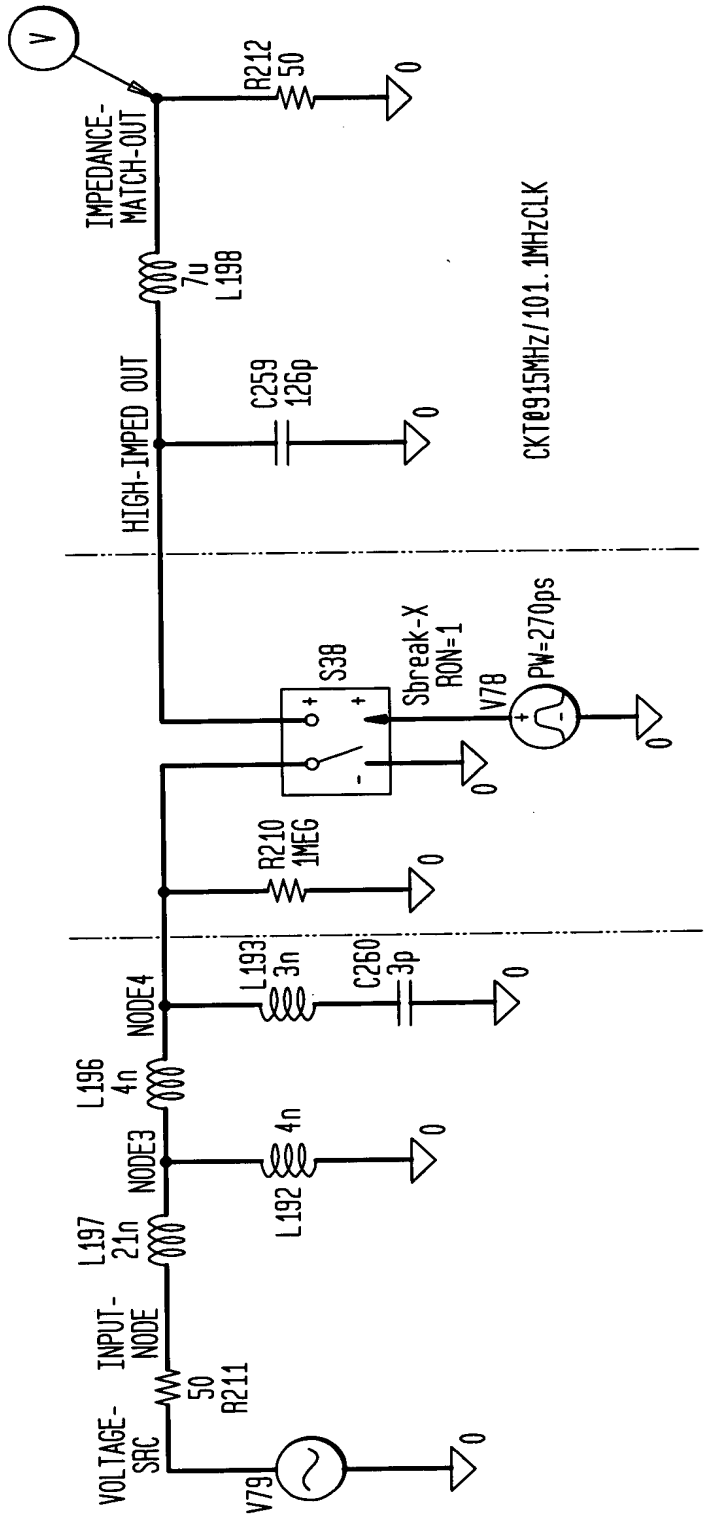

V
OUT1
R212
50
0
7u
L198
HIGH-IMPED-OUT
C259
126p
0
CKT@915MHz/101.1MHzCLK
S38
Sbreak-X
RON=1
V78
PW=550ps
0
0
R210
1MEG
0
L193
3n
C260
3p
0
NODE4
L196
4n
NODE3
4n
L192
0
L197
21n
INPUT-
NODE
50
R211
VOLTAGE-
SRC
V79
0

FIG. 104


V
R212
50
0
IMPEDANCE-
MATCH-OUT
7u
L198
HIGH-IMPED OUT
C259
126p
0
CKT@915MHz/101.1MHzCLK
S38
Sbreak-X
RON=1
V78
PW=270ps
0
0
R210
1MEG
0
L193
3n
C260
3p
0
NODE4
L196
4n
NODE3
4n
L192
0
L197
21n
INPUT-
NODE
50
R211
VOLTAGE-
SRC
V79
0

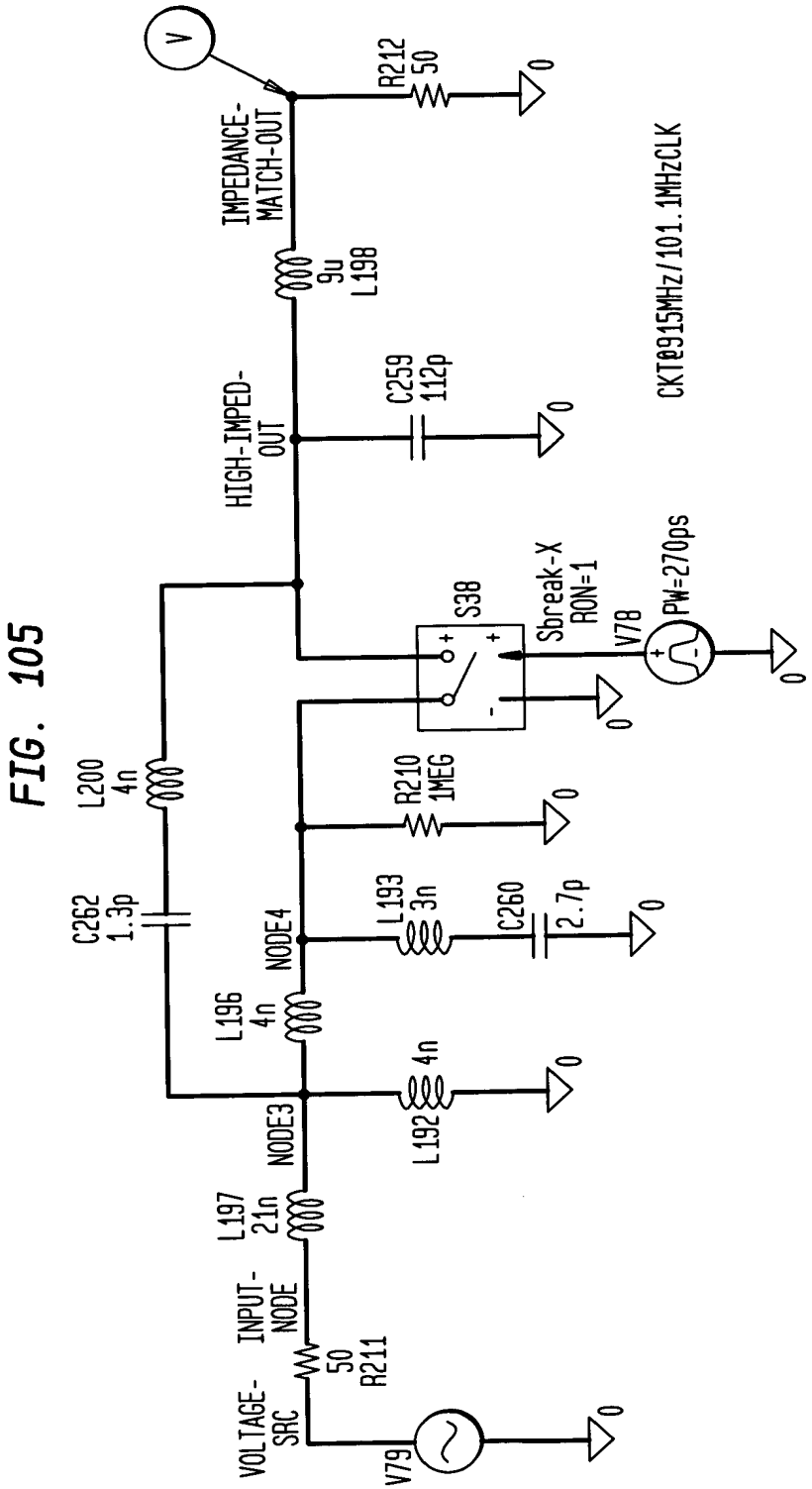

V
R212
50
0
IMPEDANCE-
MATCH-OUT
9u
L198
C259
112p
HIGH-IMPED-
OUT
CKT@915MHz/101.1MHzCLK
S38
Sbreak-X
RON=1
V78
PW=270ps
L200
4n
R210
1MEG
C262
1.3p
L193
3n
C260
2.7p
NODE4
L196
4n
4n
L192
NODE3
L197
21n
INPUT-
NODE
50
R211
VOLTAGE-
SRC
V79

FIG. 105

FIG. 106

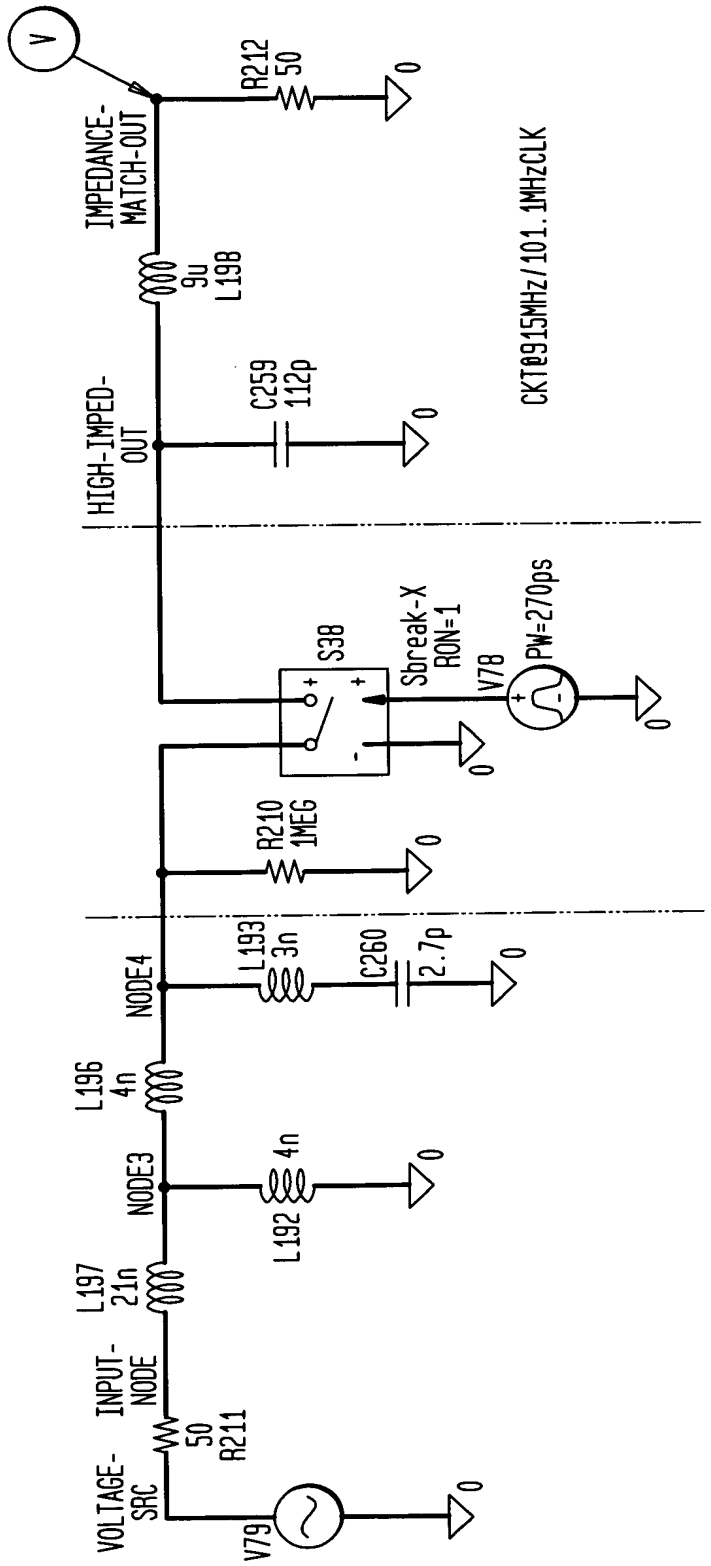

V
R212
50
0
IMPEDANCE-
MATCH-OUT
9u
L198
C259
112p
HIGH-IMPED-
OUT
CKT@915MHz/101.1MHzCLK
S3B
Sbreak-X
RON=1
V78
PW=270ps
R210
1MEG
L193
3n
C260
2.7p
NODE4
L196
4n
NODE3
4n
L192
L197
21n
INPUT-
NODE
50
R211
VOLTAGE-
SRC
V79

FIG. 107A

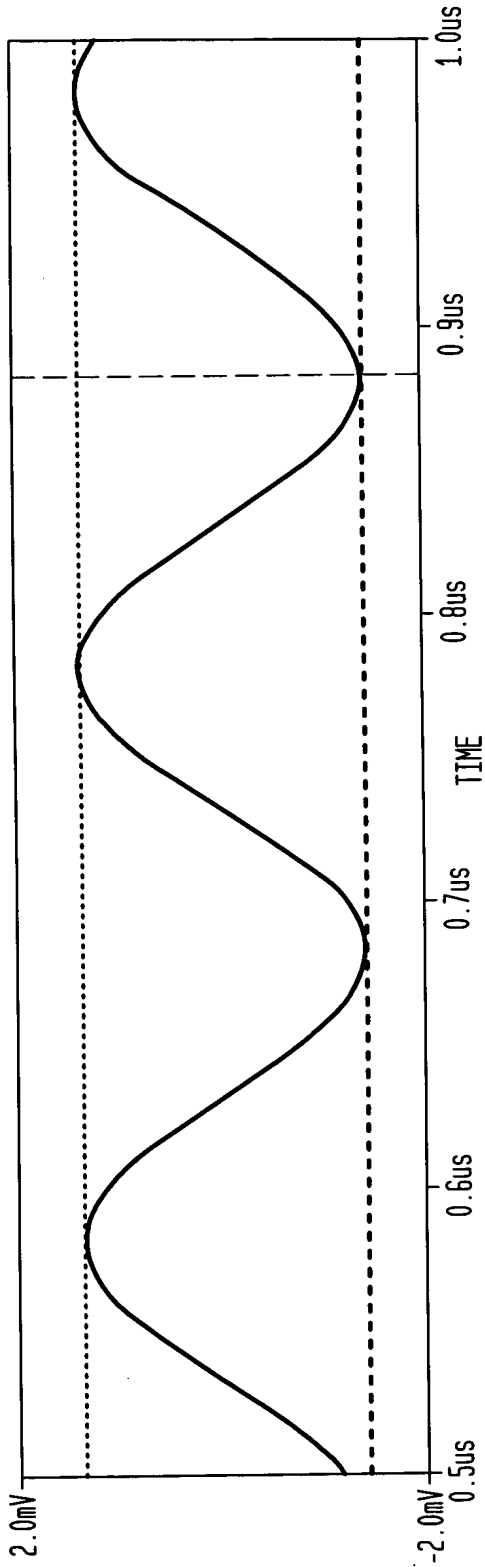



FIG. 107B

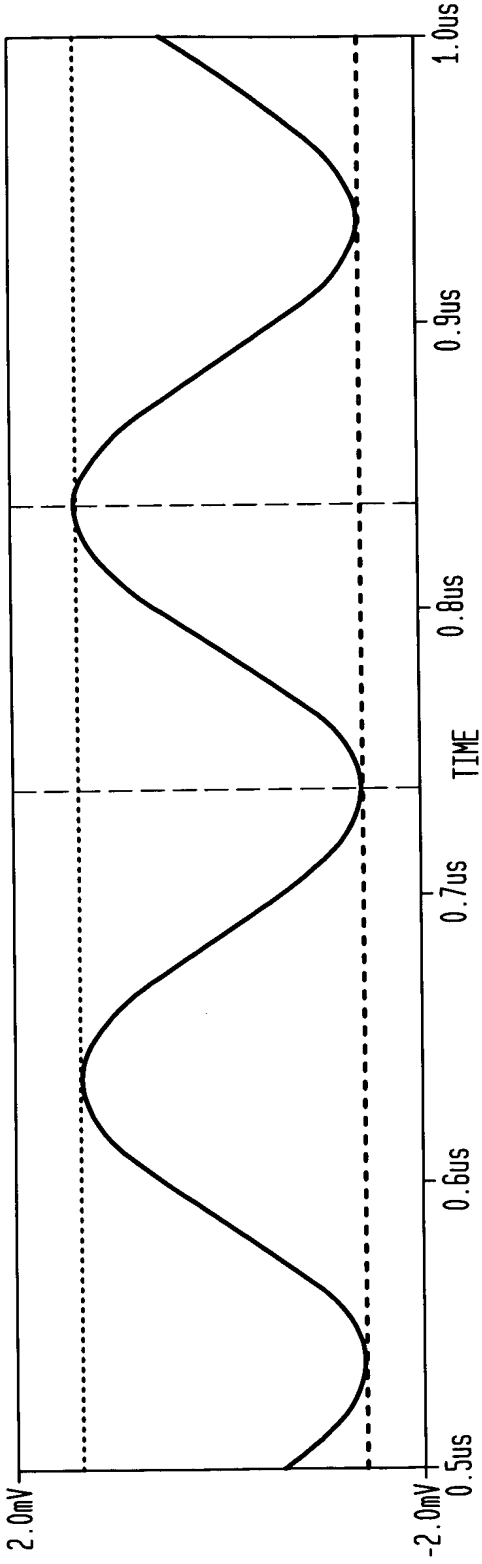


FIG. 108A

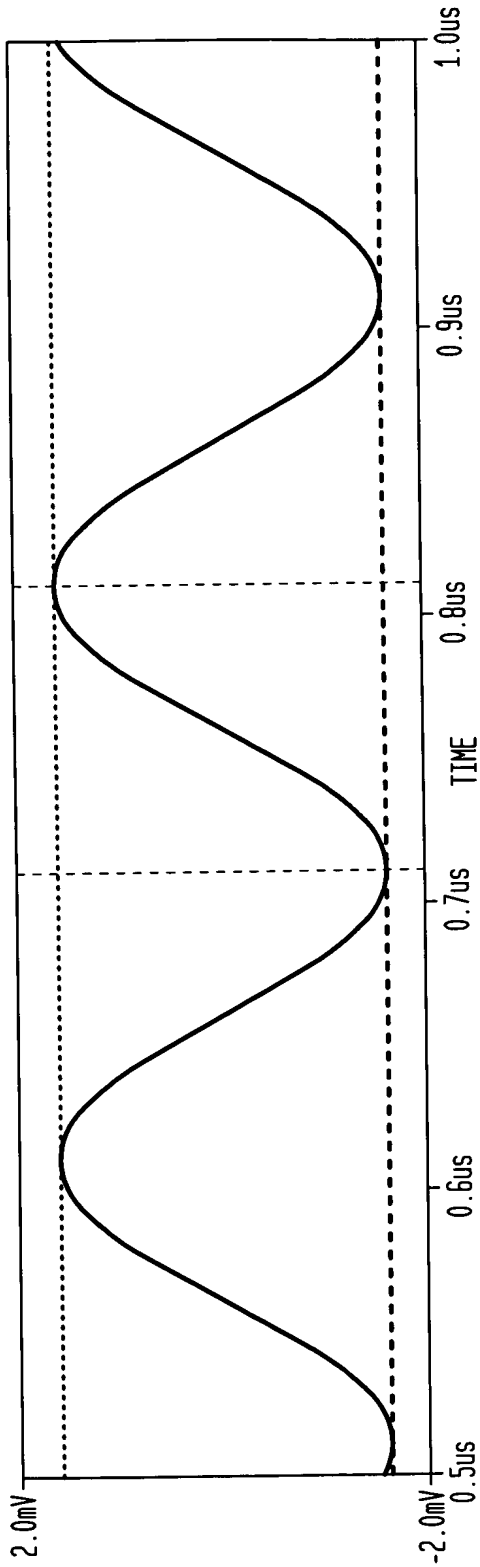
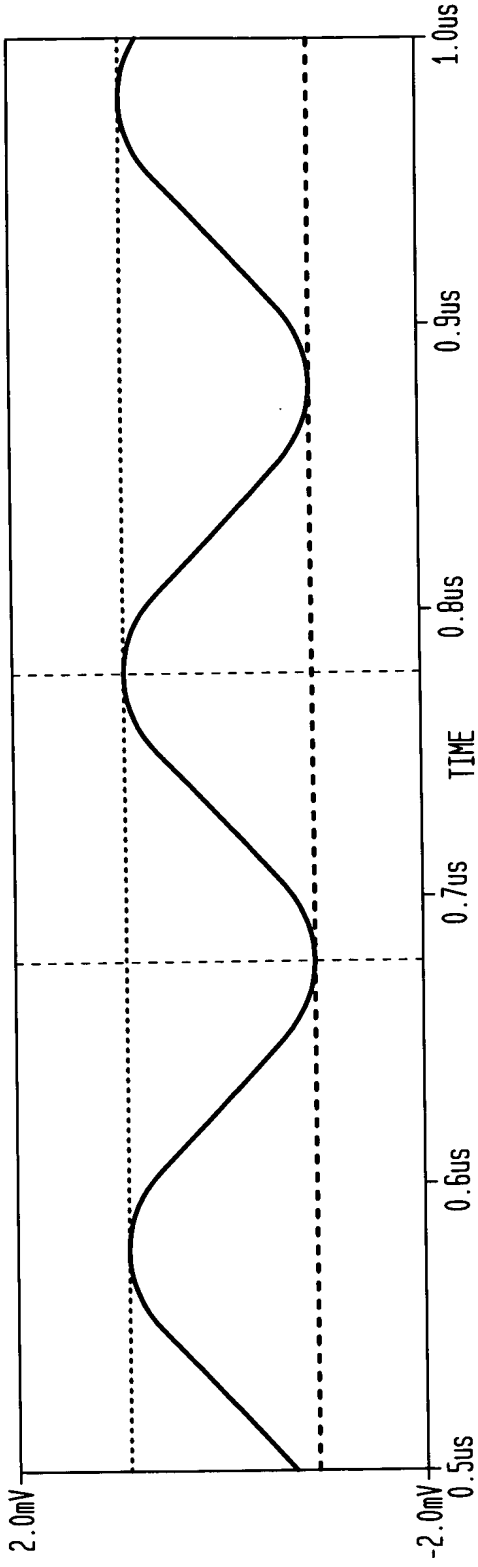



FIG. 108B



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Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
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FIG. 109A

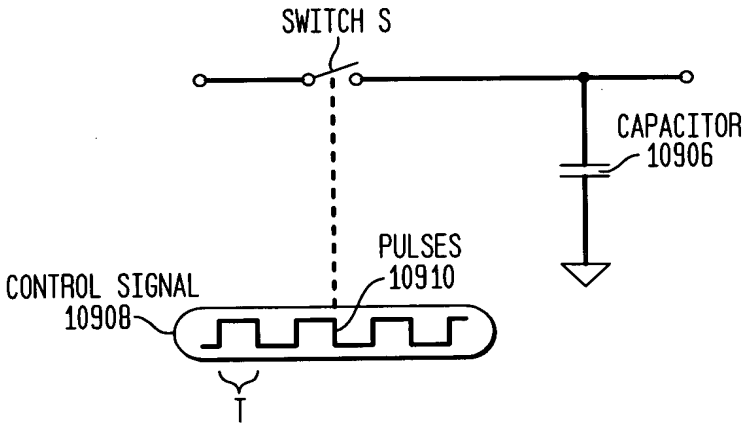



FIG. 109B

$$q=C\cdot V \qquad \text{EQ. 10}$$

$$V=A\cdot\sin(t) \qquad \text{EQ. 11}$$

$$q(t)=C\cdot A\cdot\sin(t) \qquad \text{EQ. 12}$$

$$\Delta q(t)=C\cdot A\cdot\sin(t)-C\cdot A\cdot\sin(t-T) \qquad \text{EQ. 13}$$

$$\Delta q(t)=C\cdot A\cdot(\sin(t)-\sin(t-T)) \qquad \text{EQ. 14}$$

$$\sin(\alpha)-\sin(\beta)=2\cdot\sin\left(\frac{\alpha-\beta}{2}\right)\cdot\cos\left(\frac{\alpha+\beta}{2}\right) \qquad \text{EQ. 15}$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left[\frac{t-(t-T)}{2}\right]\cdot\cos\left[\frac{t+(t-T)}{2}\right] \qquad \text{EQ. 16}$$

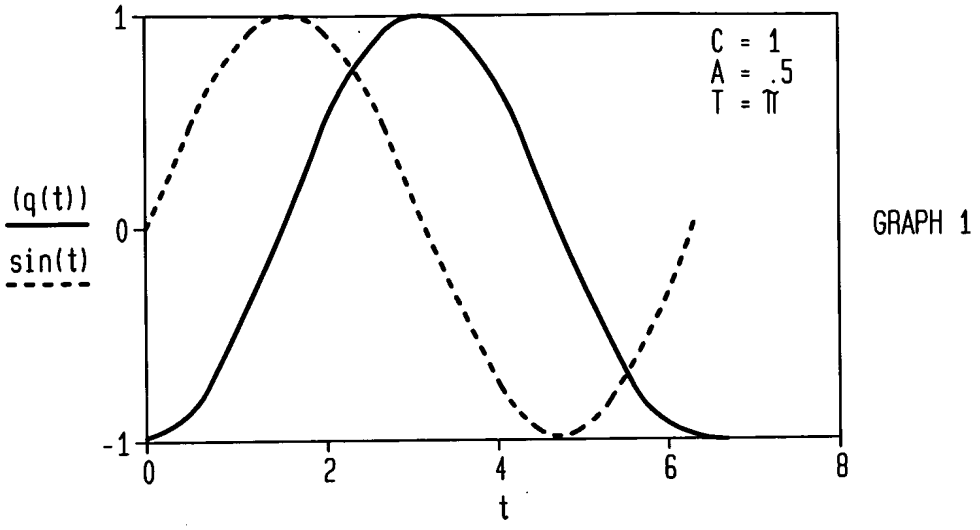
$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left(\frac{1}{2}\cdot T\right)\cdot\cos\left(t-\frac{1}{2}\cdot T\right) \qquad \text{EQ. 17}$$

$$q(t)=\int_{\cdot}^{\cdot} C\cdot A\cdot(\sin(t)-\sin(t-T))\,dt \qquad \text{EQ. 18}$$

$$q(t)=-\cos(t)\cdot C\cdot A+\cos(t-T)\cdot C\cdot A \qquad \text{EQ. 19}$$

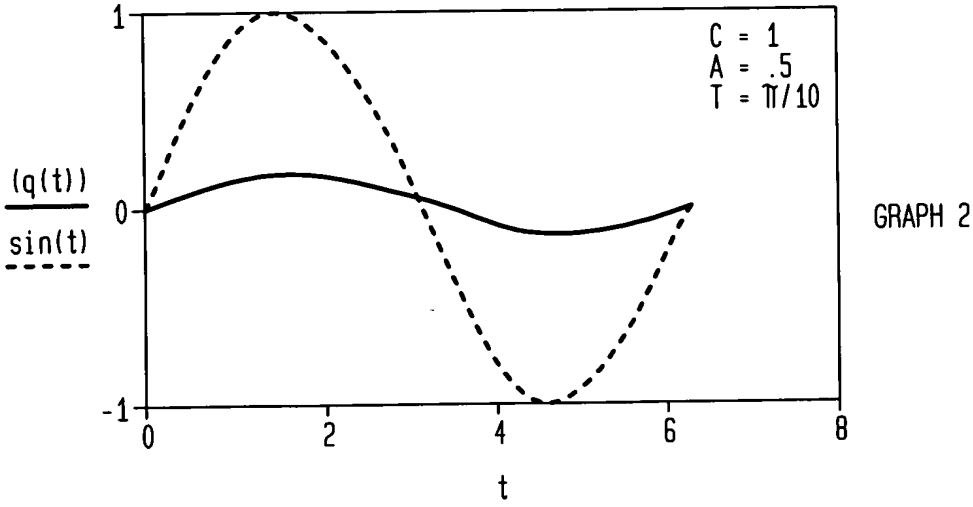
$$q(t)=C\cdot A\cdot(\cos(t-T)-\cos(t)) \qquad \text{EQ. 20}$$

## FIG. 109C




GRAPH 1

## FIG. 109D




GRAPH 2

## FIG. 109E

POWER-CHARGE RELATIONSHIP

| | |
|---|---|
| $q=C \cdot V$ | EQ. 21 |
| $V=q/C$ | EQ. 22 |
| $V=J/C$ | EQ. 23 |
| $J=q^2/C$ | EQ. 24 |
| $P=J/S$ | EQ. 25 |
| $P=\frac{q^2}{C \cdot S}$ | EQ. 26 |

## FIG. 109F

INSERTION LOSS

INSERTION LOSS IN dB IS EXPRESSED BY:

$$ILdB=10 \cdot \log\left(\frac{Pin}{Pout}\right) \text{ or}$$

$$ILdB=10 \cdot \log\left[\frac{\left(\frac{Vin^2}{Rin}\right)}{\left(\frac{Vout^2}{Rout}\right)}\right]$$

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FIG. 110A

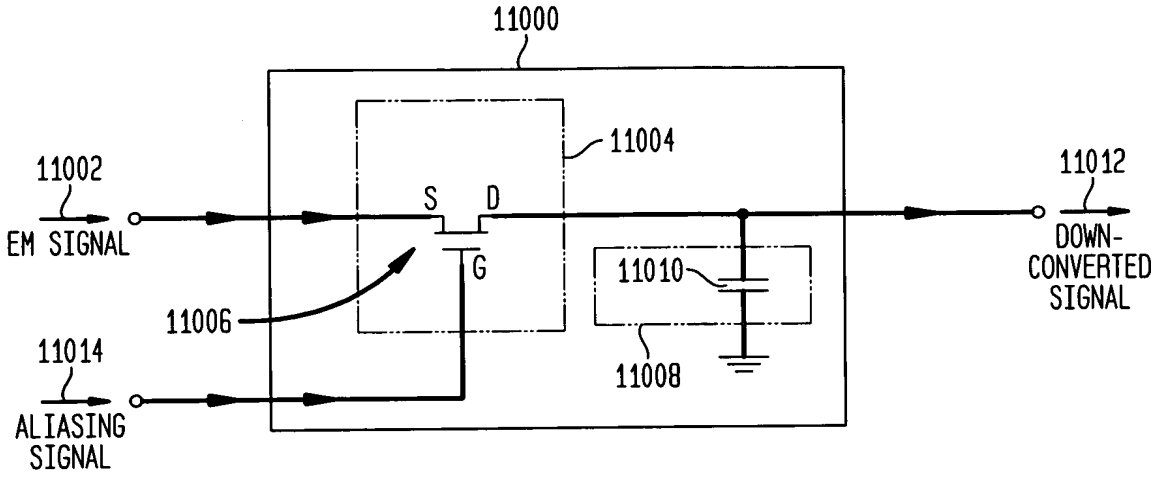
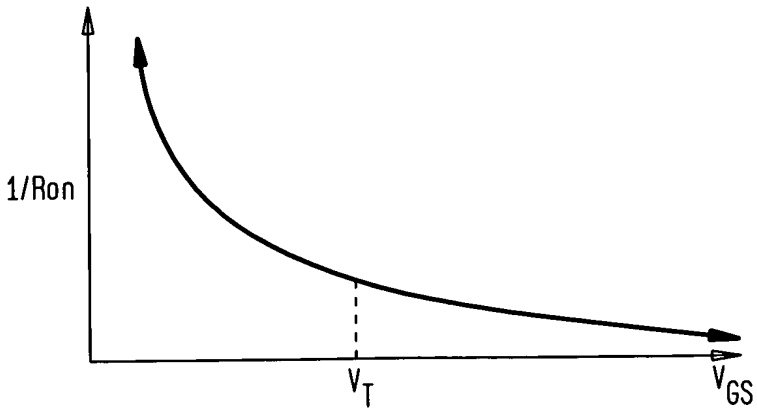



FIG. 110B



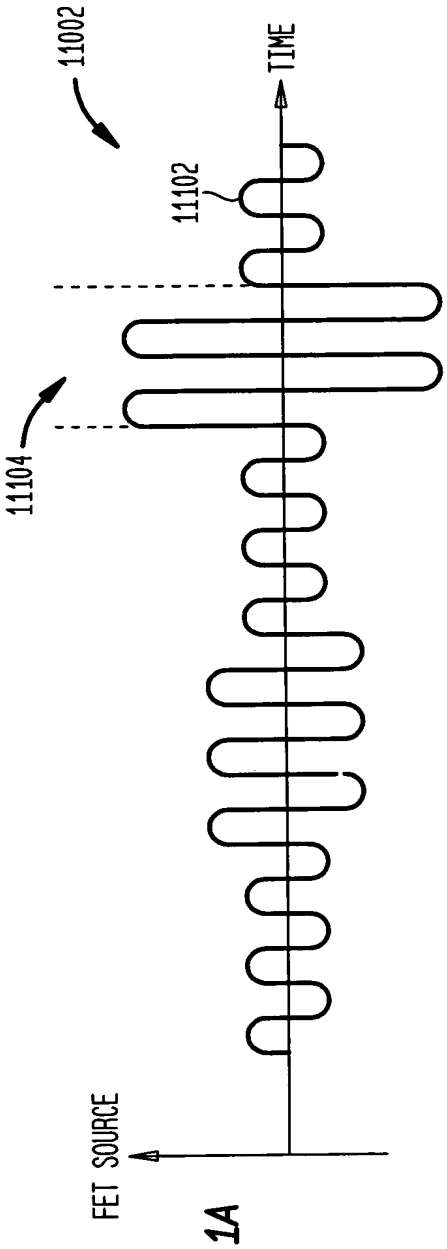



FIG. 111A

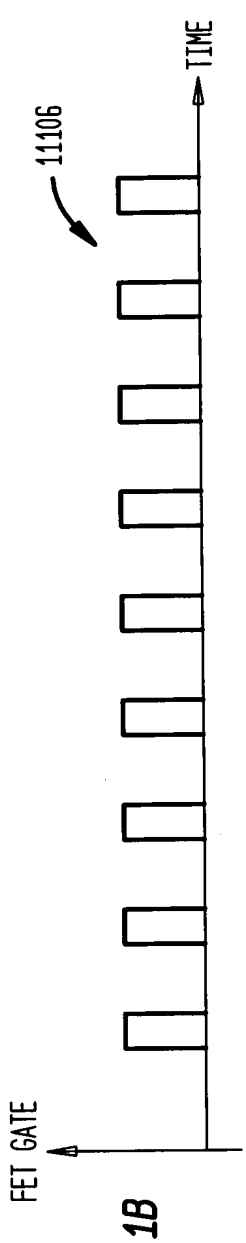



FIG. 111B

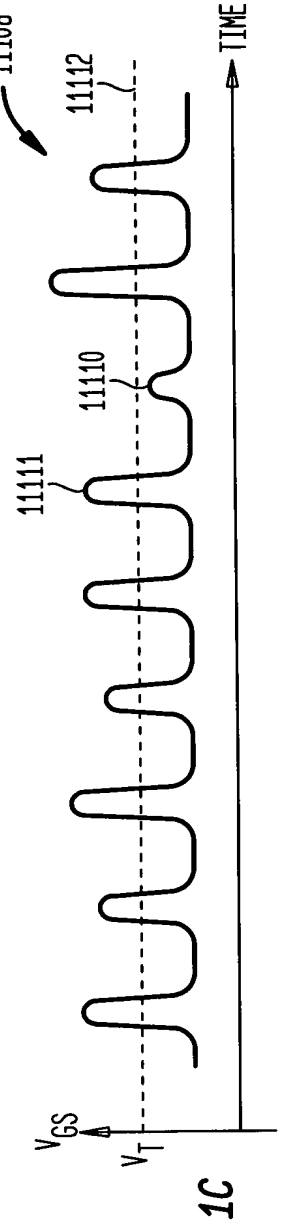



FIG. 111C

FIG. 112

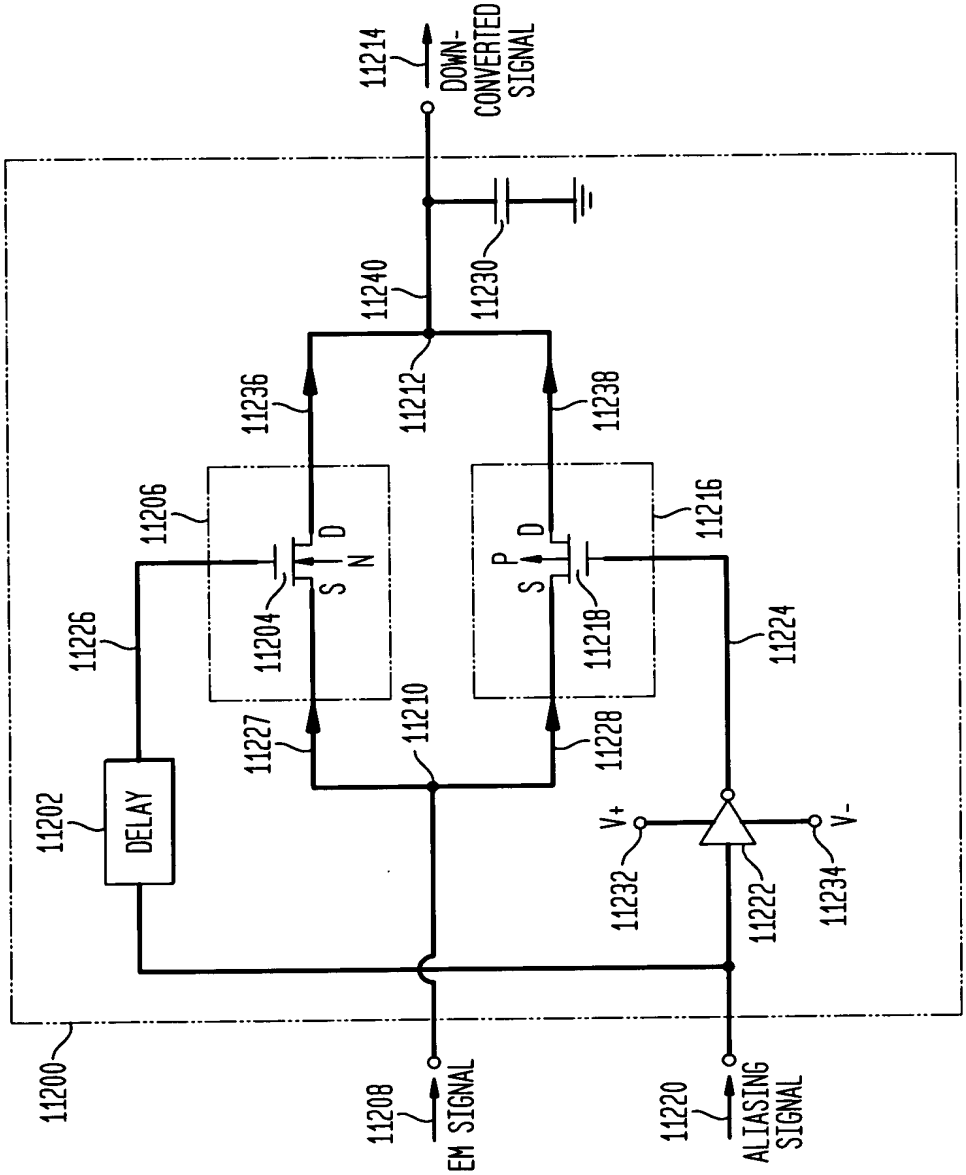

11214
DOWN-CONVERTED SIGNAL
11230
11240
11212
11236
11238
11206
11216
D
N
S
P
D
S
11204
11218
11226
11224
11227
11210
11228
11202
DELAY
V+
V-
11232
11222
11234
11200
11208
EM SIGNAL
11220
ALIASING SIGNAL

FIG. 113A

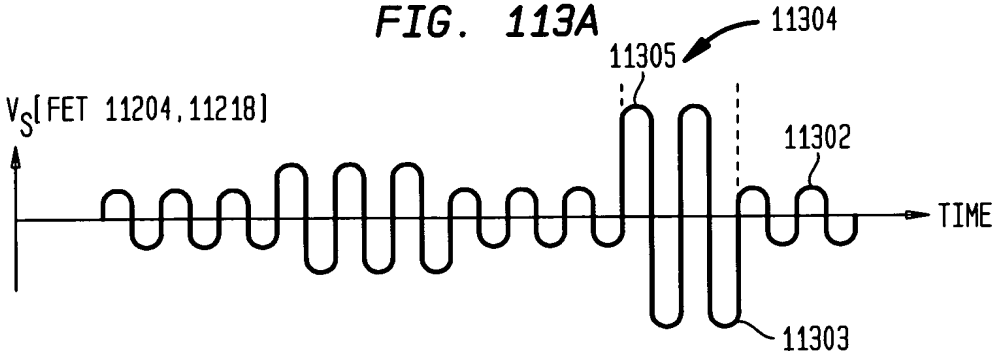



FIG. 113B

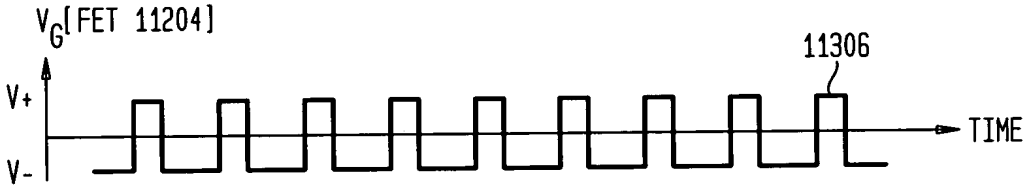



FIG. 113C

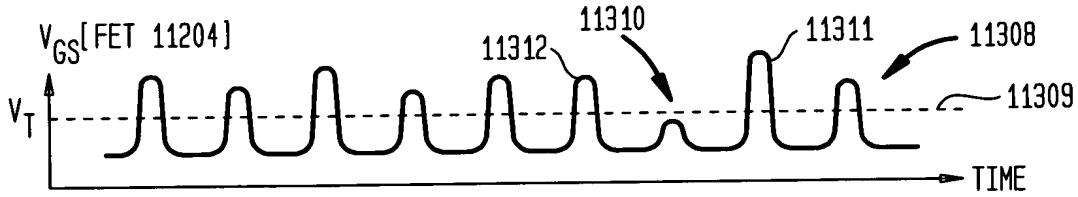



FIG. 113D

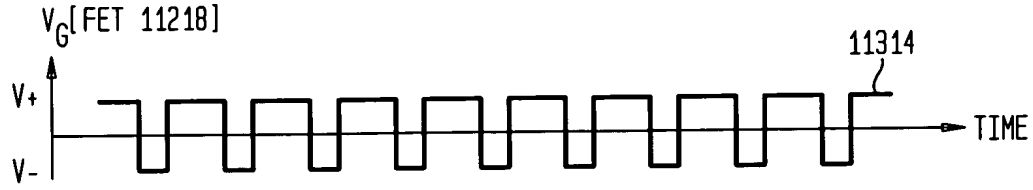



FIG. 113E

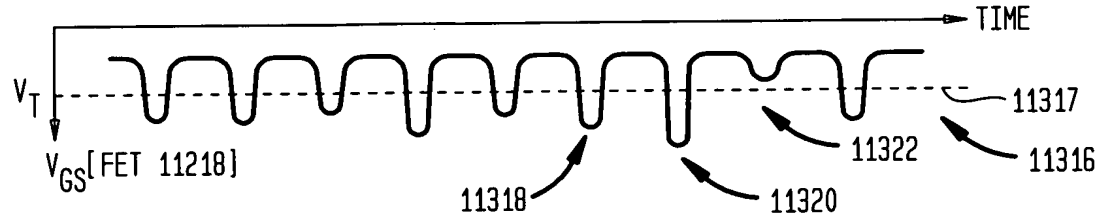


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FIG. 114

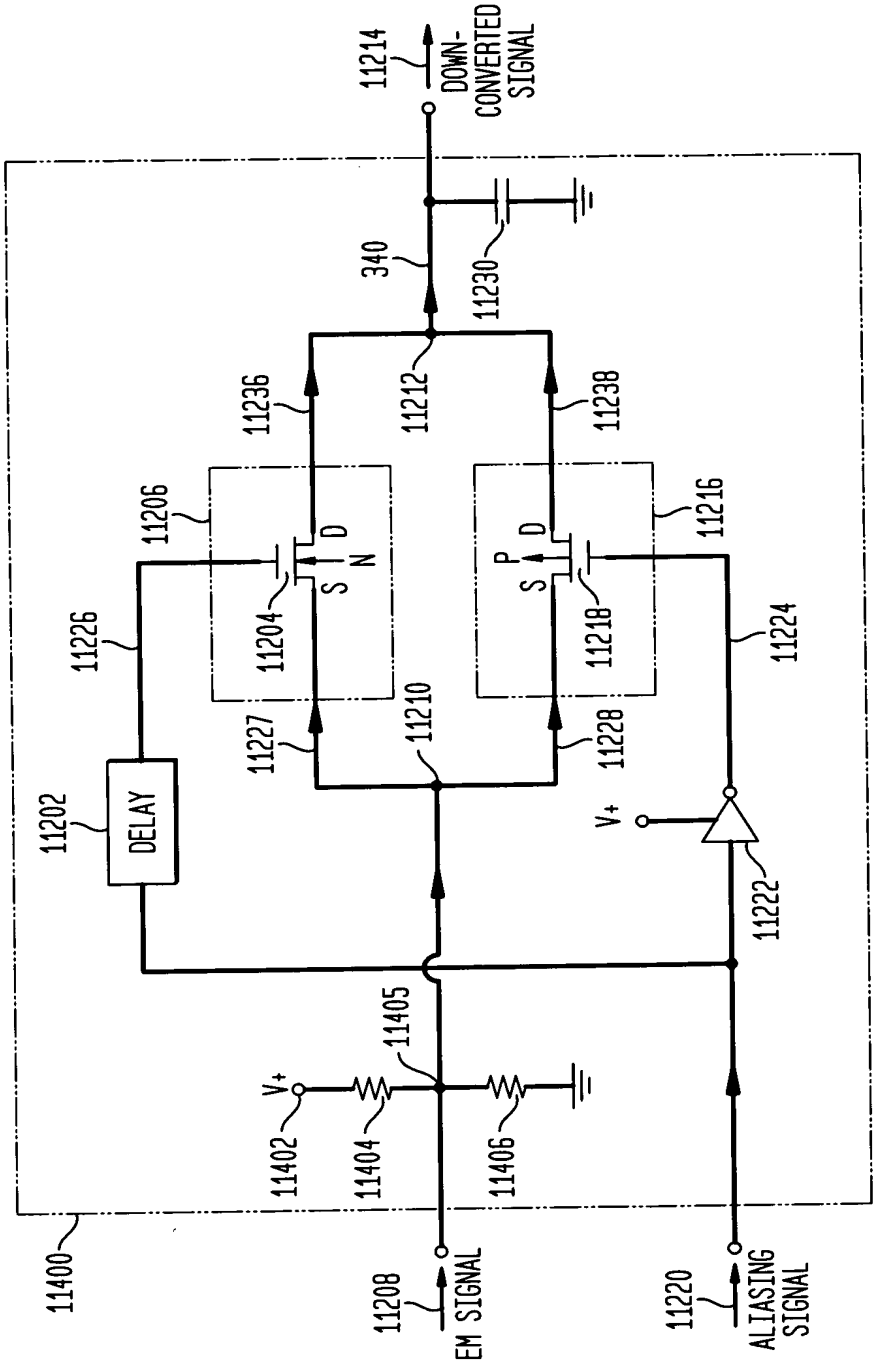

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FIG. 115

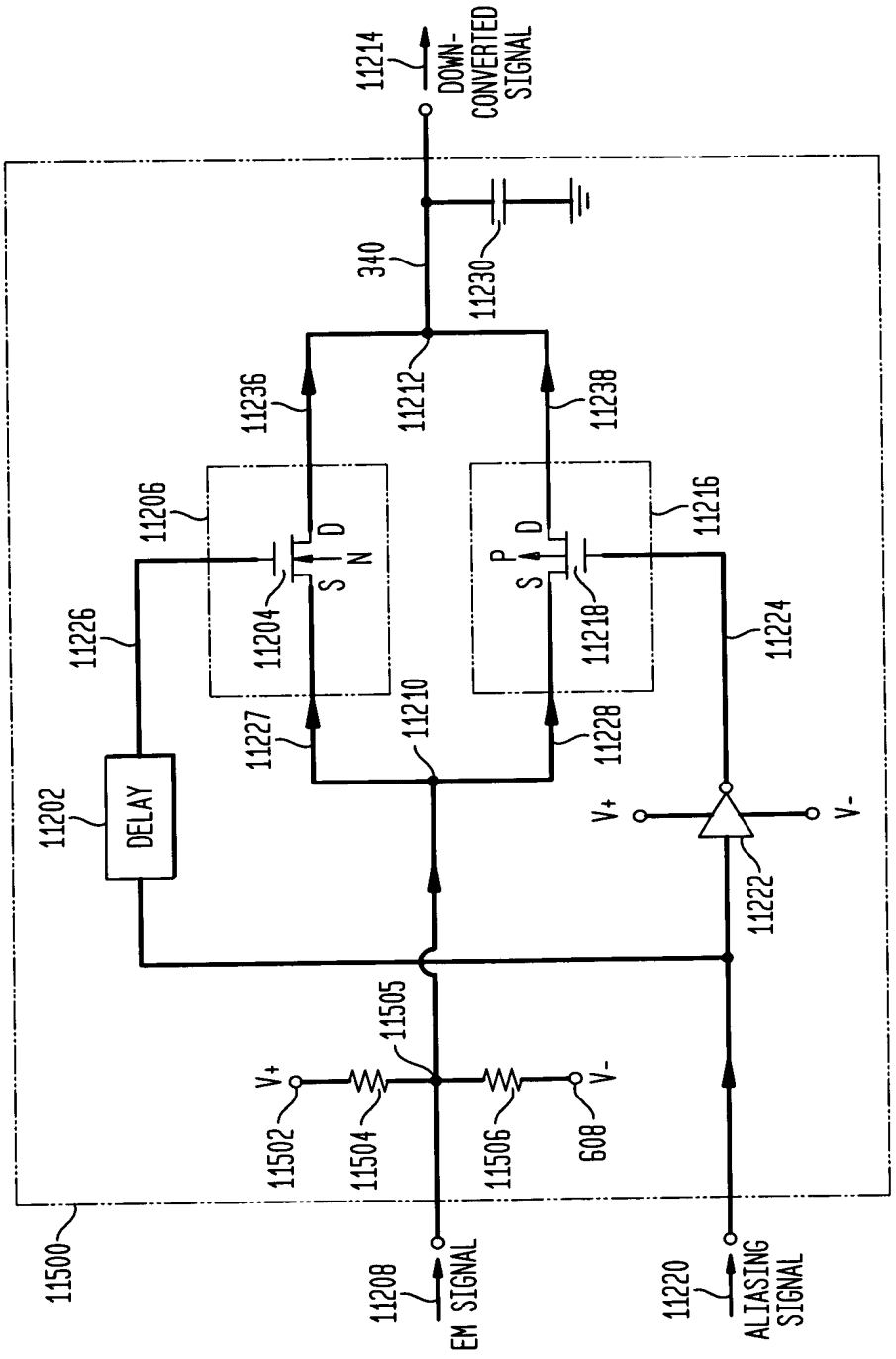


FIG. 116

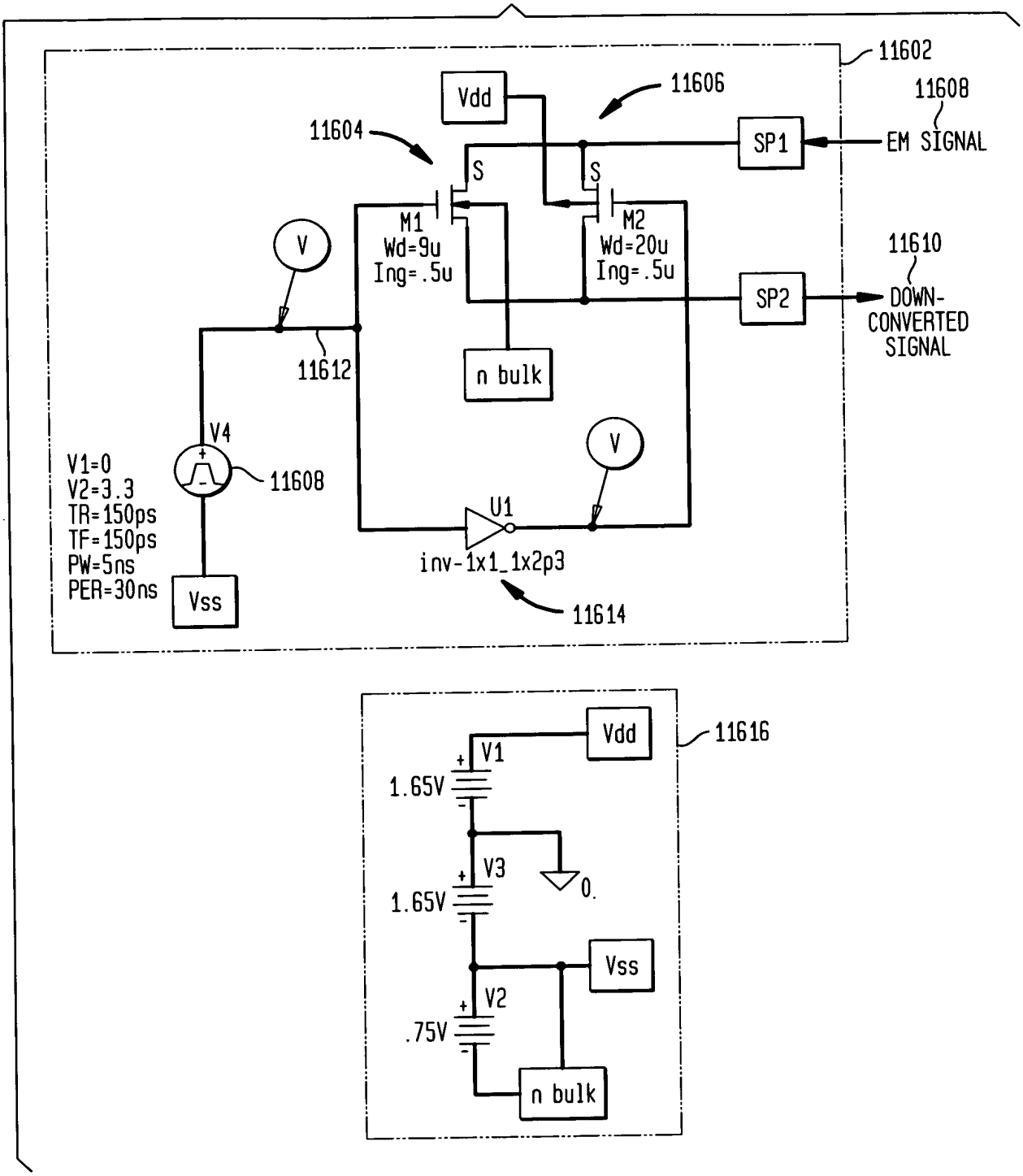
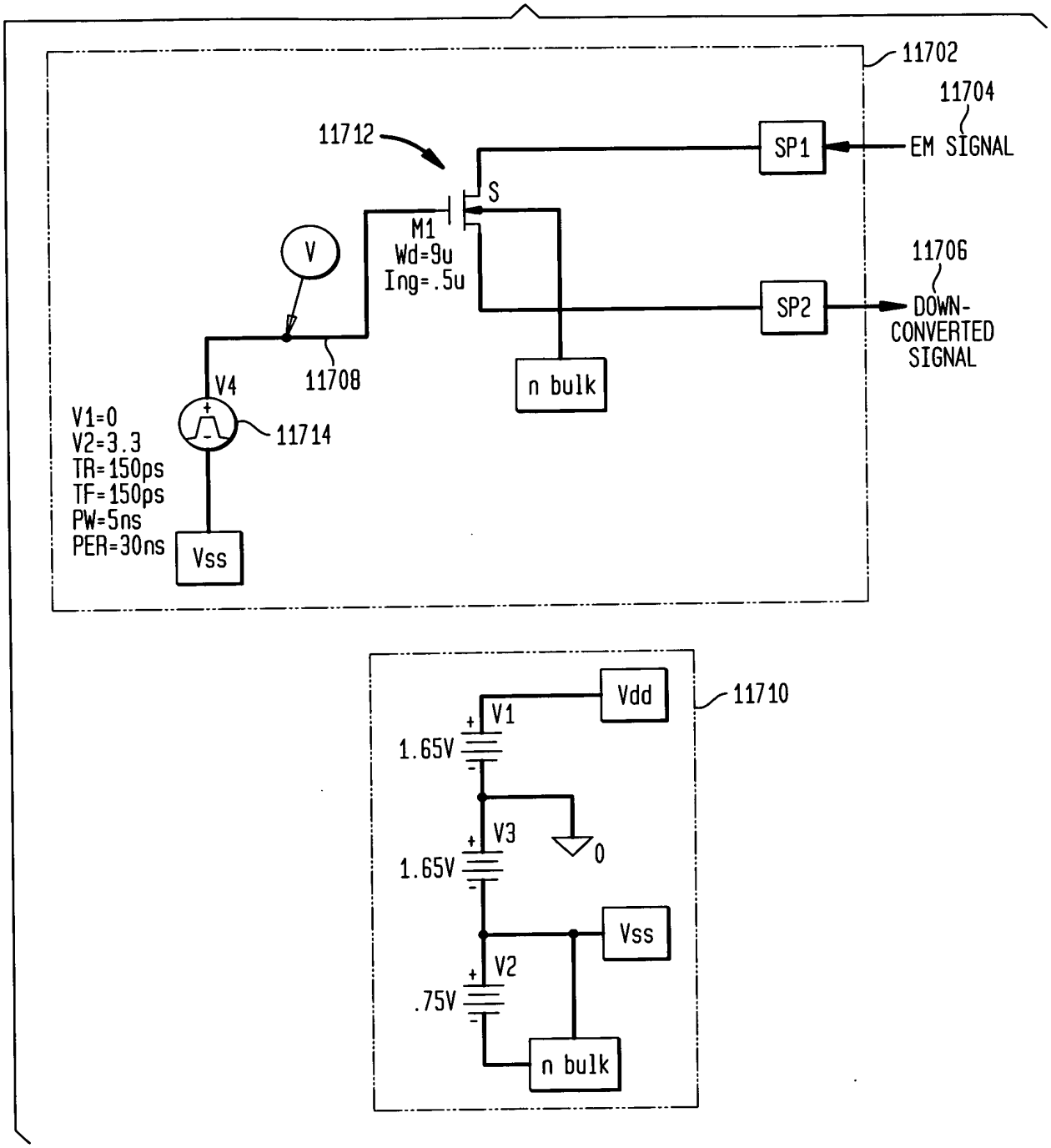
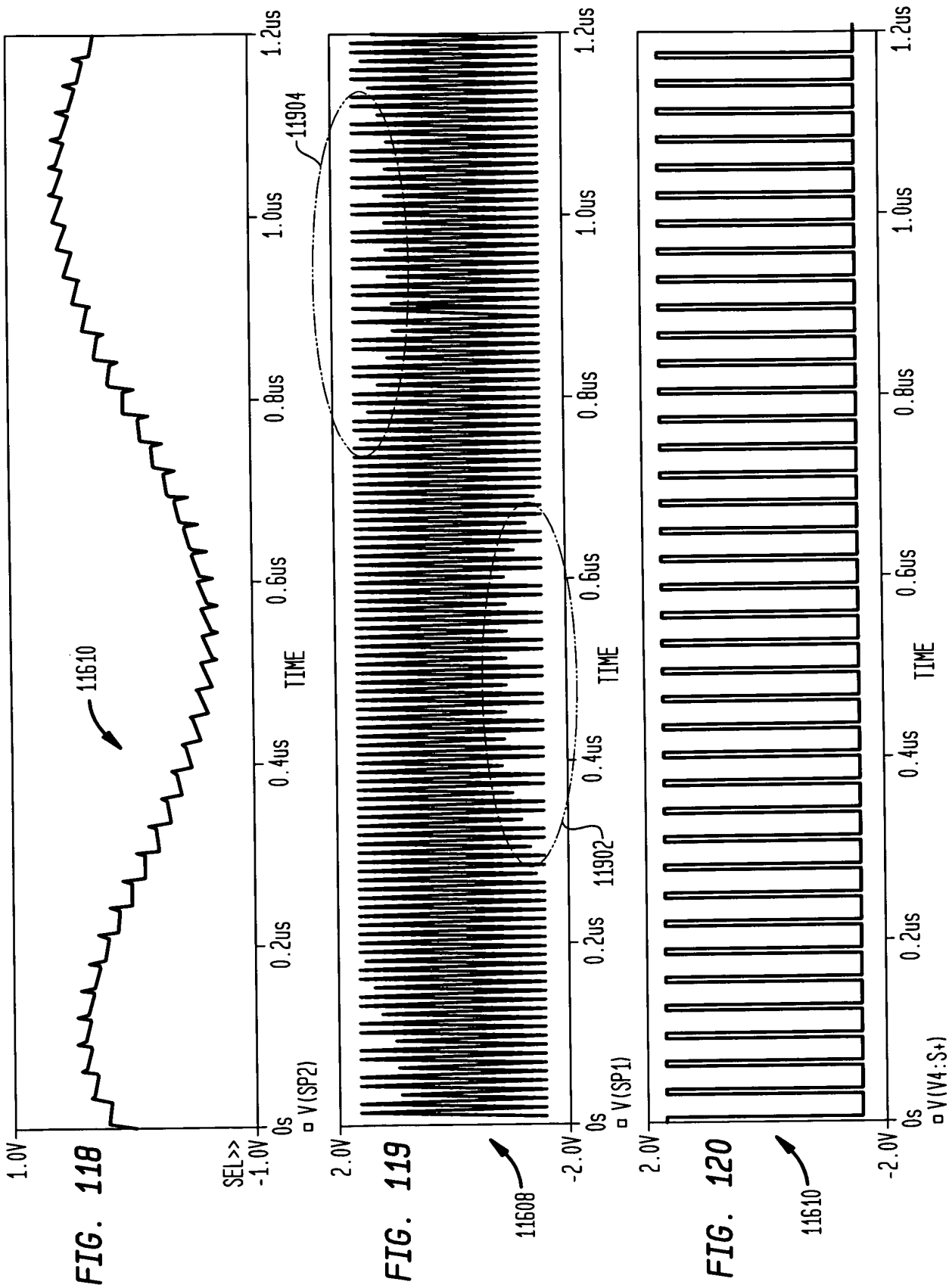

11602
11606
11608
11604
Vdd
SP1
EM SIGNAL
S
S
M1
Wd=9u
Lng=.5u
M2
Wd=20u
Lng=.5u
V
11610
SP2
DOWN-
CONVERTED
SIGNAL
11612
n bulk
V4
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=5ns
PER=30ns
11608
V
U1
inv-1x1_1x2p3
Vss
11614
11616
Vdd
V1
1.65V
V3
1.65V
0.
Vss
V2
.75V
n bulk

FIG. 117


11702
11704
EM SIGNAL
11712
SP1
S
M1
Wd=9u
Lng=.5u
V
11706
SP2
DOWN-
CONVERTED
SIGNAL
n bulk
11708
V4
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=5ns
PER=30ns
11714
Vss
11710
Vdd
V1
1.65V
V3
1.65V
0
Vss
V2
.75V
n bulk


1.0V
SEL>>
-1.0V
11610
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
TIME
V(SP2)
FIG. 118
2.0V
-2.0V
11904
11902
11608
V(SP1)
FIG. 119
11610
V(V4:S+)
FIG. 120

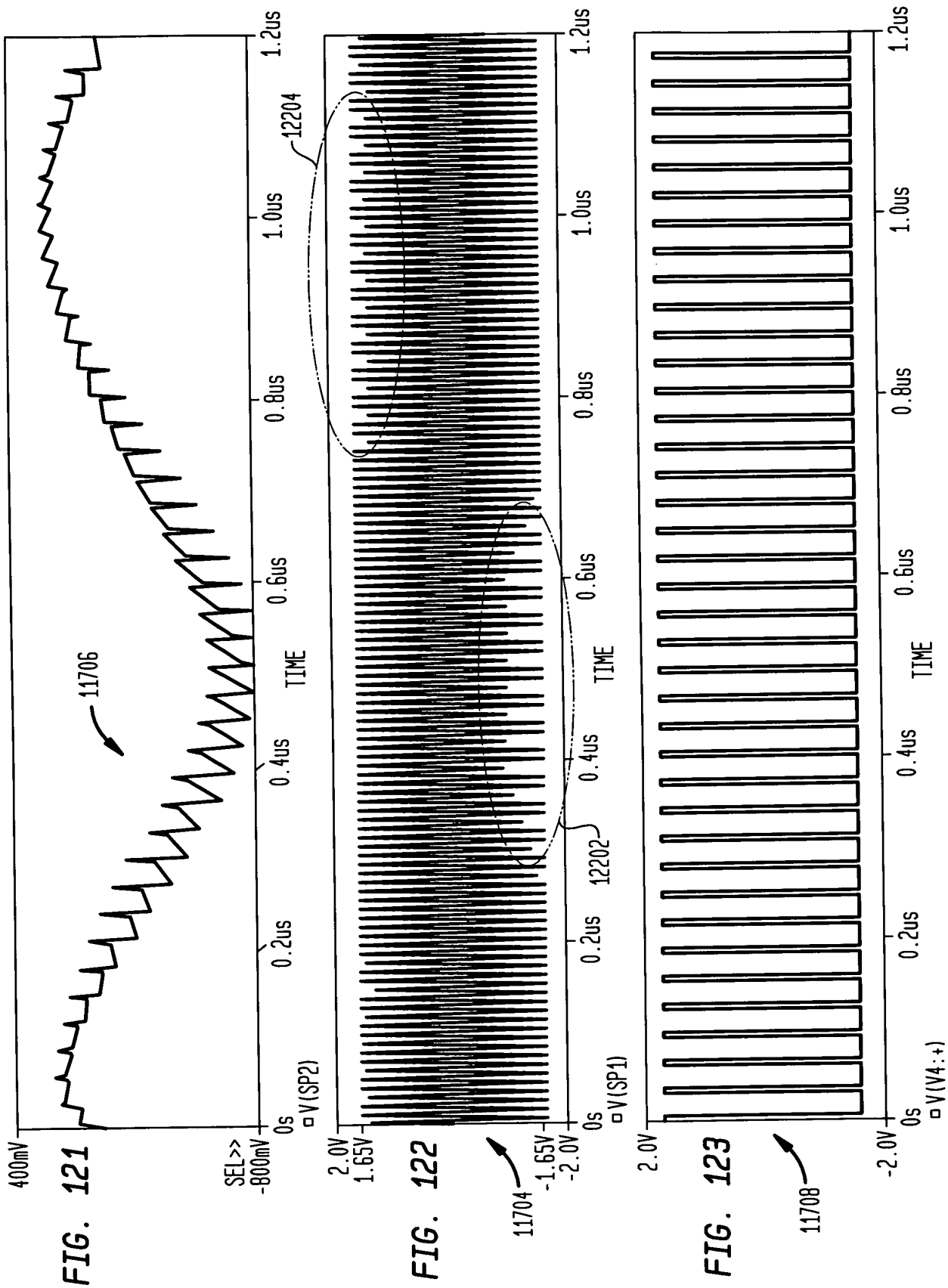

400mV
SEL>>
-800mV
11706
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
TIME
V(SP2)
FIG. 121
2.0V
1.65V
-1.65V
-2.0V
12204
12202
11704
V(SP1)
FIG. 122
2.0V
-2.0V
11708
V(V4:+)
FIG. 123

FIG. 124A

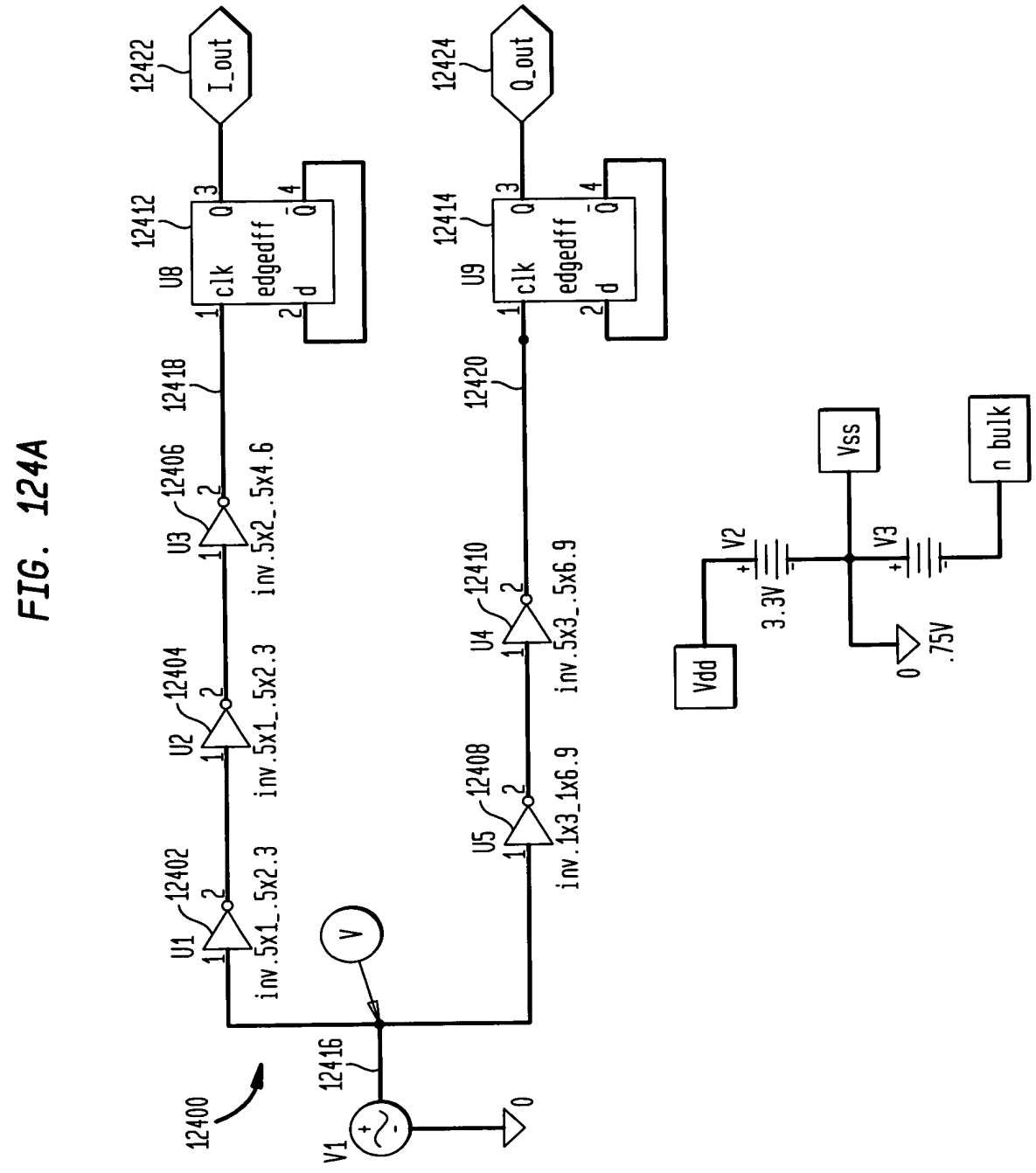

12422
I_out
12424
Q_out
12412
U8
clk
edgedff
d
Q
12414
U9
12418
12420
U3
12406
inv.5x2_.5x4.6
U4
12410
inv.5x3_.5x6.9
U2
12404
inv.5x1_.5x2.3
U5
12408
inv.1x3_1x6.9
U1
12402
inv.5x1_.5x2.3
V
12416
V1
12400
0
Vdd
V2
3.3V
Vss
V3
.75V
n bulk

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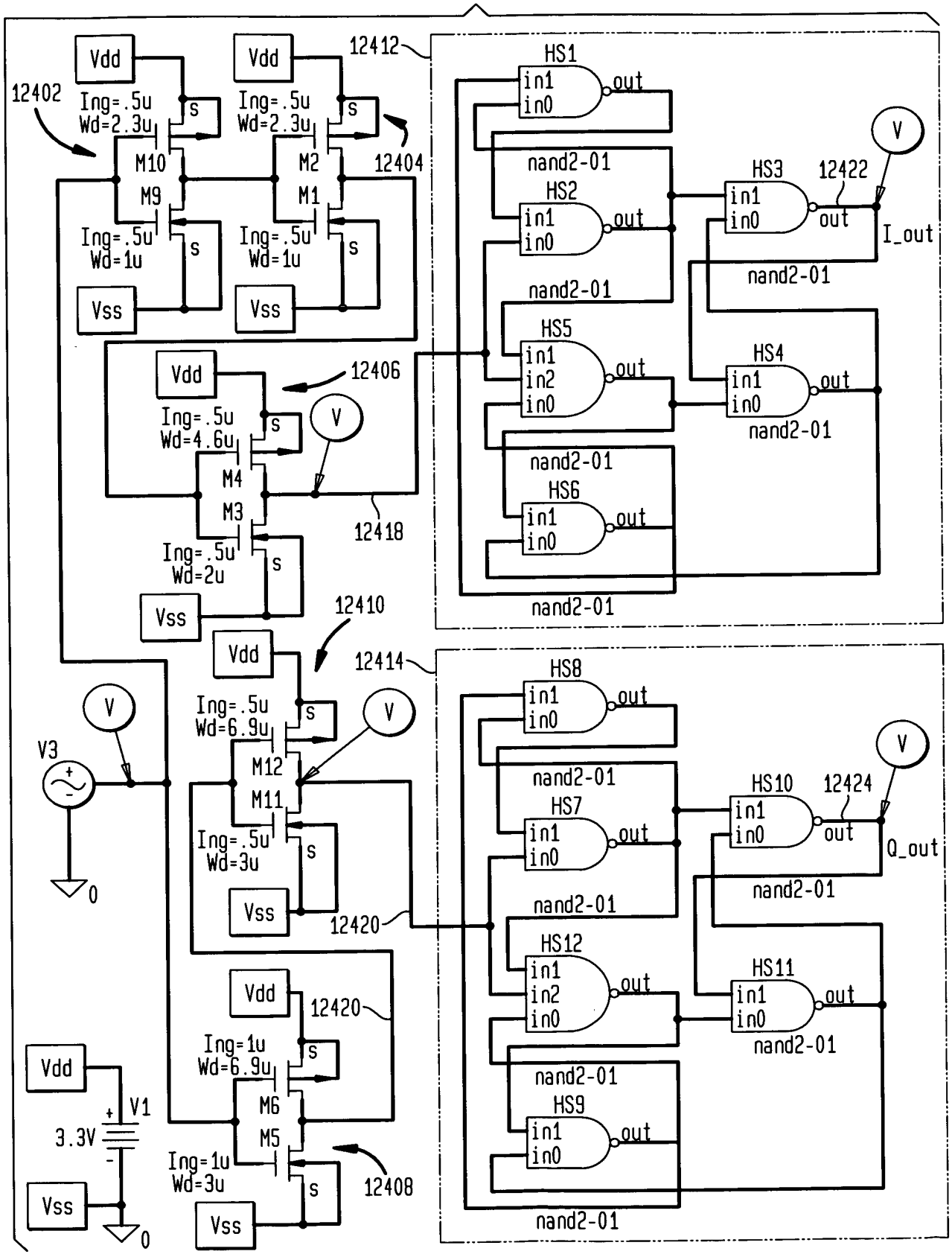
FIG. 124B



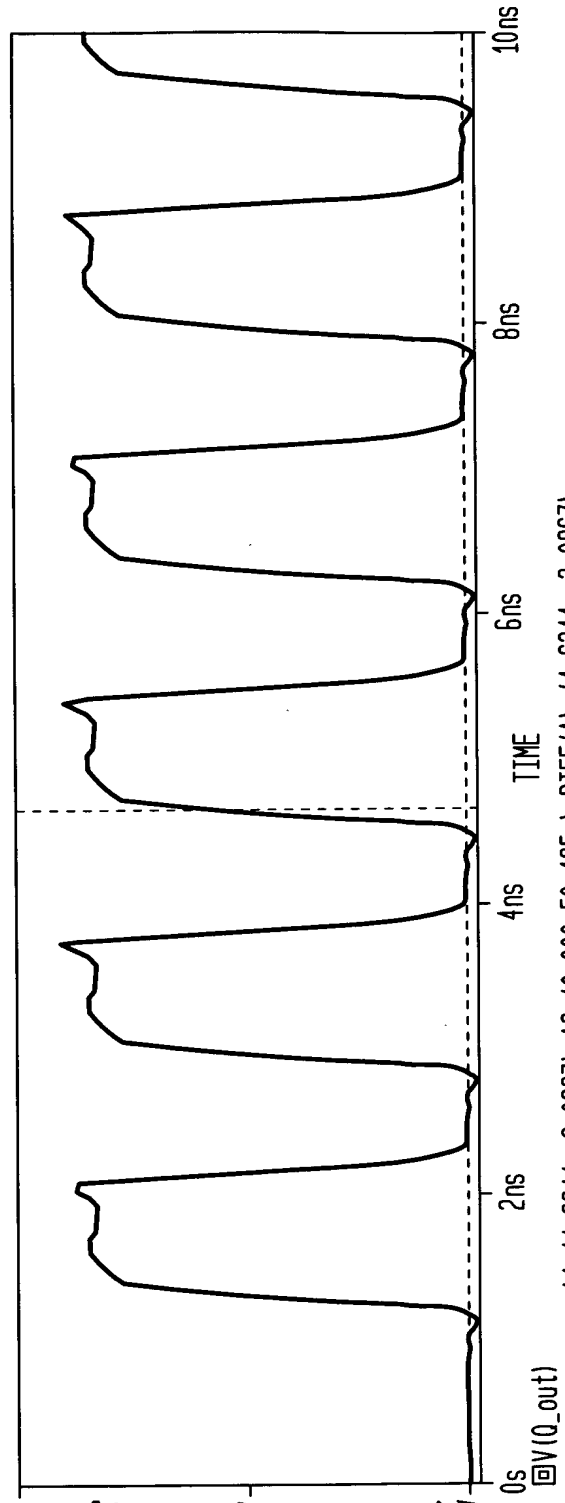



FIG. 124C

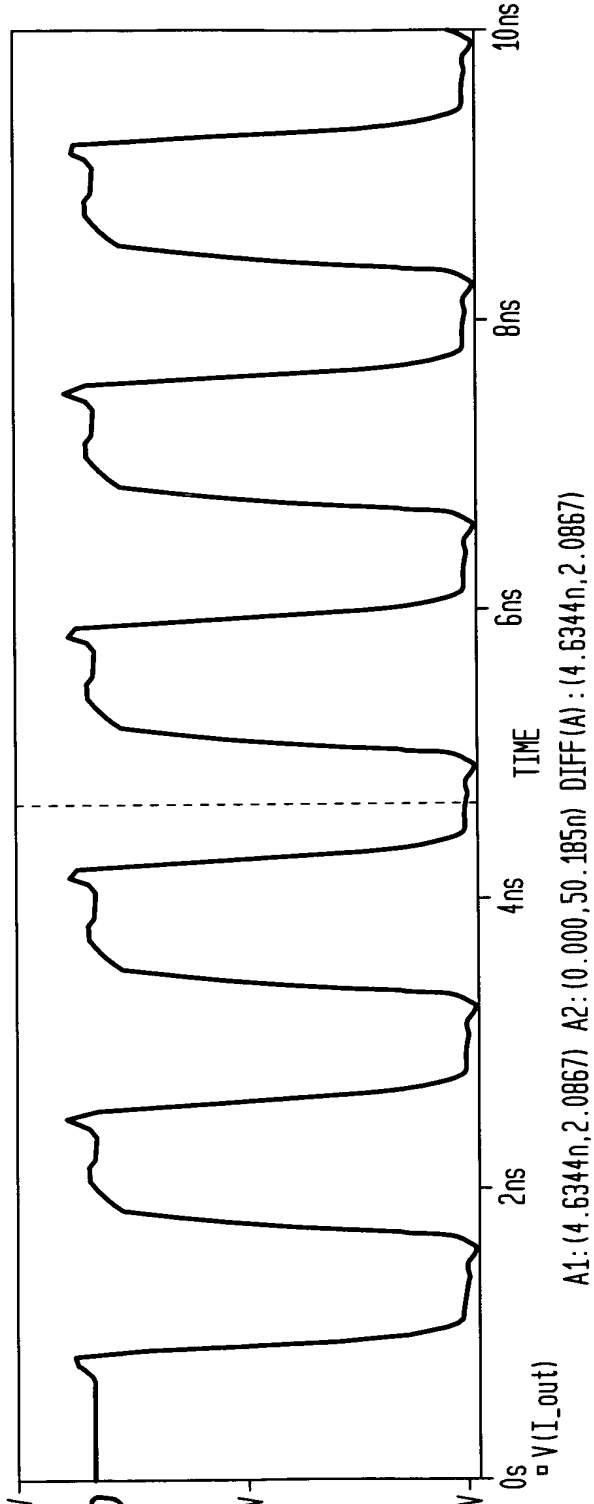



FIG. 124D

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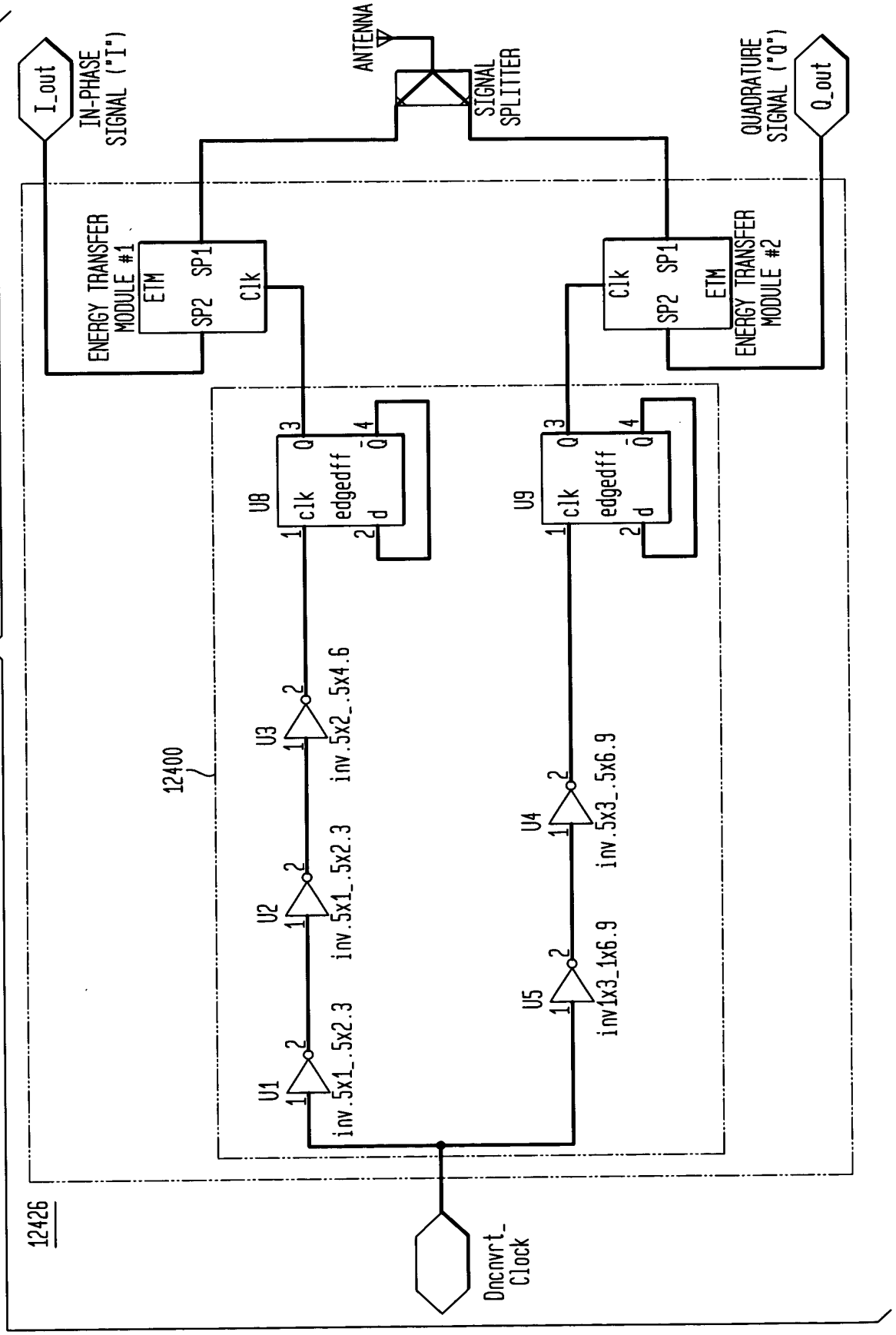


FIG. 124E

FIG. 124F

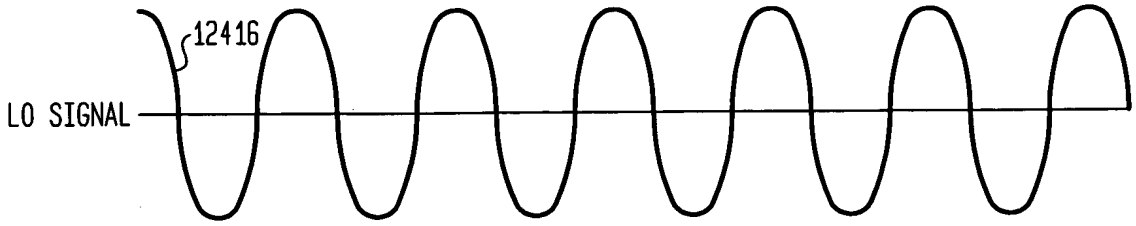


FIG. 124G

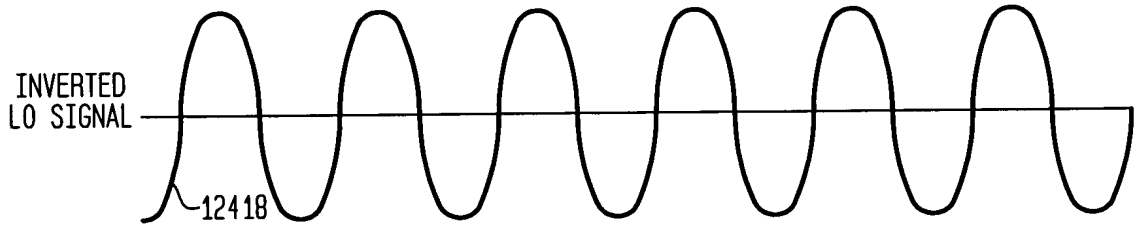


FIG. 124H

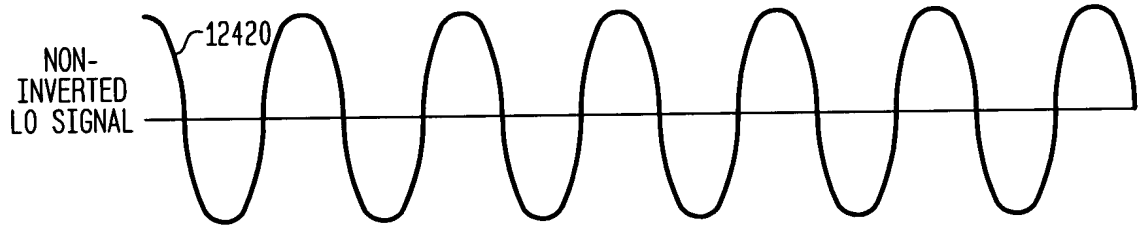


FIG. 124I

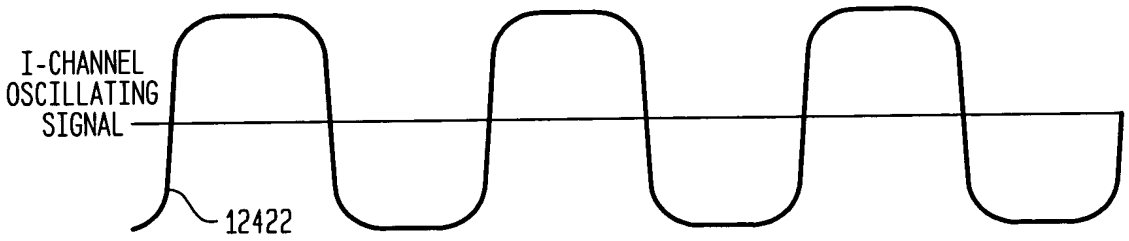


FIG. 124J

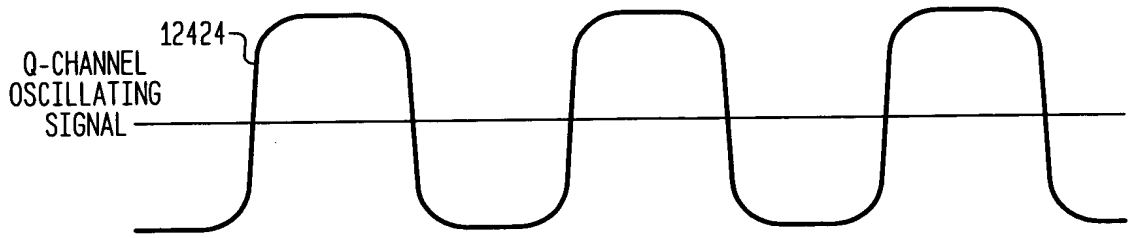

FIG. 125

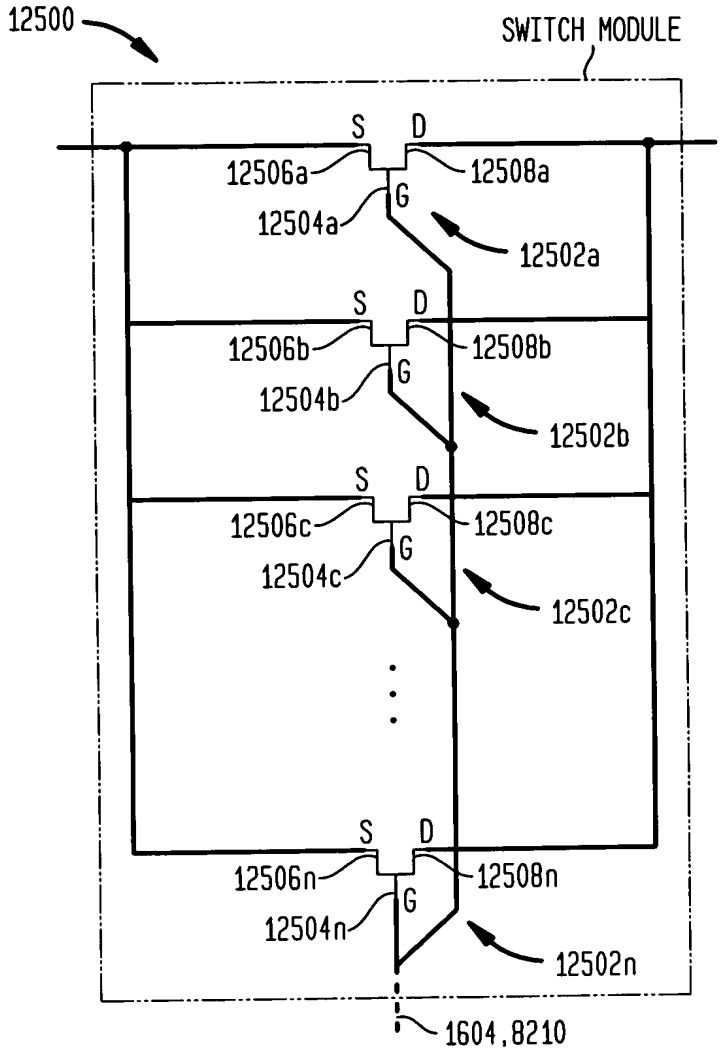
12500
SWITCH MODULE
S
D
12506a
12508a
G
12504a
12502a
S
D
12506b
12508b
G
12504b
12502b
S
D
12506c
12508c
G
12504c
12502c
S
D
12506n
12508n
G
12504n
12502n
1604, 8210

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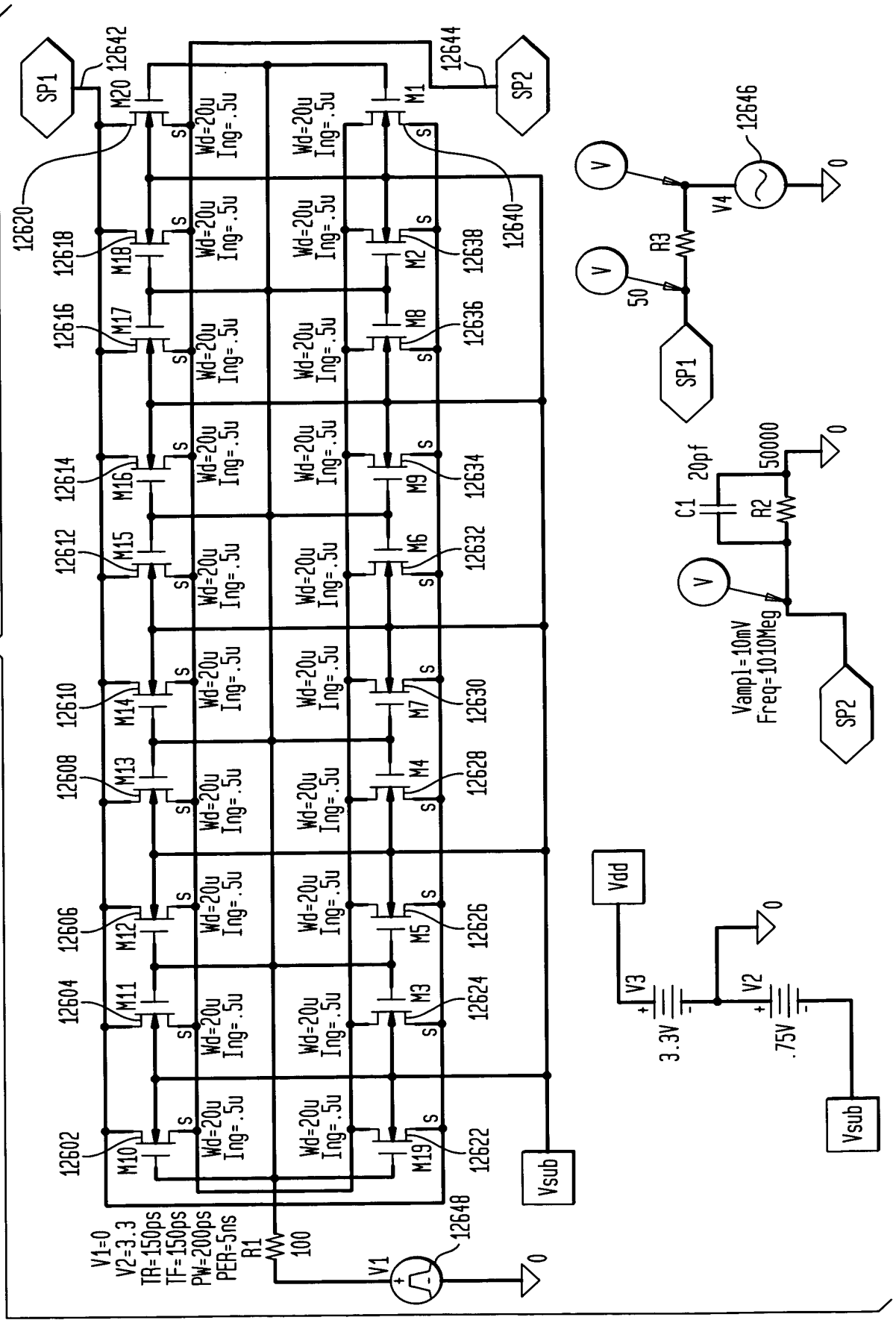
FIG. 126A



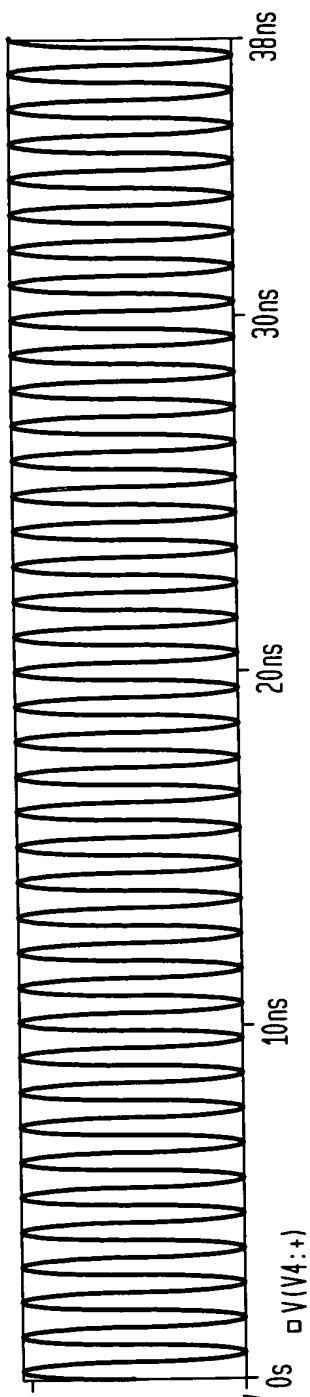



FIG. 126B

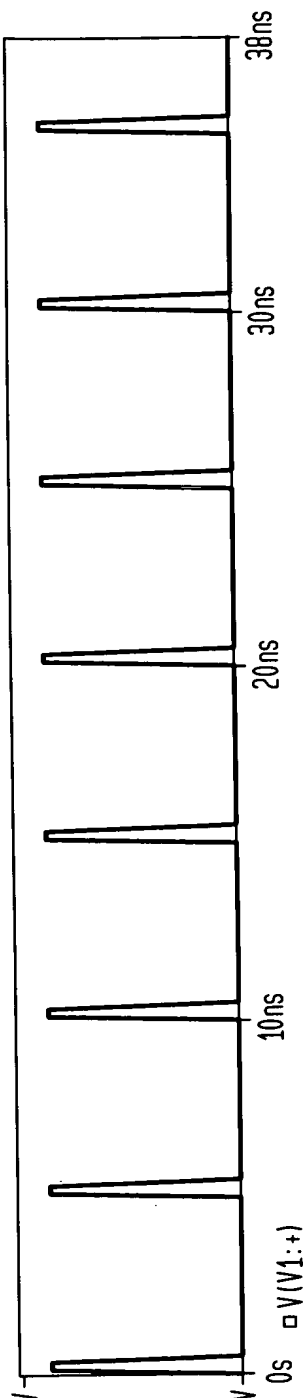



FIG. 126C

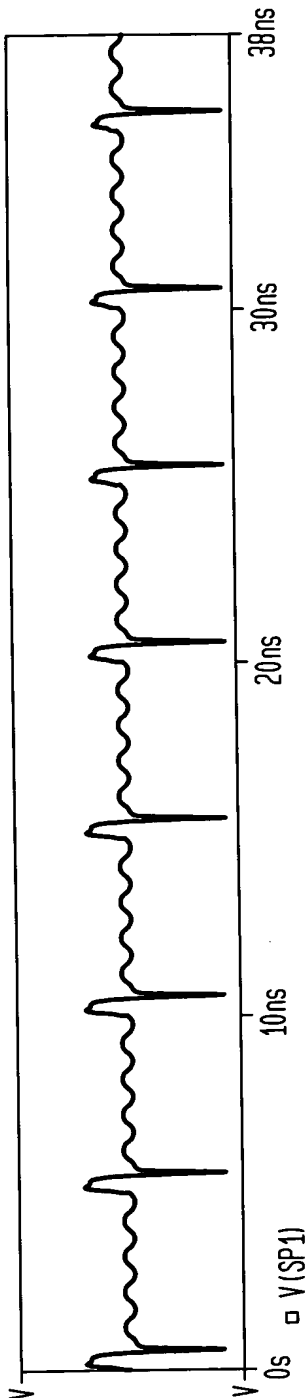



FIG. 126D

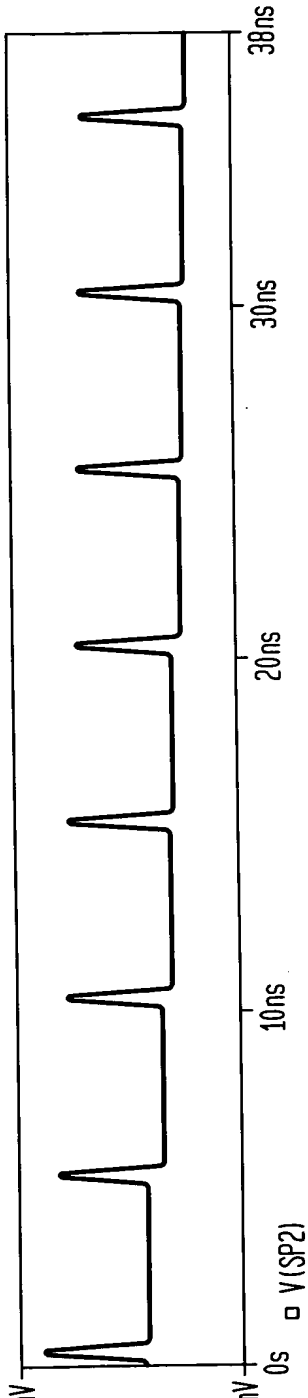



FIG. 126E

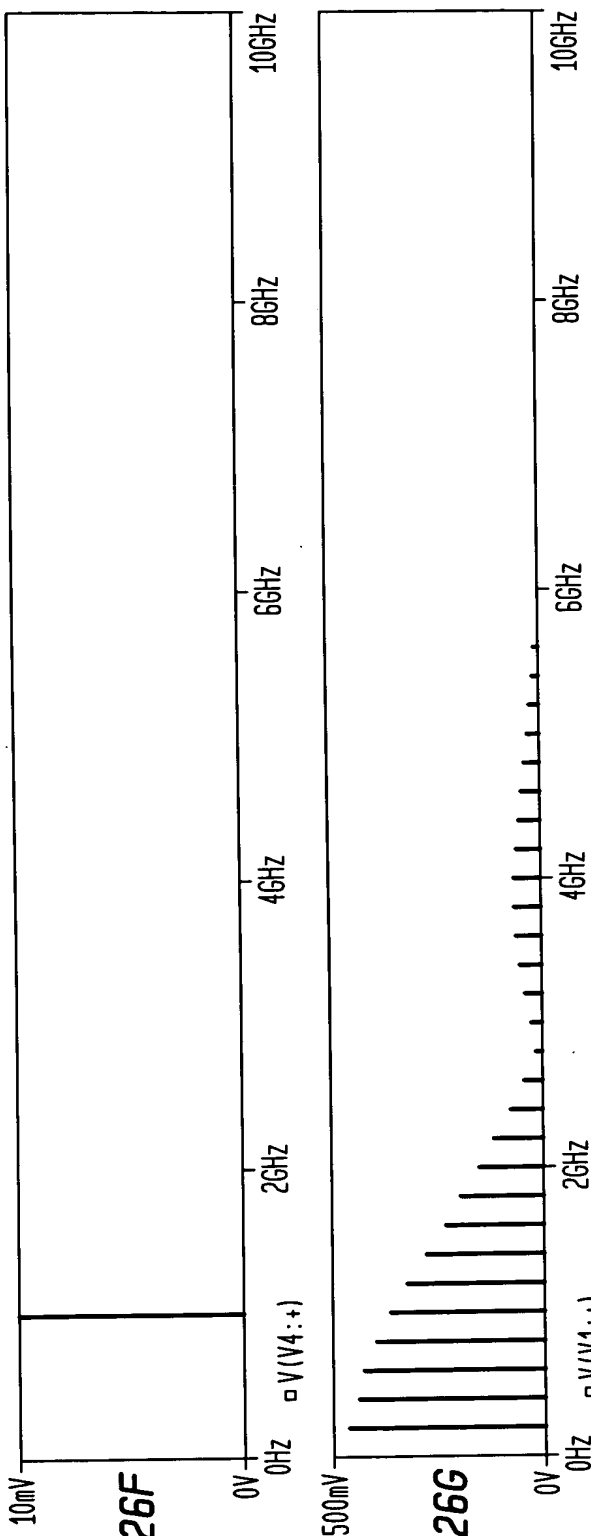



FIG. 126F




FIG. 126G

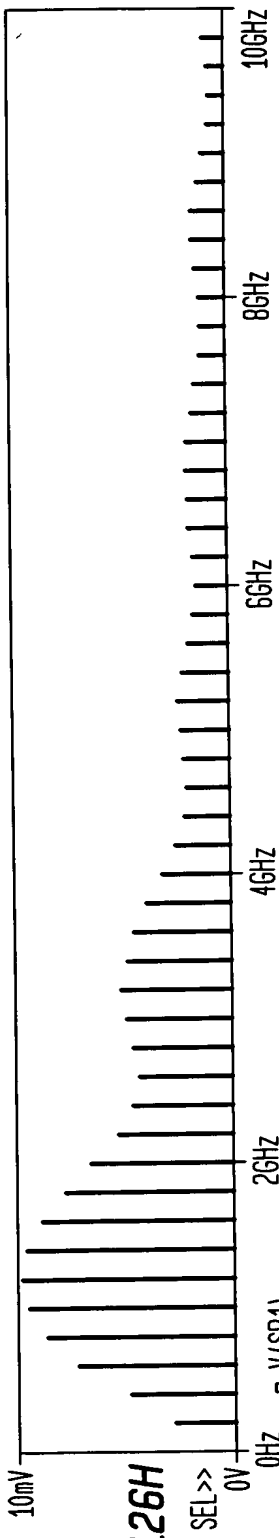



FIG. 126H

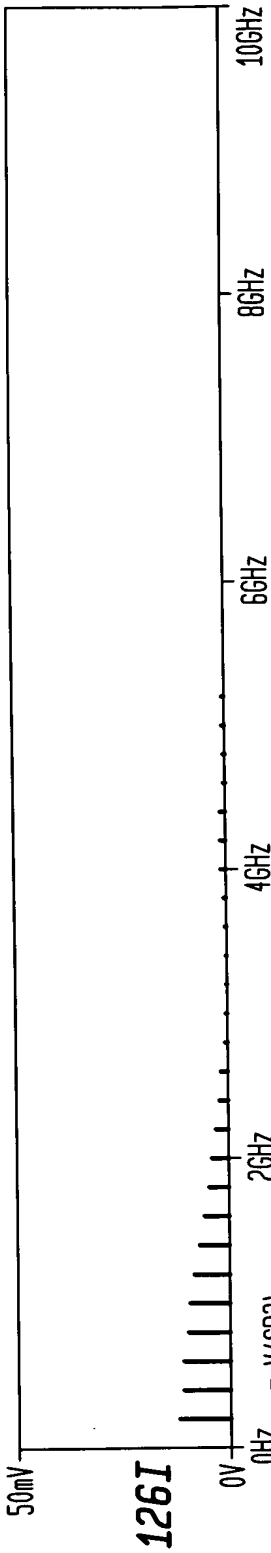



FIG. 126I

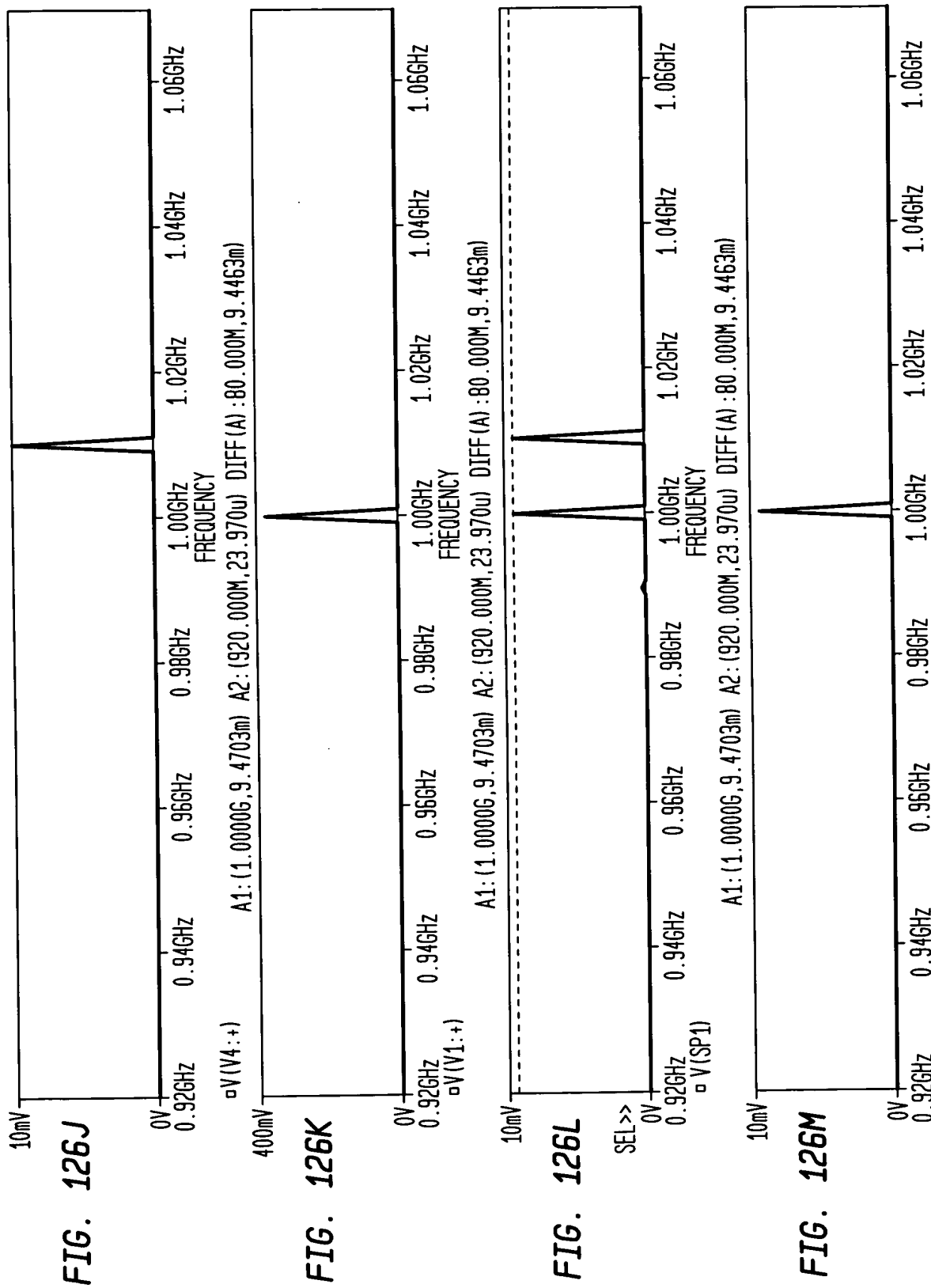



FIG. 126J

FIG. 126K

FIG. 126L

FIG. 126M

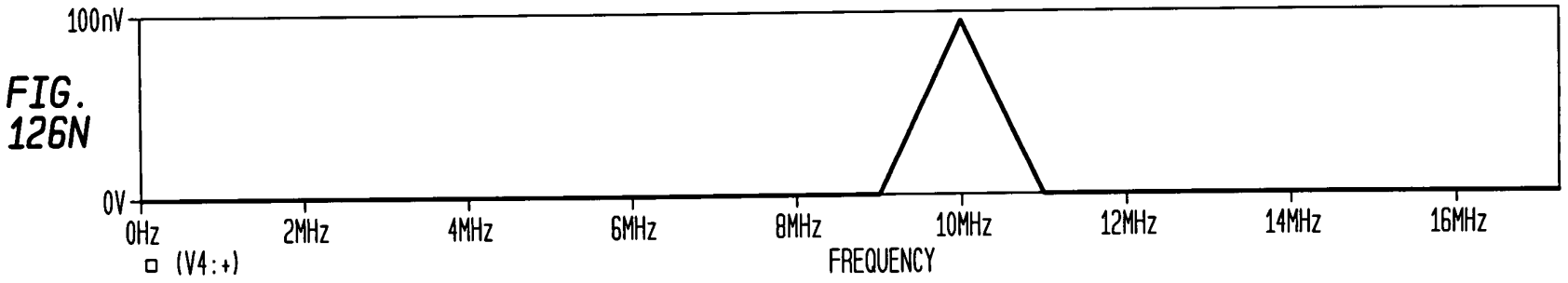



FIG. 126N

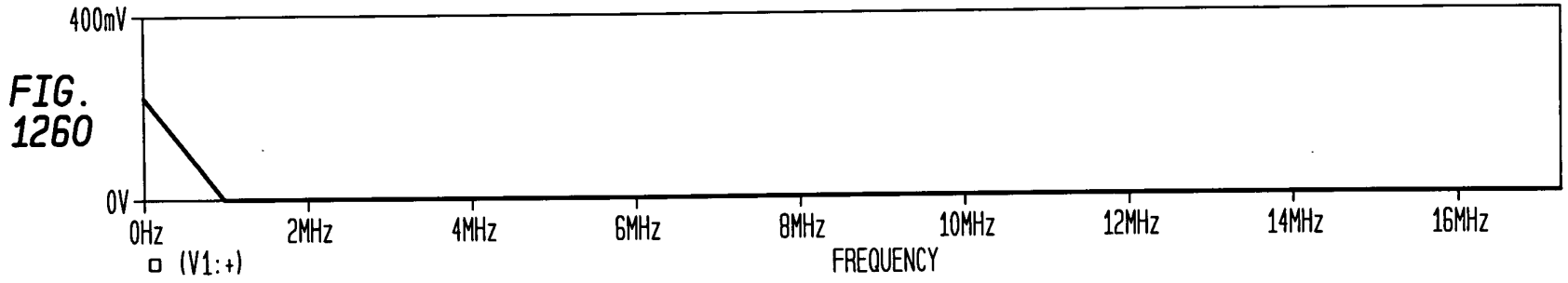



FIG. 126O

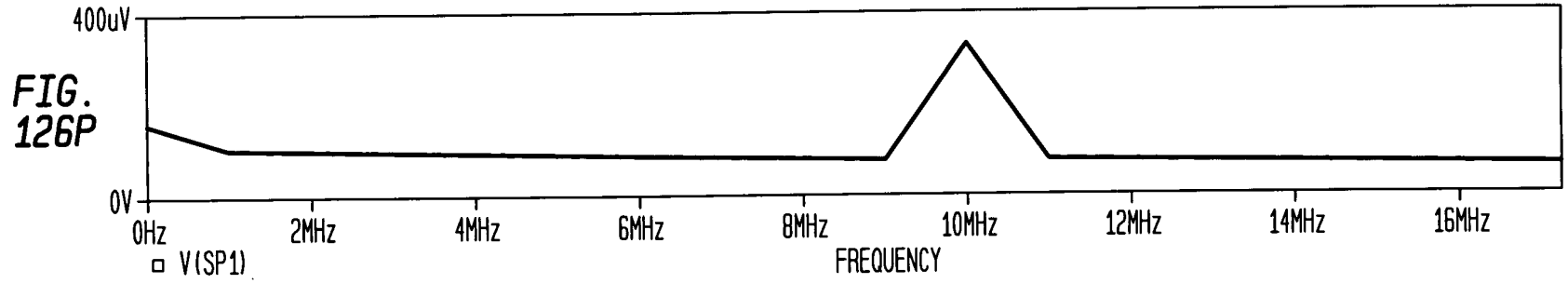



FIG. 126P

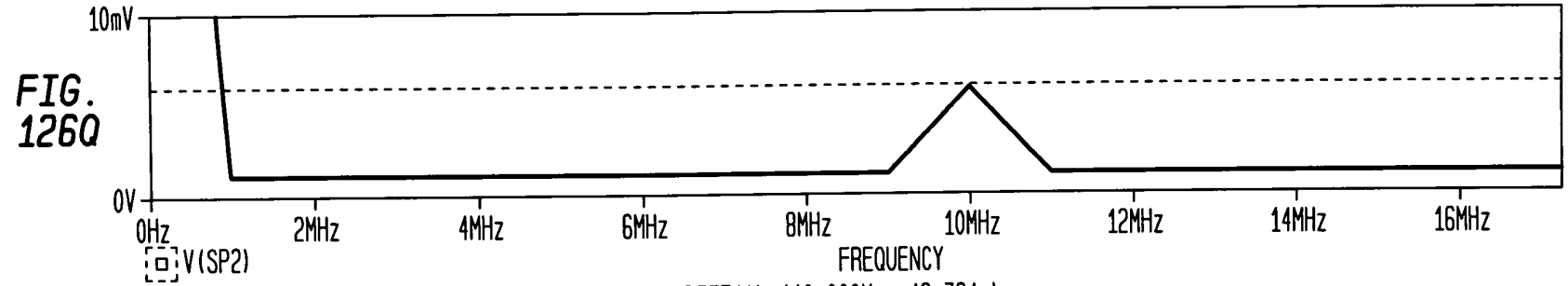



FIG. 126Q

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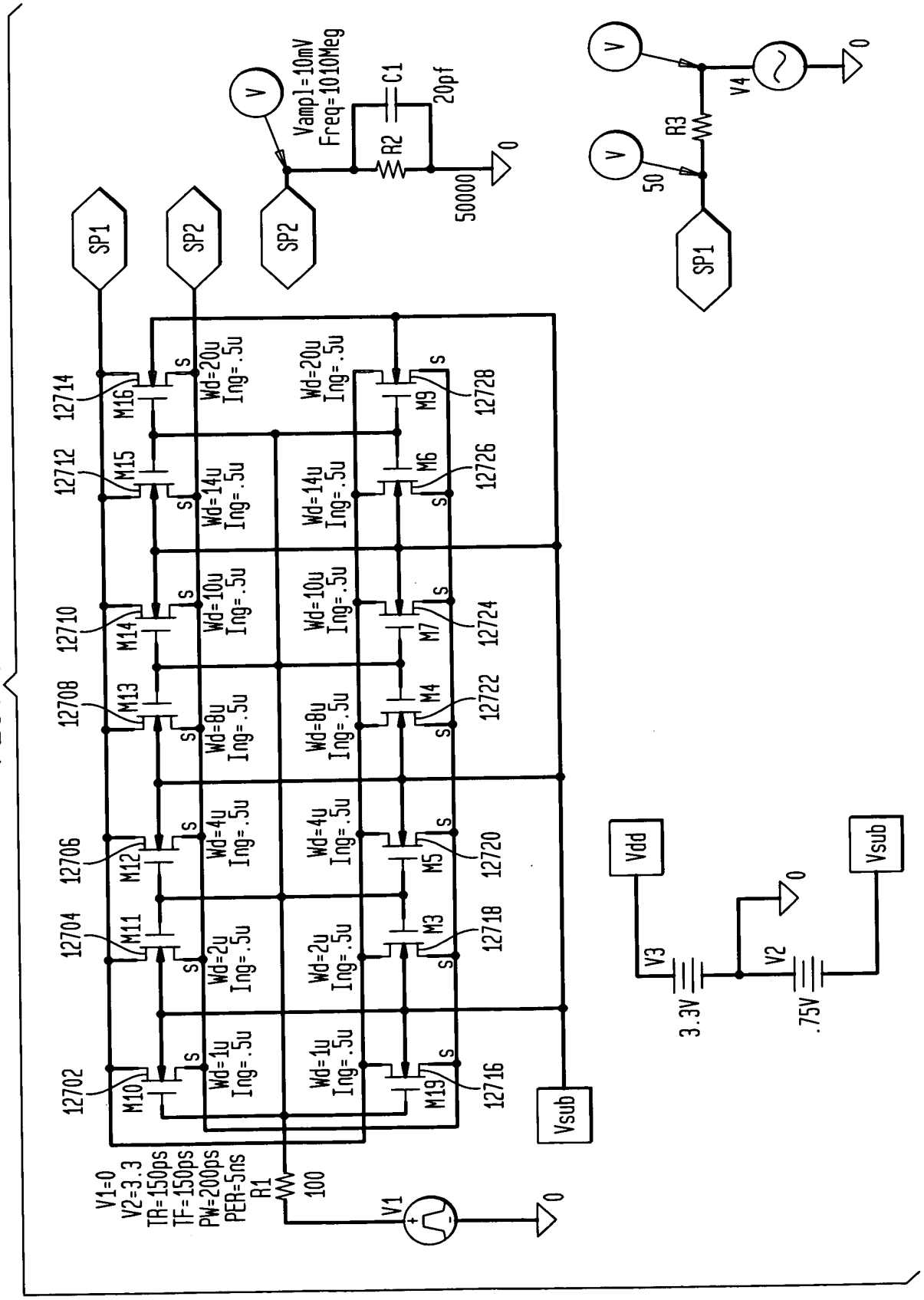
Dkt No. 1744.092000I; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

FIG. 127A


SP1
SP2
SP2
V
Vampl=10mV
Freq=1010Meg
C1
20pf
R2
50000
0
V
V
50
R3
V4
0
SP1
12714
M16
12712
M15
12710
M14
12708
M13
12706
M12
12704
M11
12702
M10
Wd=20u
Lng=.5u
Wd=14u
Lng=.5u
Wd=10u
Lng=.5u
Wd=8u
Lng=.5u
Wd=4u
Lng=.5u
Wd=2u
Lng=.5u
Wd=1u
Lng=.5u
M9
12728
M6
12726
M7
12724
M4
12722
M5
12720
M3
12718
M19
12716
Vsub
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=200ps
PER=5ns
R1
100
V1
0
Vdd
V3
3.3V
0
V2
.75V
Vsub

Replacement Sheet
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Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

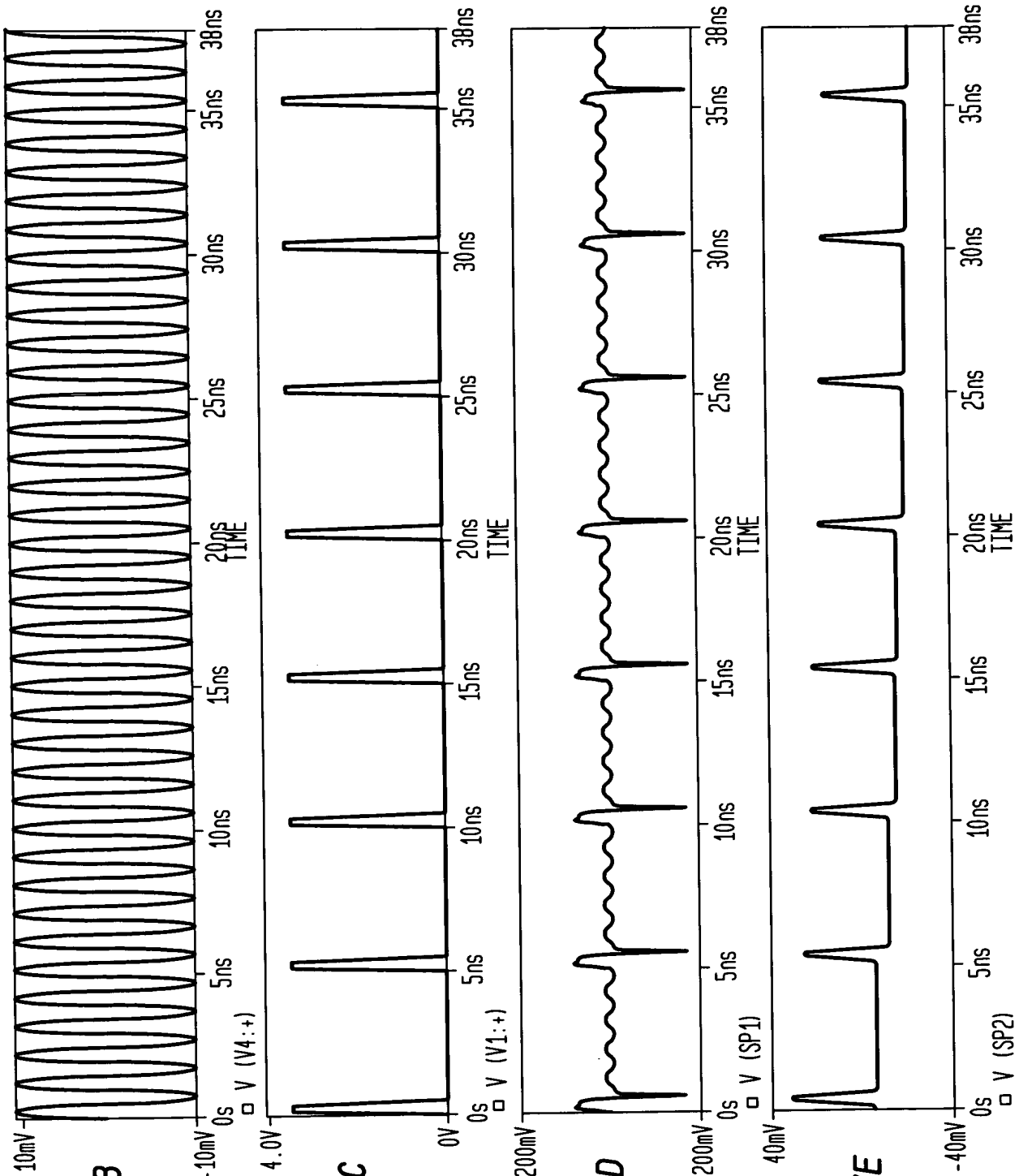


FIG. 127B

FIG. 127C

FIG. 127D

FIG. 127E

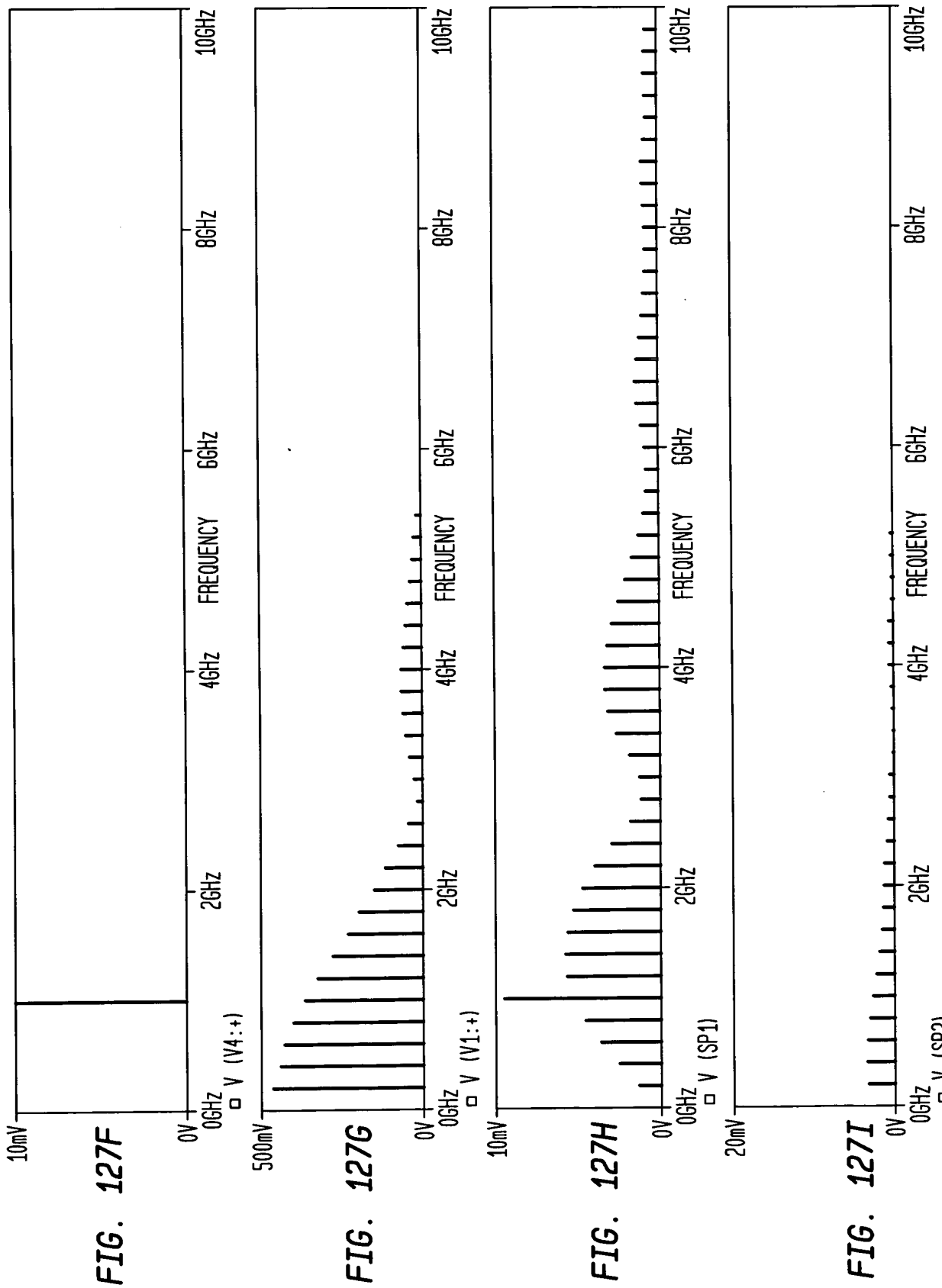


FIG. 127F

FIG. 127G

FIG. 127H

FIG. 127I

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Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
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For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

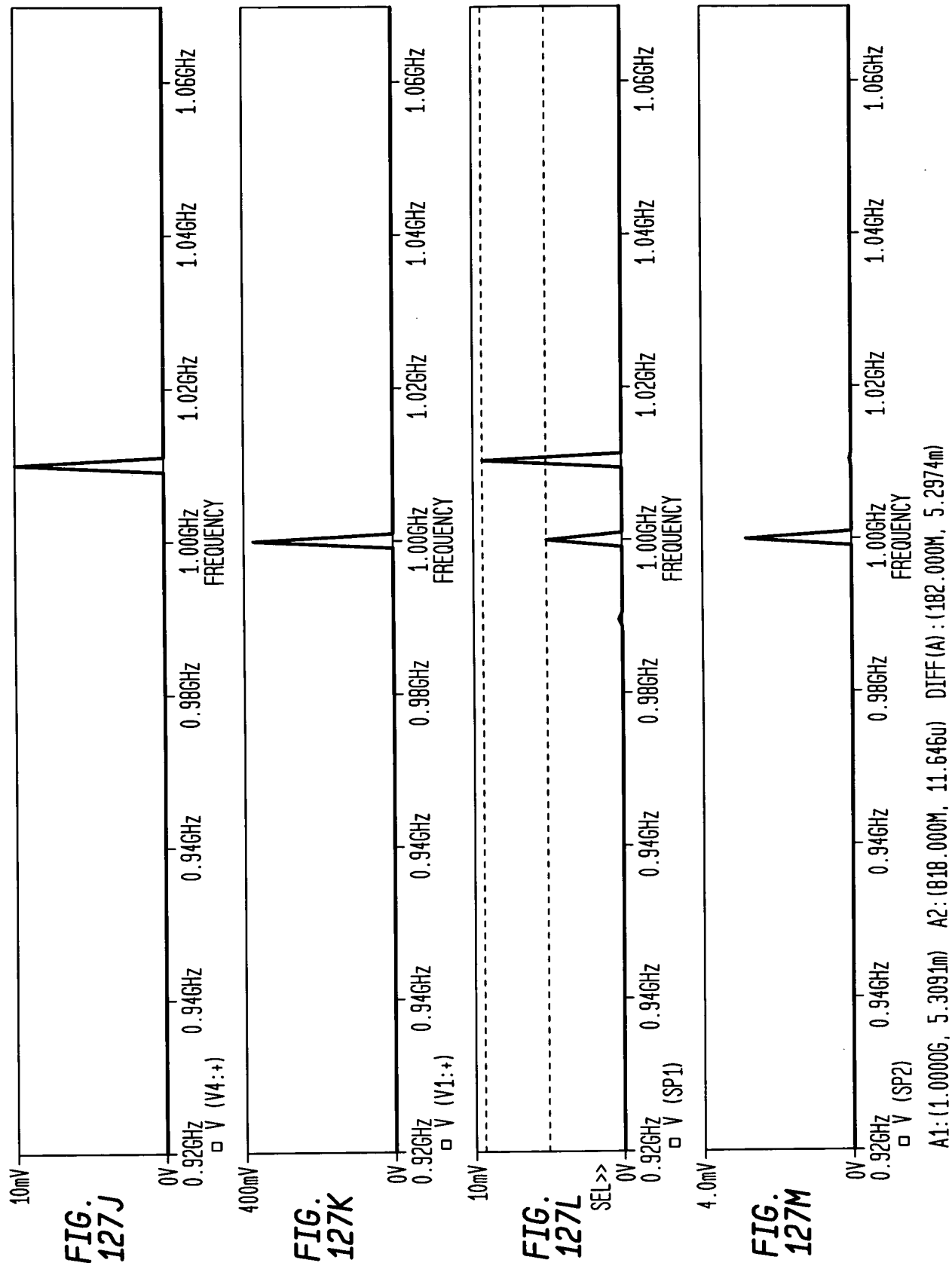



FIG. 127J

FIG. 127K

FIG. 127L

FIG. 127M

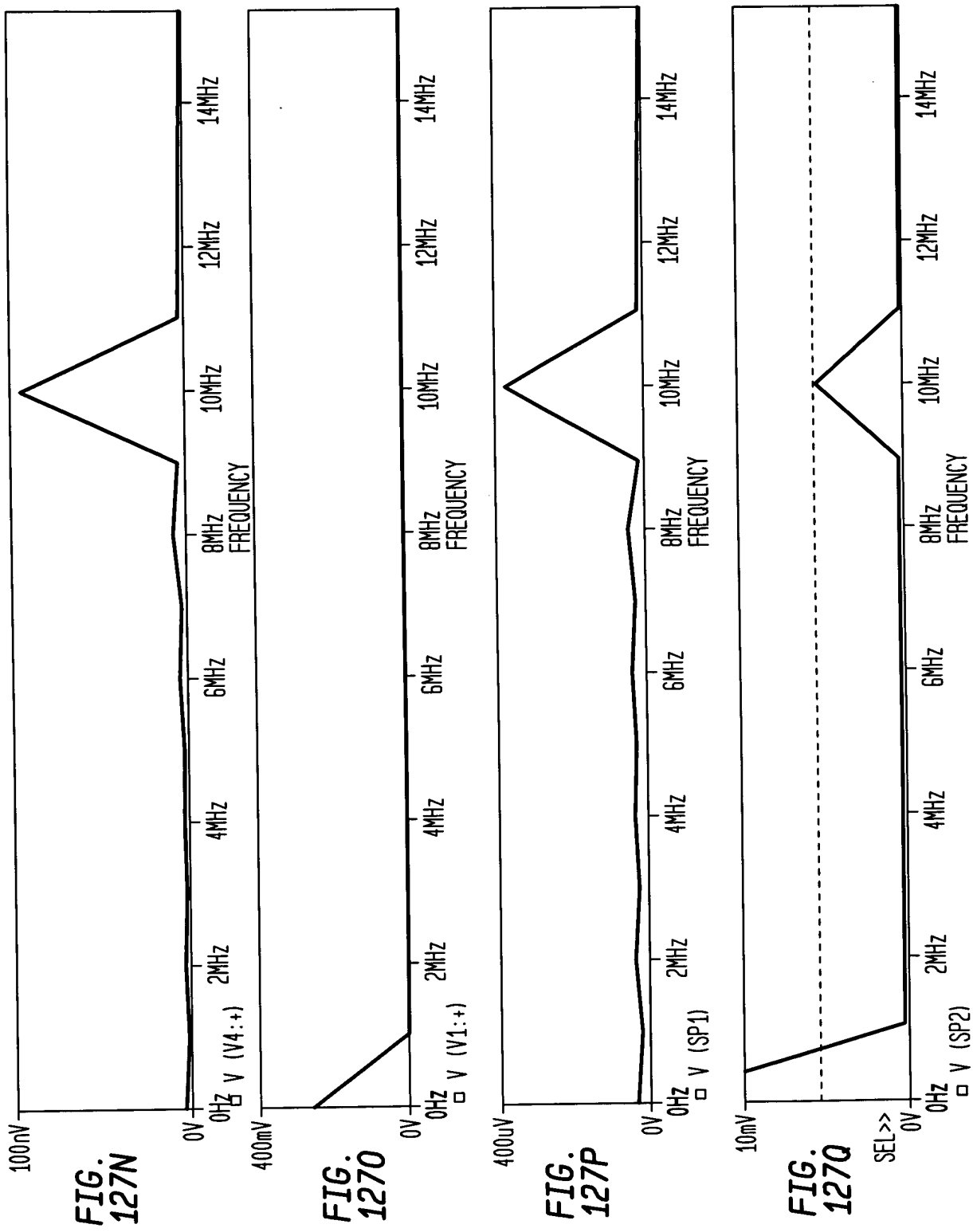



FIG. 127N

FIG. 127O

FIG. 127P

FIG. 127Q

FIG. 128A

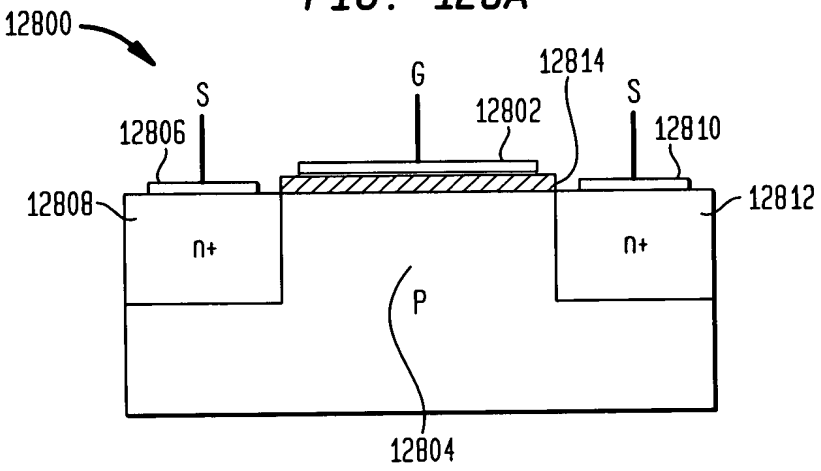



FIG. 128B

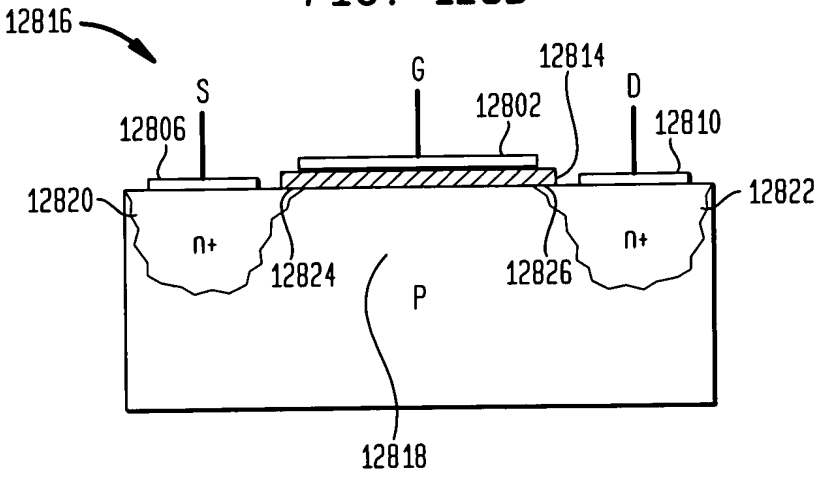


FIG. 128C

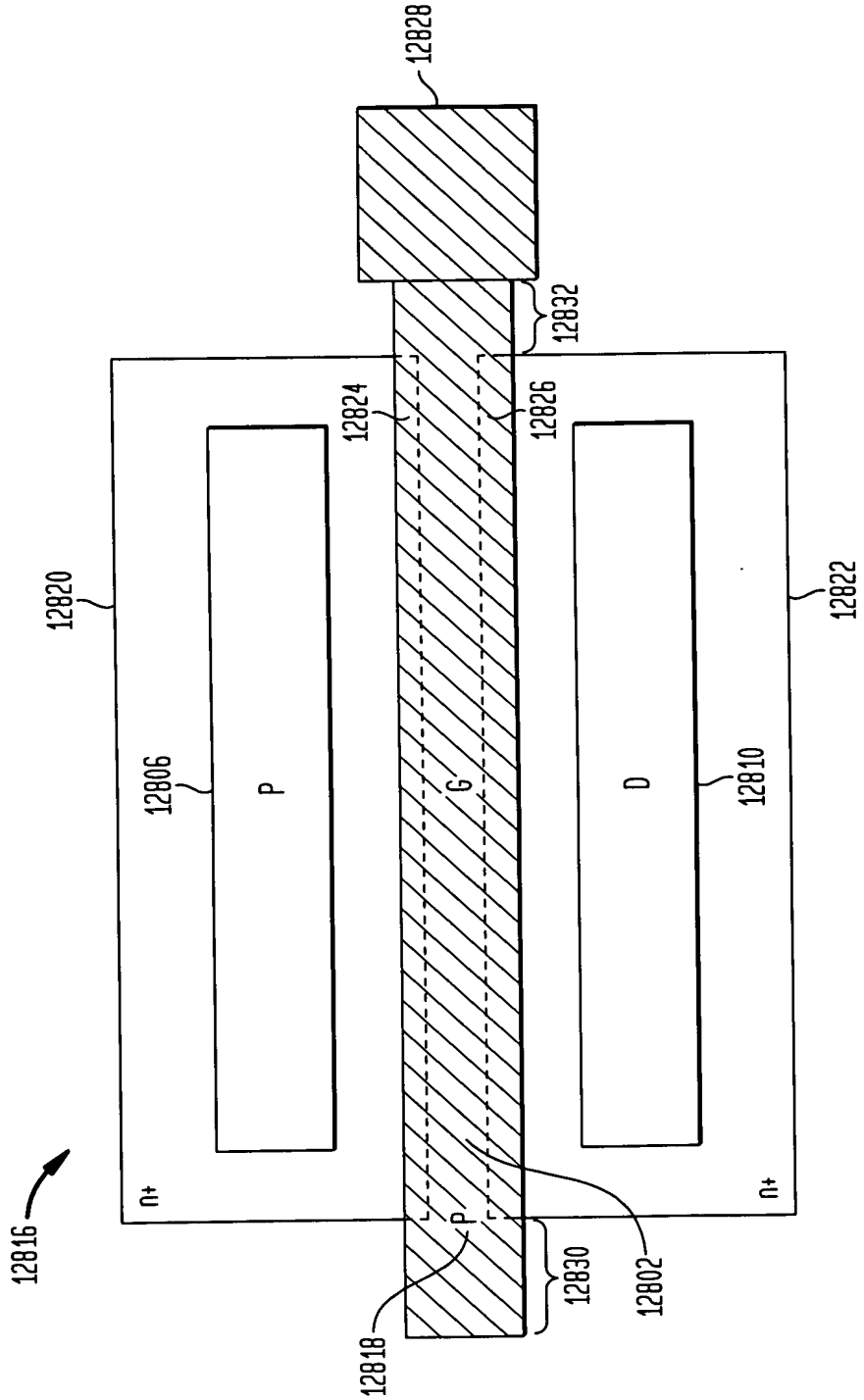
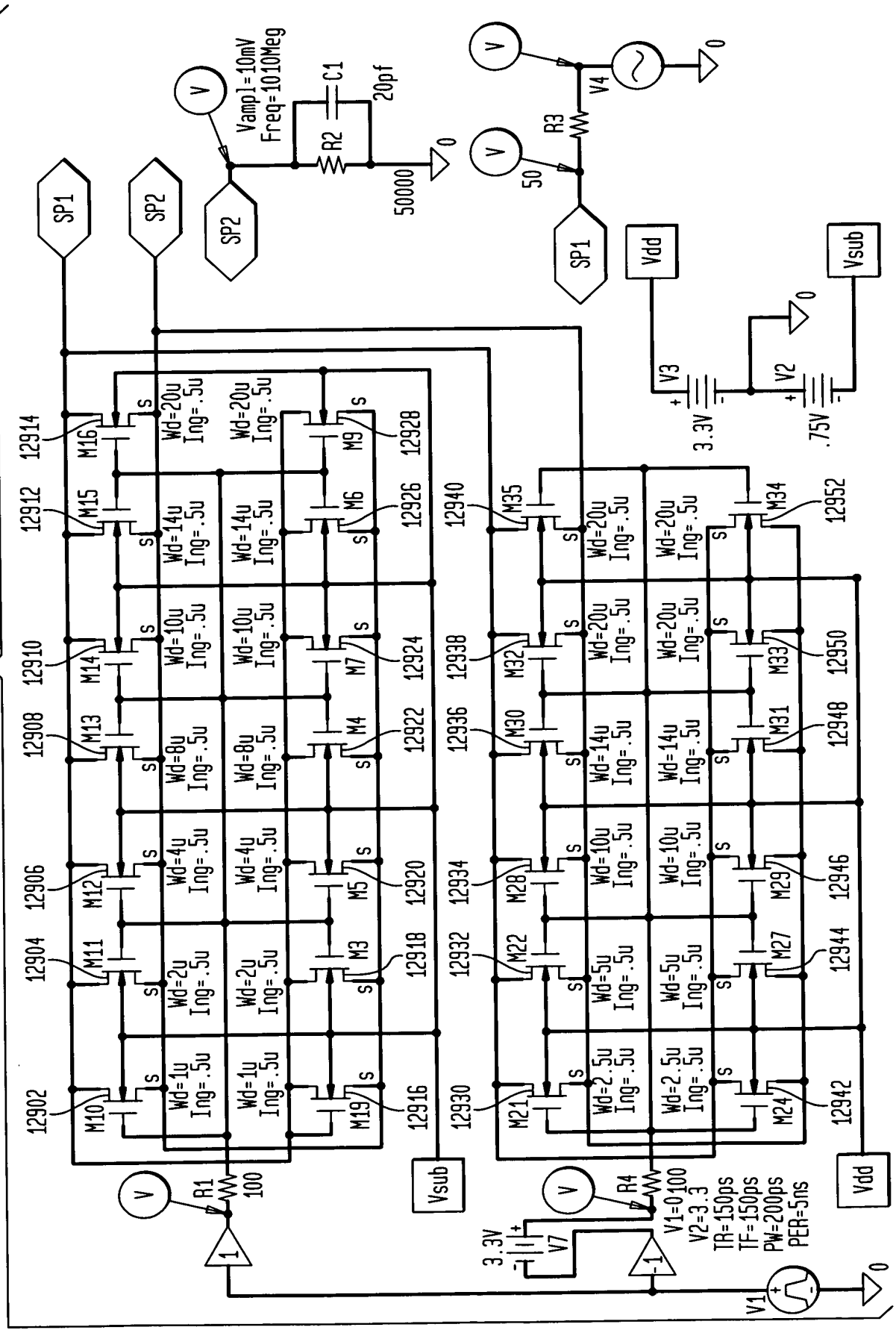

12828
12832
12824
12826
12820
12822
12806
P
G
D
12810
n+
n+
12816
P
12830
12802
12818

FIG. 129A


SP1
SP2
Vampl=10mV
Freq=1010Meg
C1
20pf
R2
50000
R3
50
V4
Vdd
Vsub
V3
3.3V
V2
.75V
R1
100
R4
V1=0100
V2=3.3
TR=150ps
TF=150ps
PW=200ps
PER=5ns
V7
3.3V
M10
M11
M12
M13
M14
M15
M16
M19
M5
M3
M4
M7
M6
M9
M21
M22
M28
M30
M32
M35
M34
M33
M31
M29
M27
M24
12902
12904
12906
12908
12910
12912
12914
12916
12918
12920
12922
12924
12926
12928
12930
12932
12934
12936
12938
12940
12942
12944
12946
12948
12950
12952
Wd=1u
Wd=2u
Wd=4u
Wd=8u
Wd=10u
Wd=14u
Wd=20u
Wd=2.5u
Wd=5u
Lng=.5u

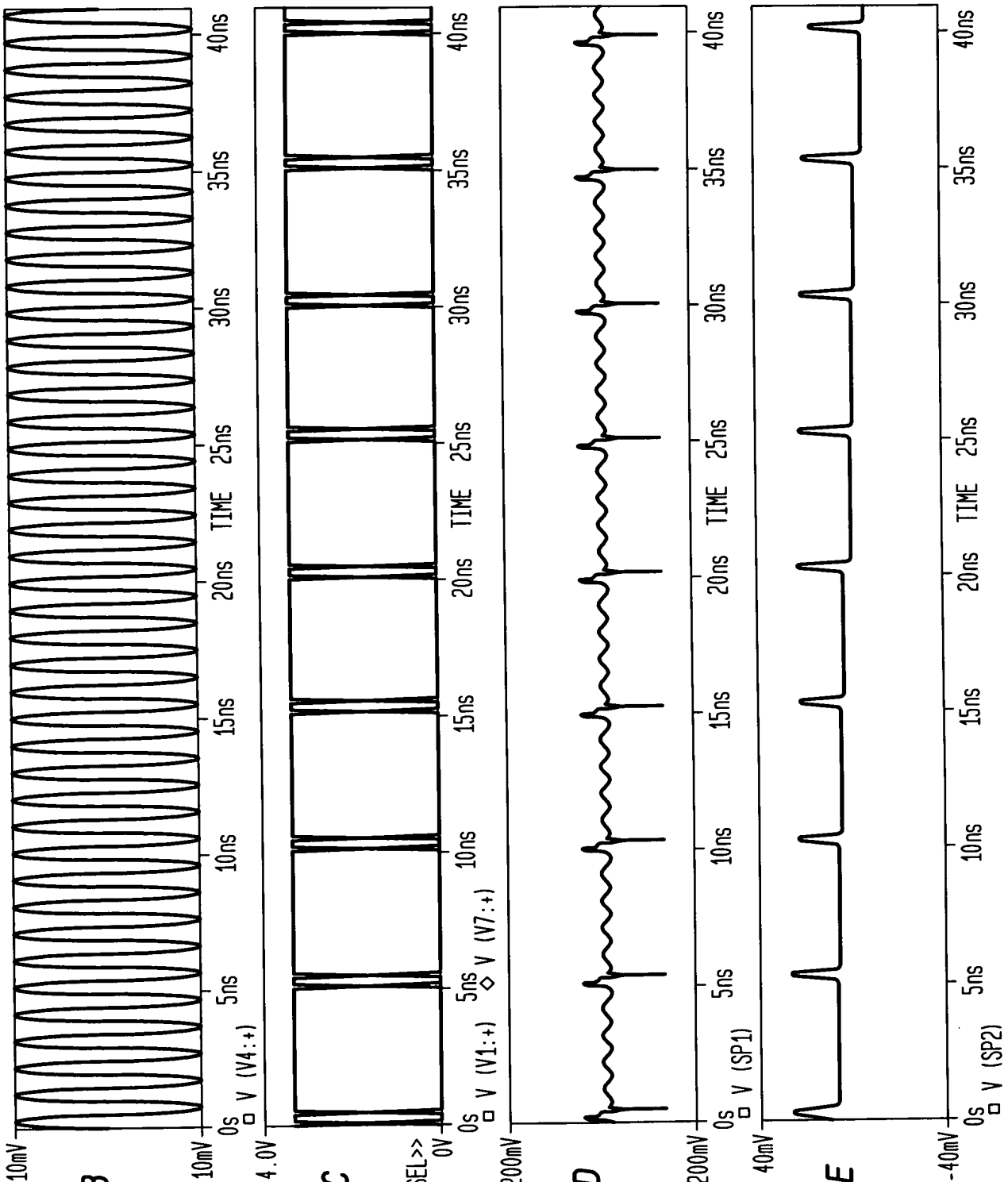



FIG. 129B

FIG. 129C

FIG. 129D

FIG. 129E

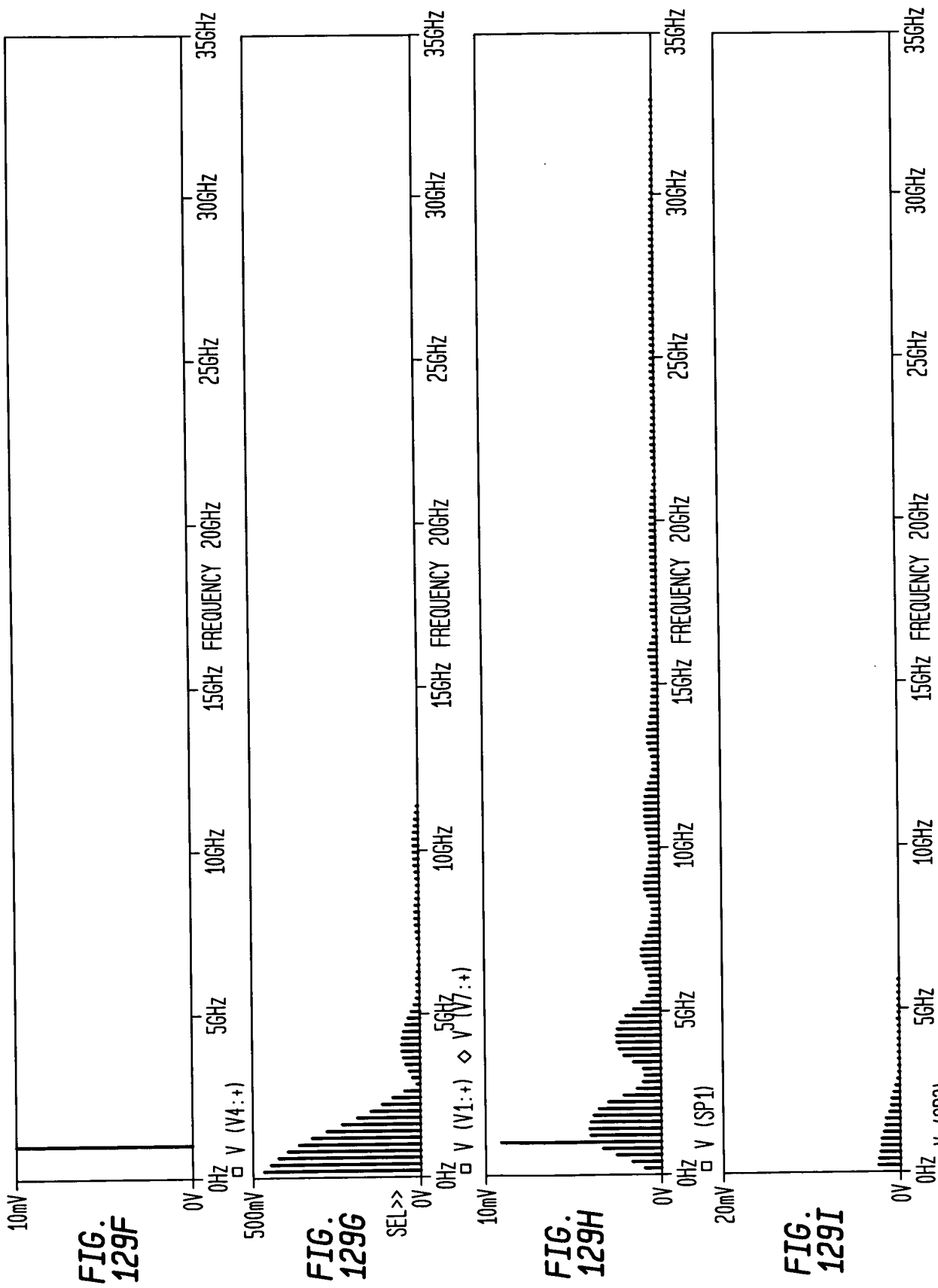



FIG. 129F

FIG. 129G

FIG. 129H

FIG. 129I

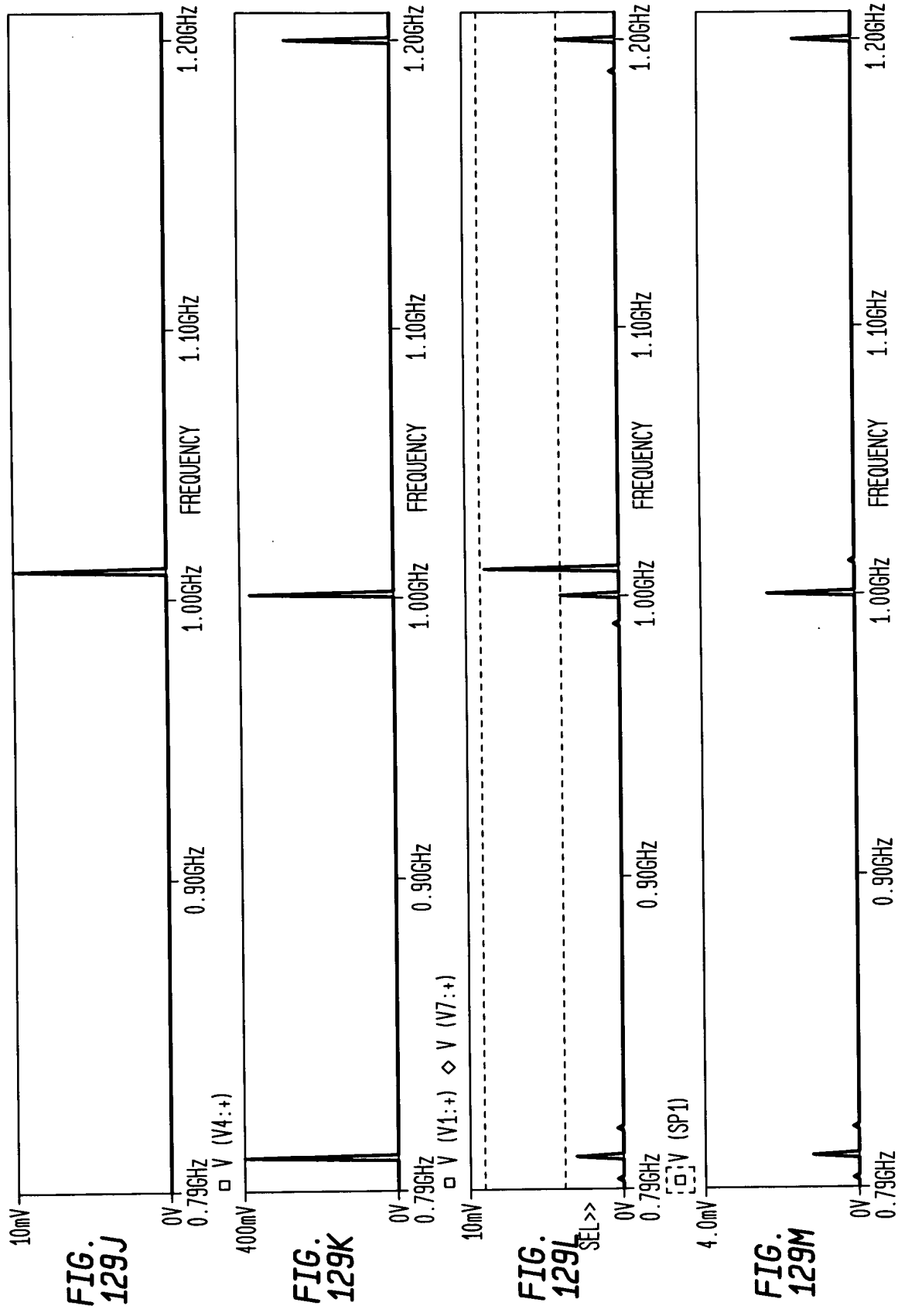



FIG. 129J

FIG. 129K

FIG. 129L

FIG. 129M

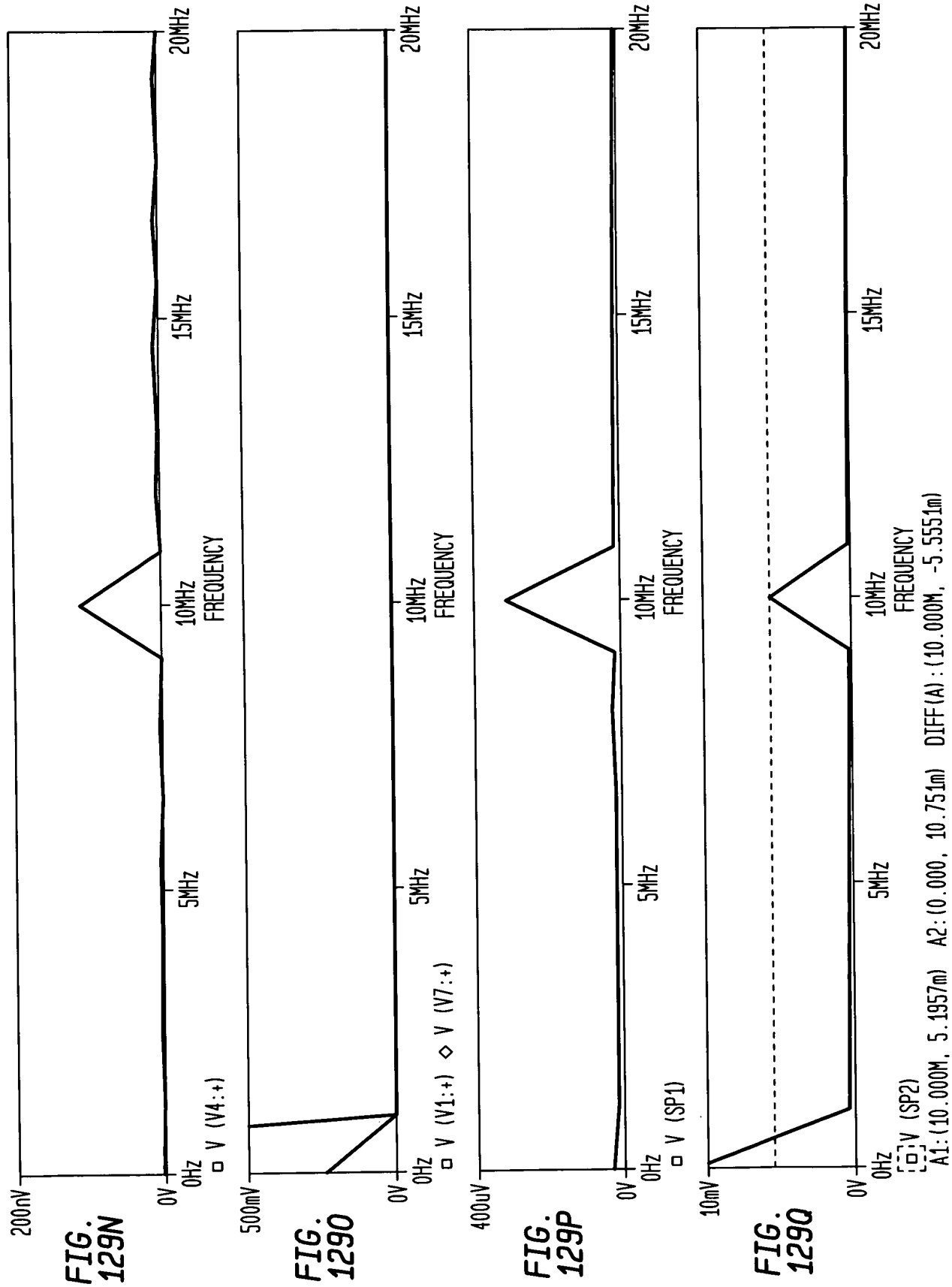



FIG. 129N

FIG. 129O

FIG. 129P

FIG. 129Q

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For: Method and System for Down-Converting an
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FIG. 130

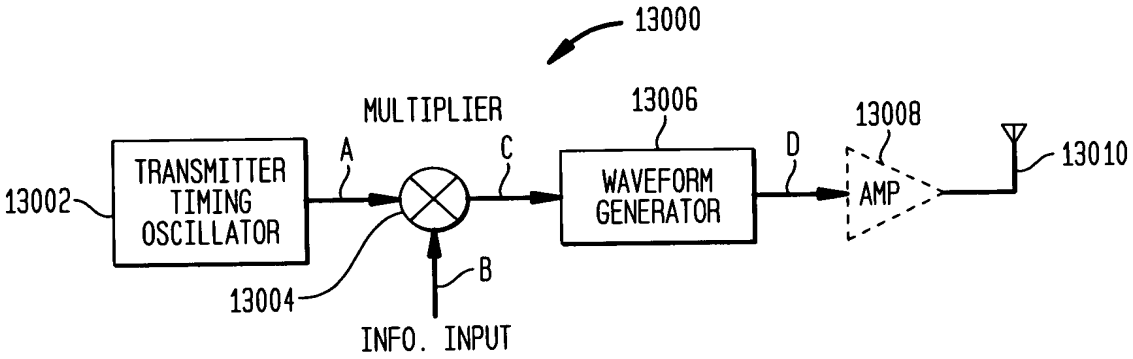

FIG. 131

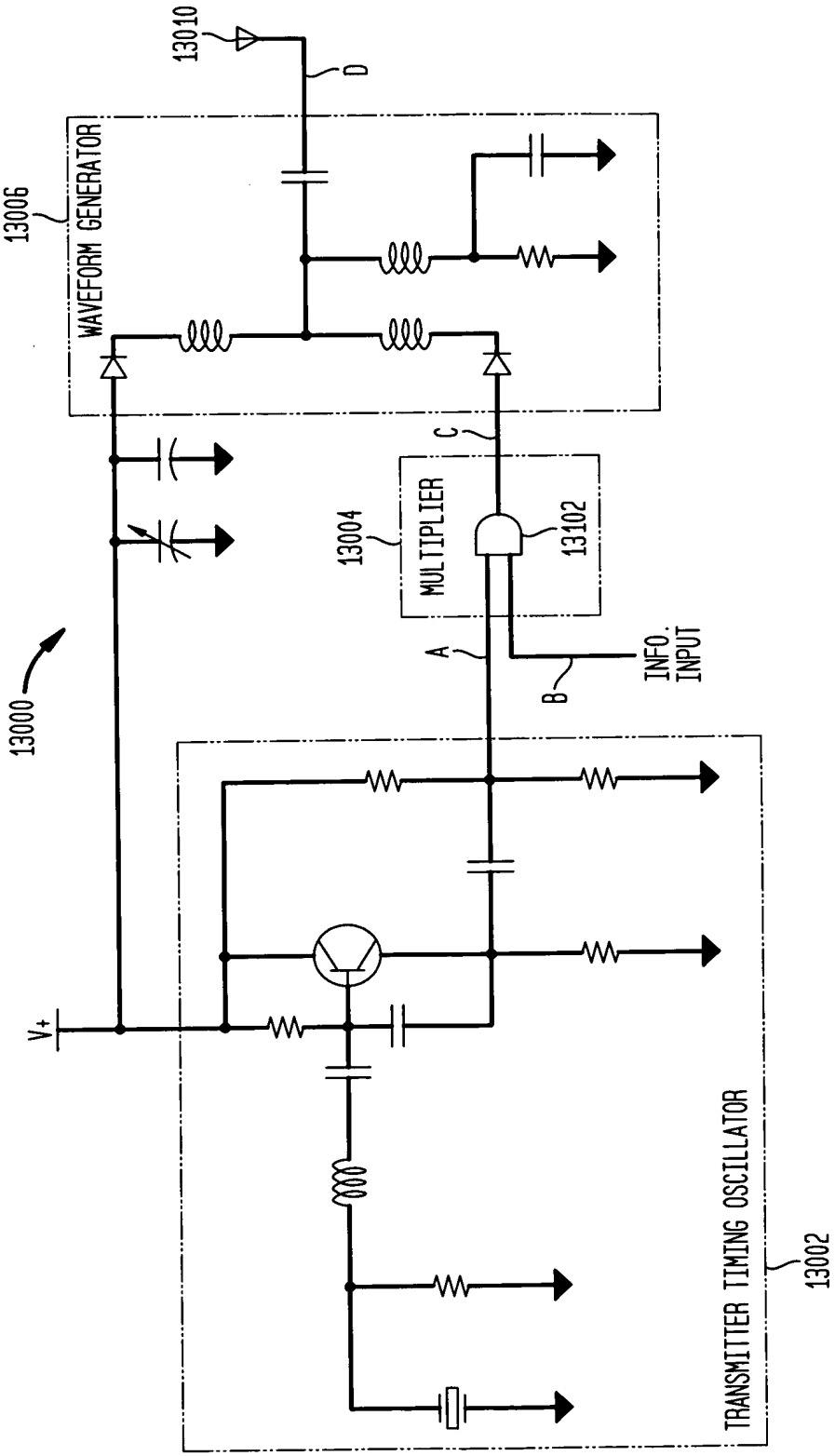
13010
D
13006
WAVEFORM GENERATOR
C
13004
MULTIPLIER
13102
A
B
INFO. INPUT
13000
V+
TRANSMITTER TIMING OSCILLATOR
13002

FIG. 132A

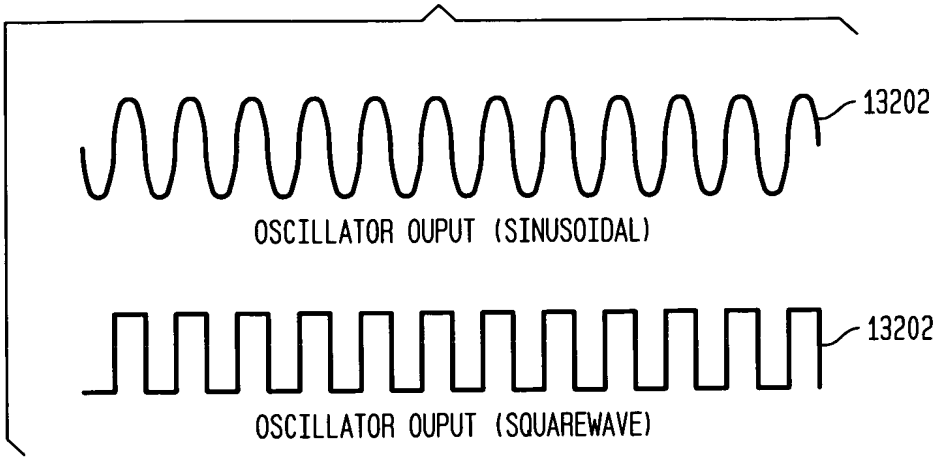


FIG. 132B

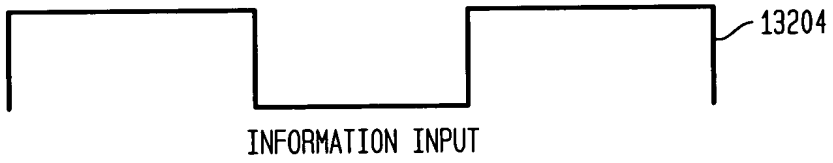


FIG. 132C

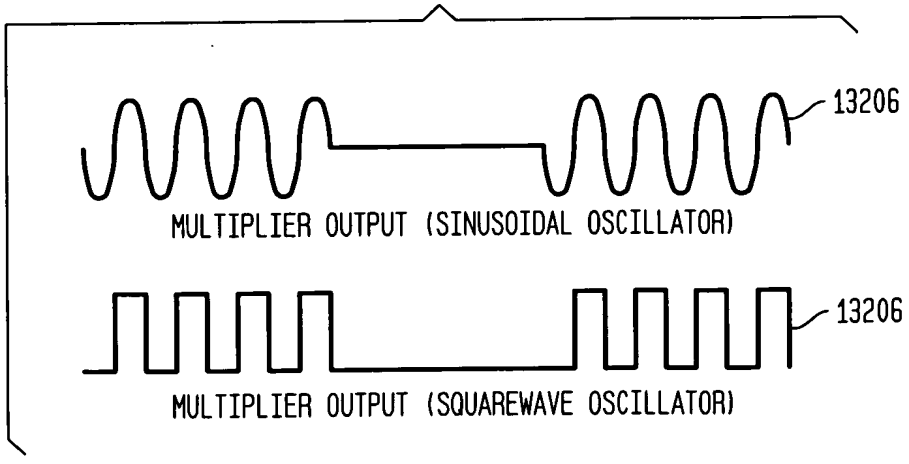


FIG. 132D

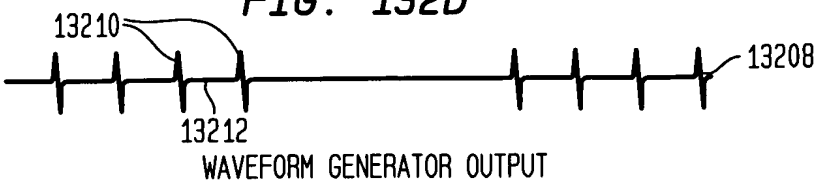

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FIG. 133

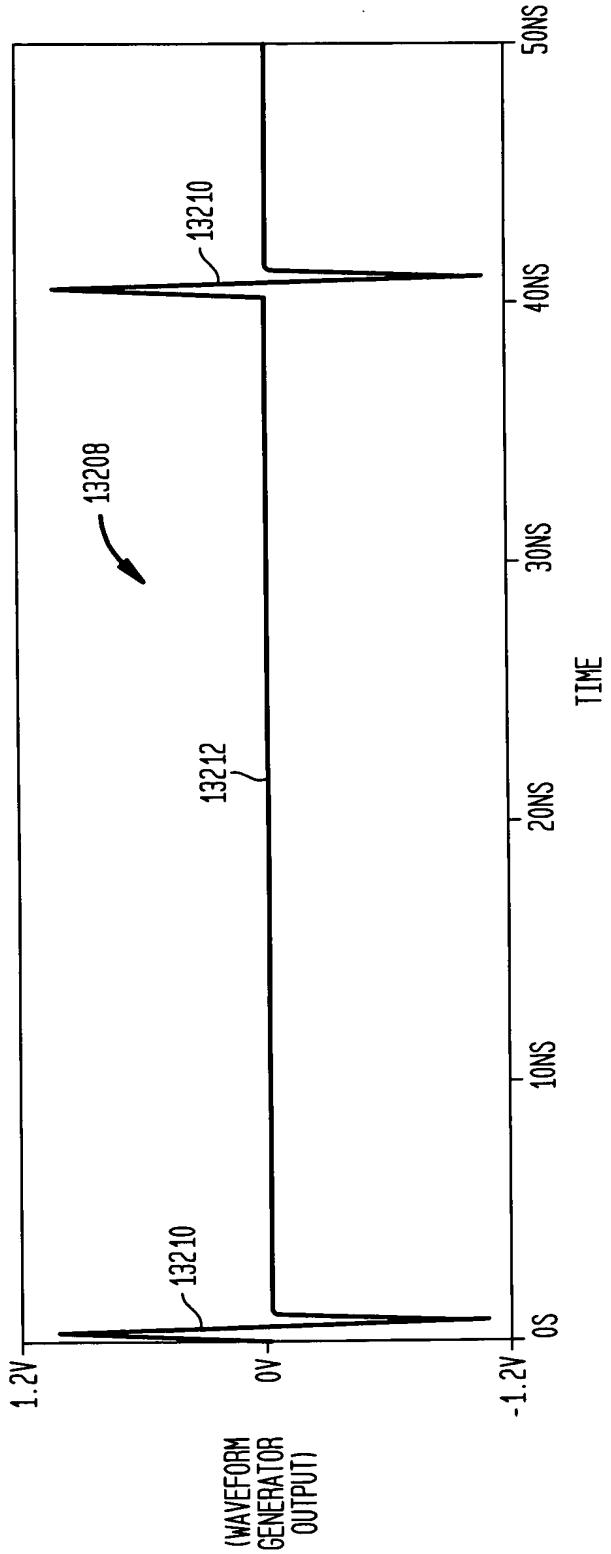

FIG. 134

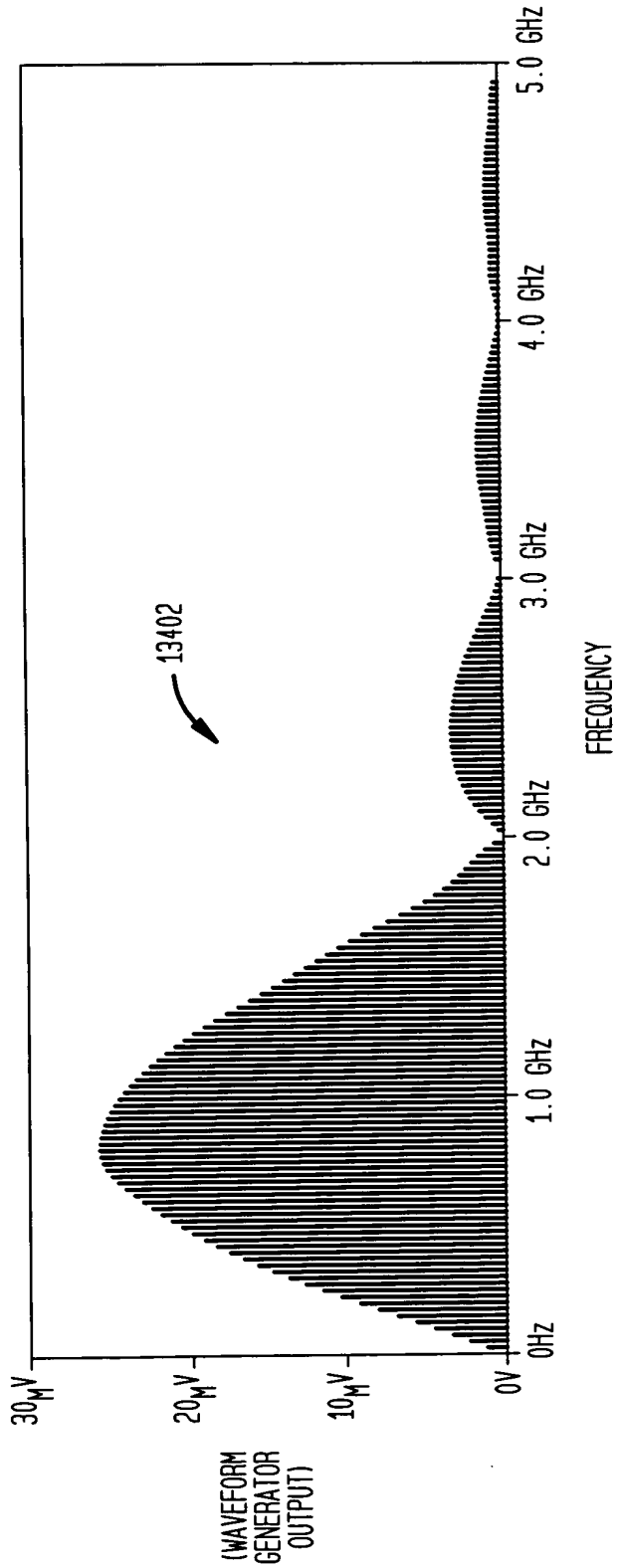
13402
30MV
20MV
10MV
0V
0Hz
1.0 GHz
2.0 GHz
3.0 GHz
4.0 GHz
5.0 GHz
FREQUENCY
(WAVEFORM GENERATOR OUTPUT)

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FIG. 135

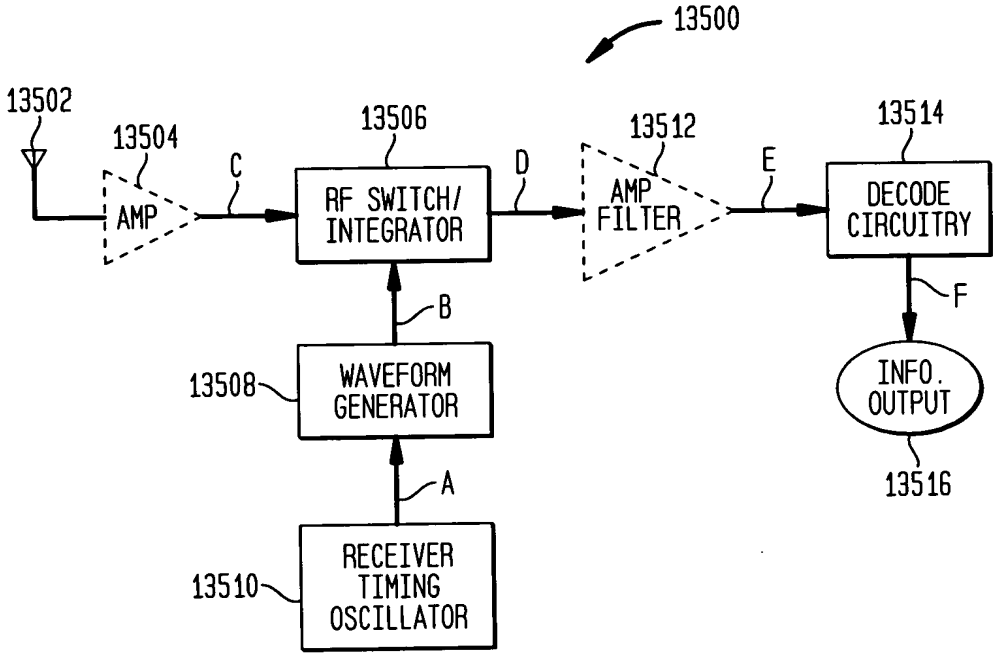
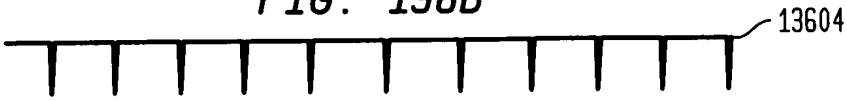


FIG. 136A


RECEIVER TIMING OSCILLATOR OUTPUT

FIG. 136B




WAVEFORM GENERATOR OUTPUT

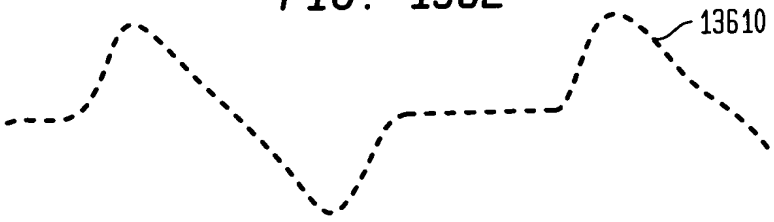
FIG. 136C


RF INPUT

FIG. 136D

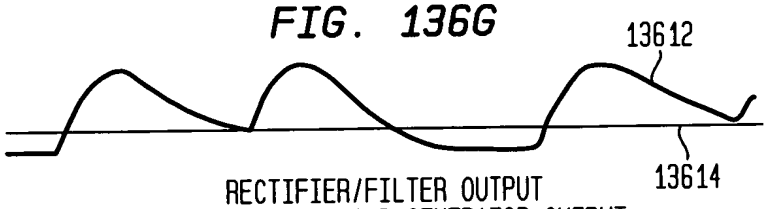

RF SWITCH/INTEGRATOR OUTPUT

FIG. 136E




OPTIONAL AMPLIFIER/FILTER OUTPUT

FIG. 136G




RECTIFIER/FILTER OUTPUT
VARIABLE THRESHOLD GENERATOR OUTPUT

FIG. 136F

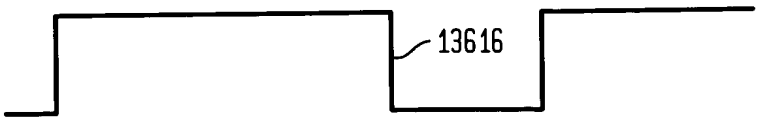
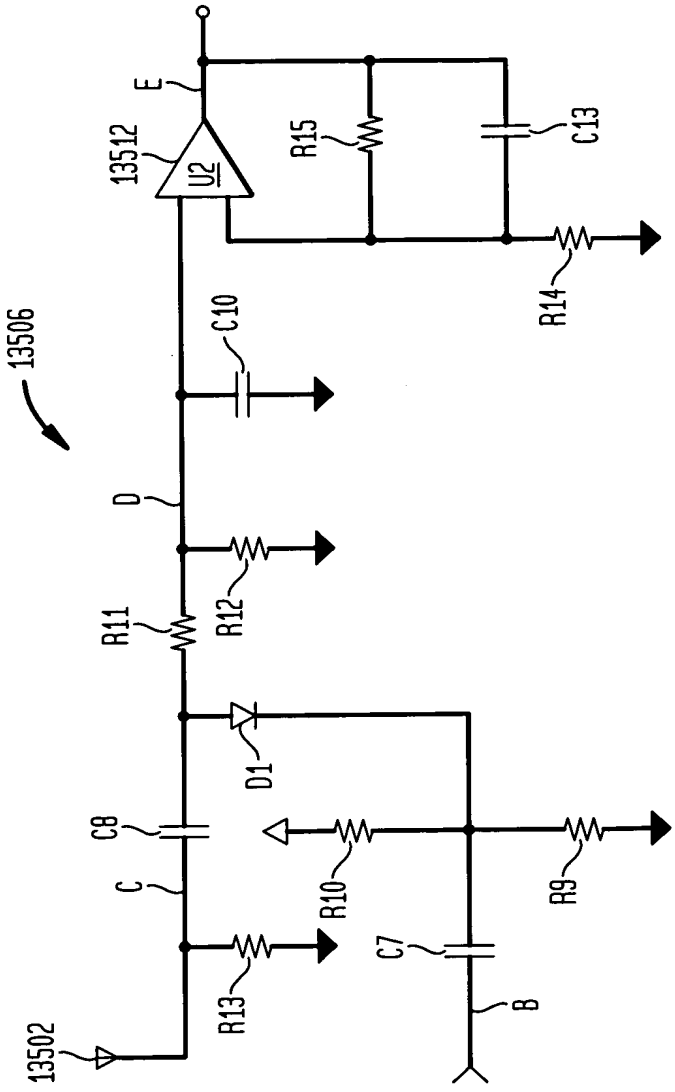


FIG. 137


13506
E
13512
U2
R15
C13
R14
C10
D
R11
R12
D1
C8
C
R10
R9
C7
R13
B
13502

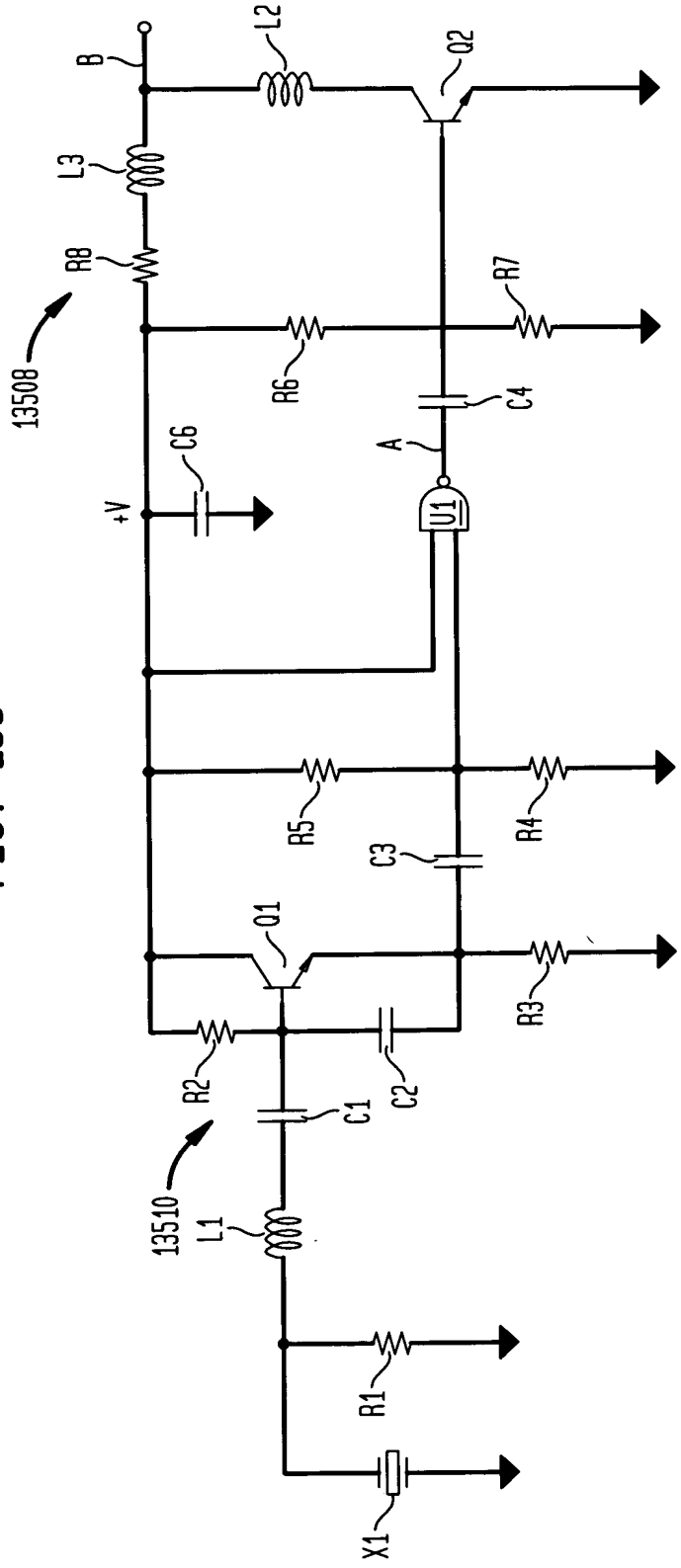

B
L2
Q2
L3
R8
13508
R7
R6
C4
A
C6
+V
U1
R5
R4
C3
Q1
R3
R2
C2
C1
13510
L1
R1
X1

FIG. 138

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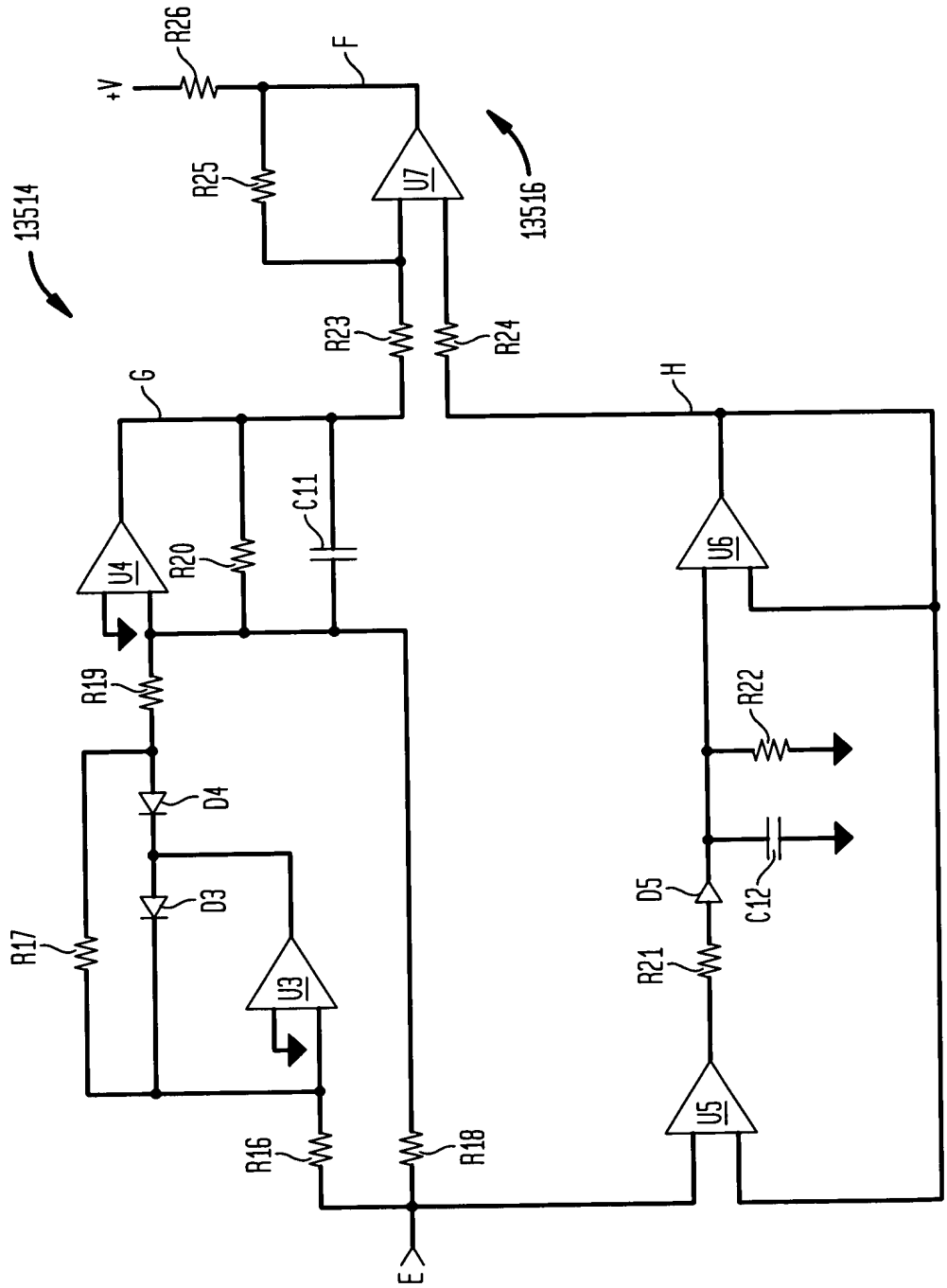


FIG. 139

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Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

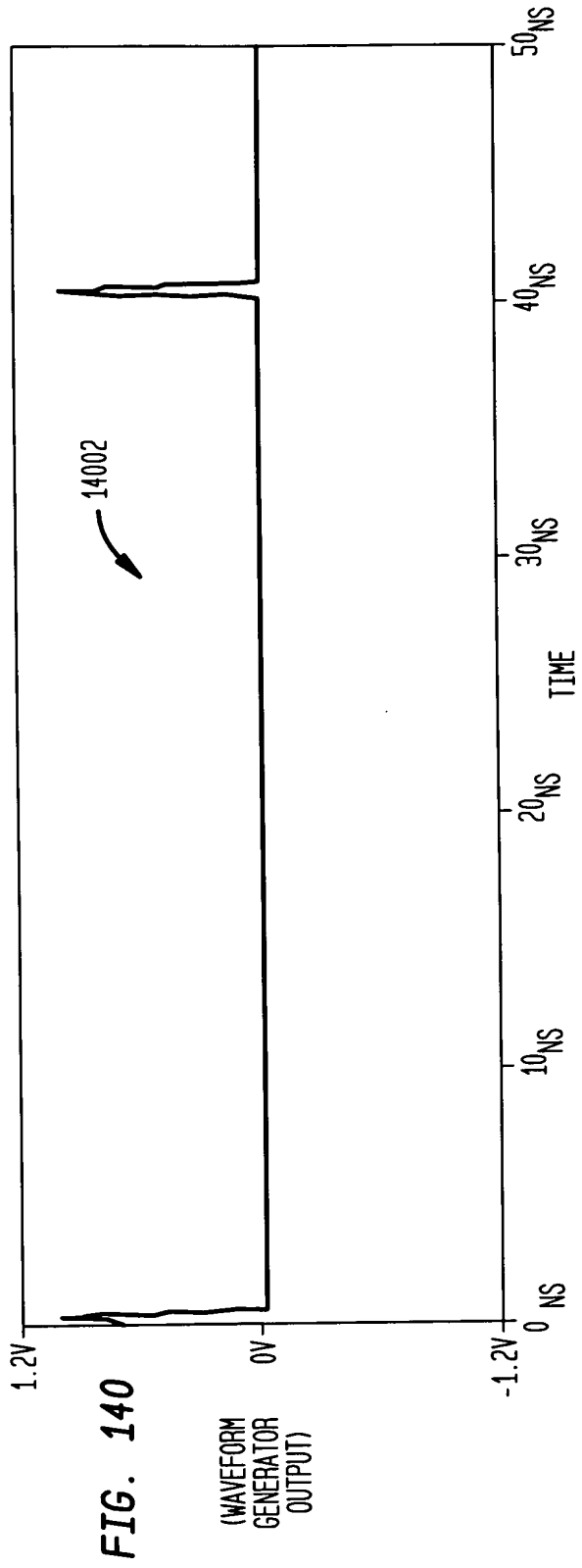


FIG. 140

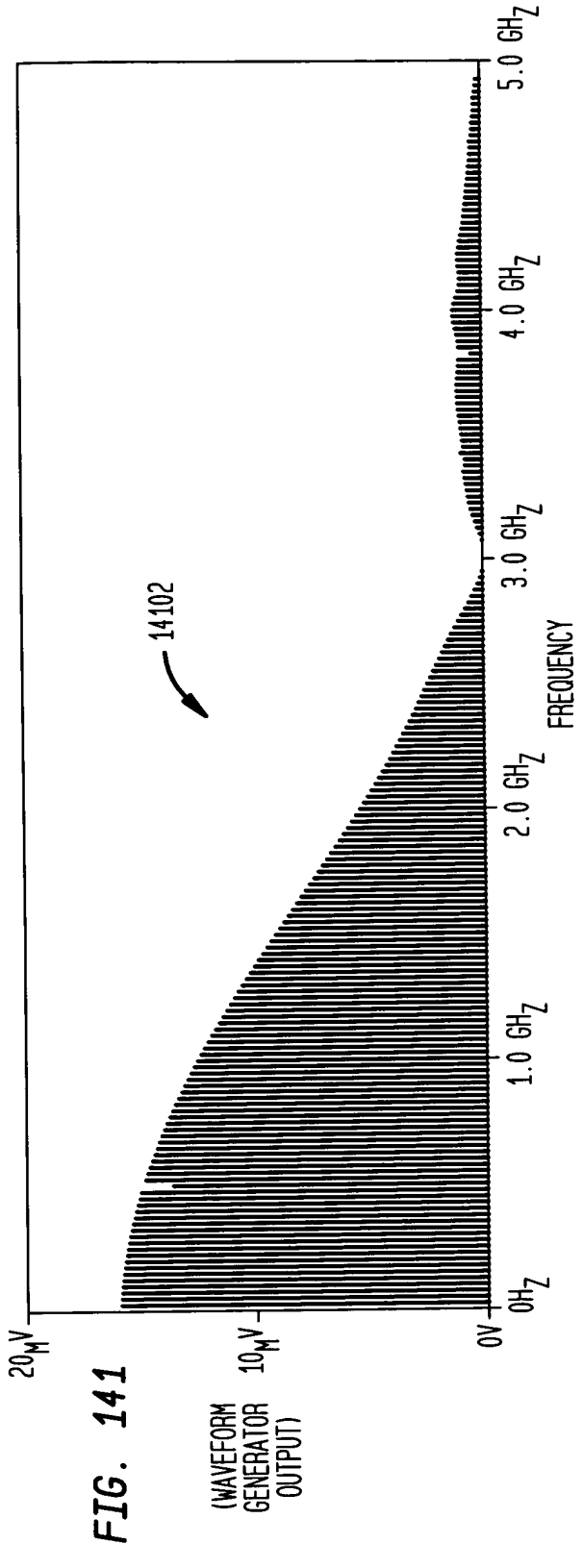


FIG. 141

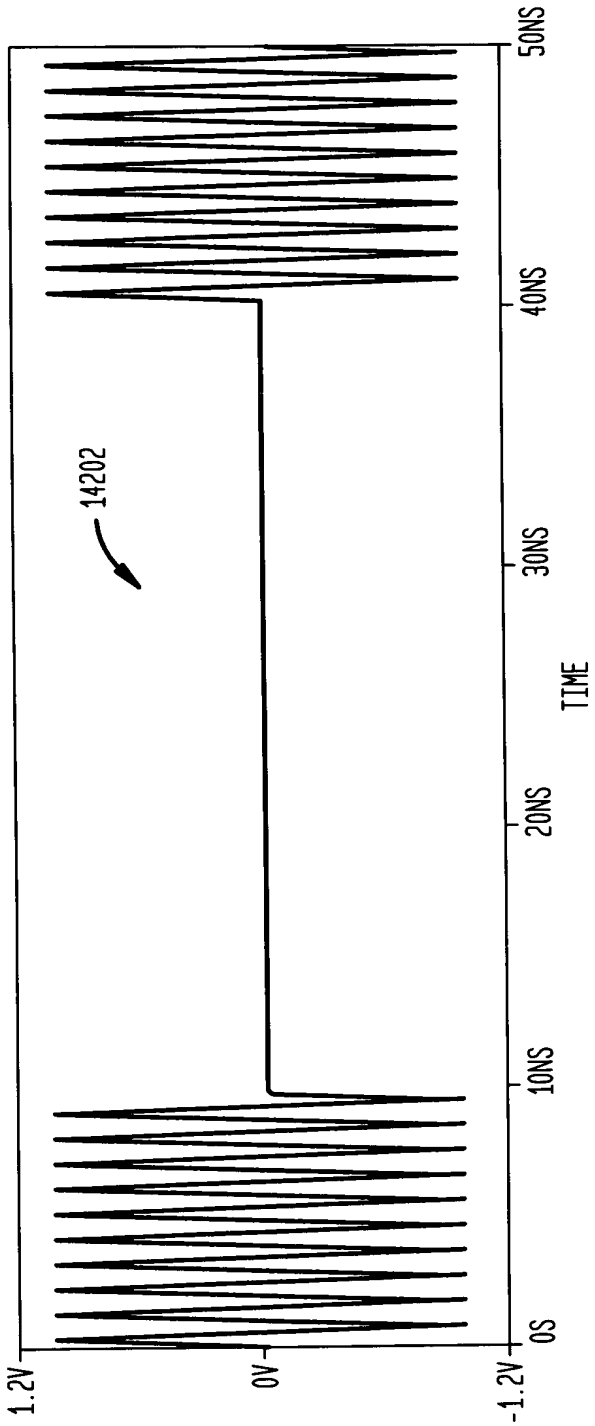


FIG. 142

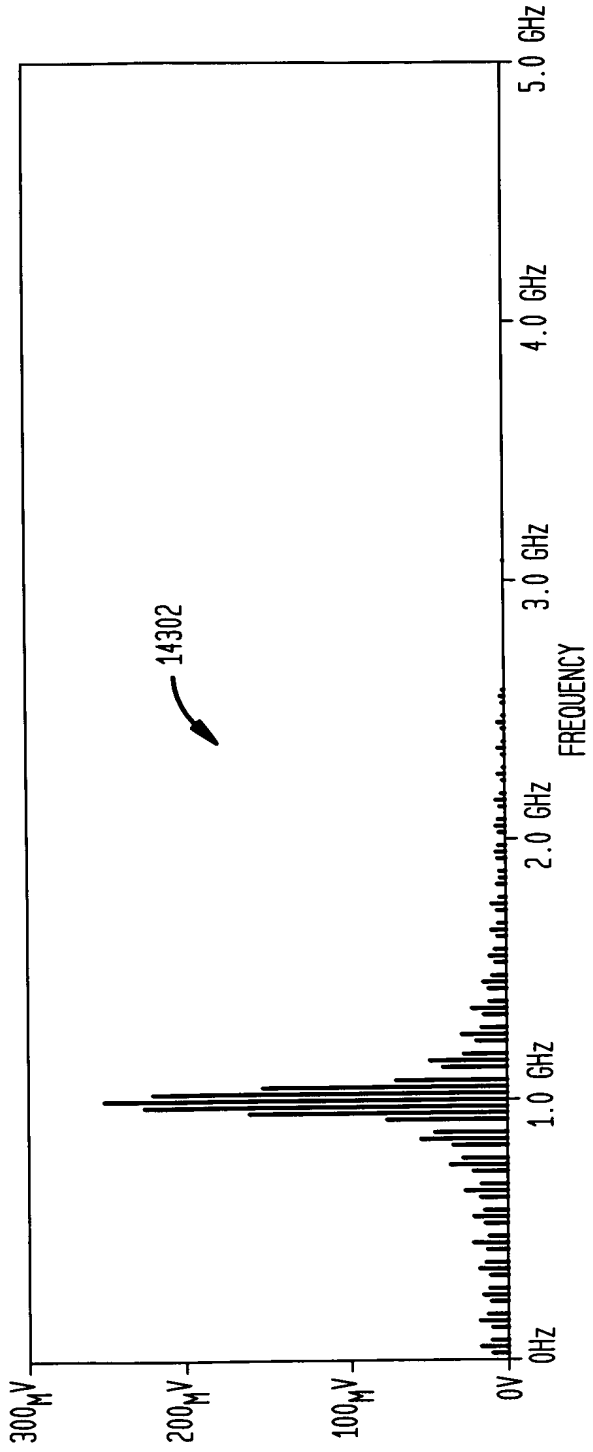


FIG. 143

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Inventors: SORRELLS et al.
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Electromagnetic Signal, and Transforms for Same

FIG. 144

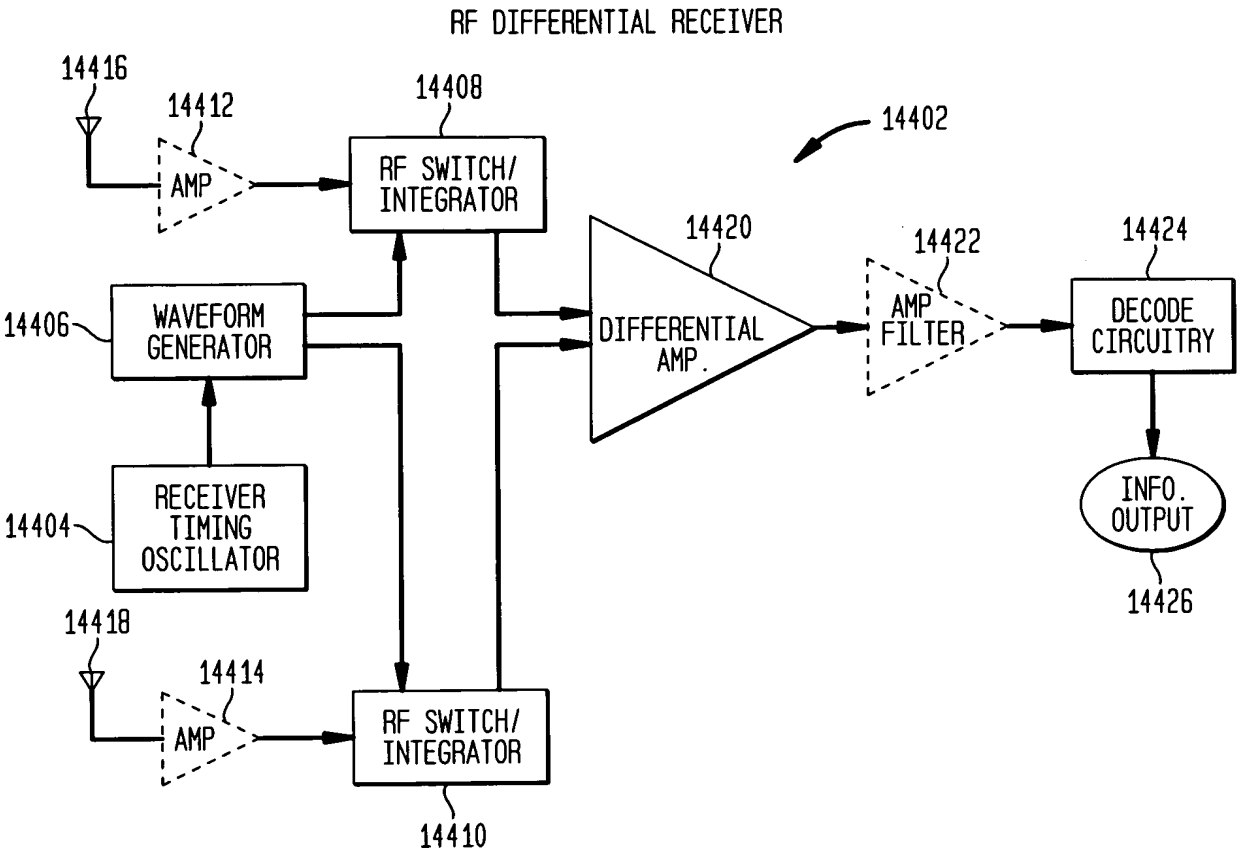
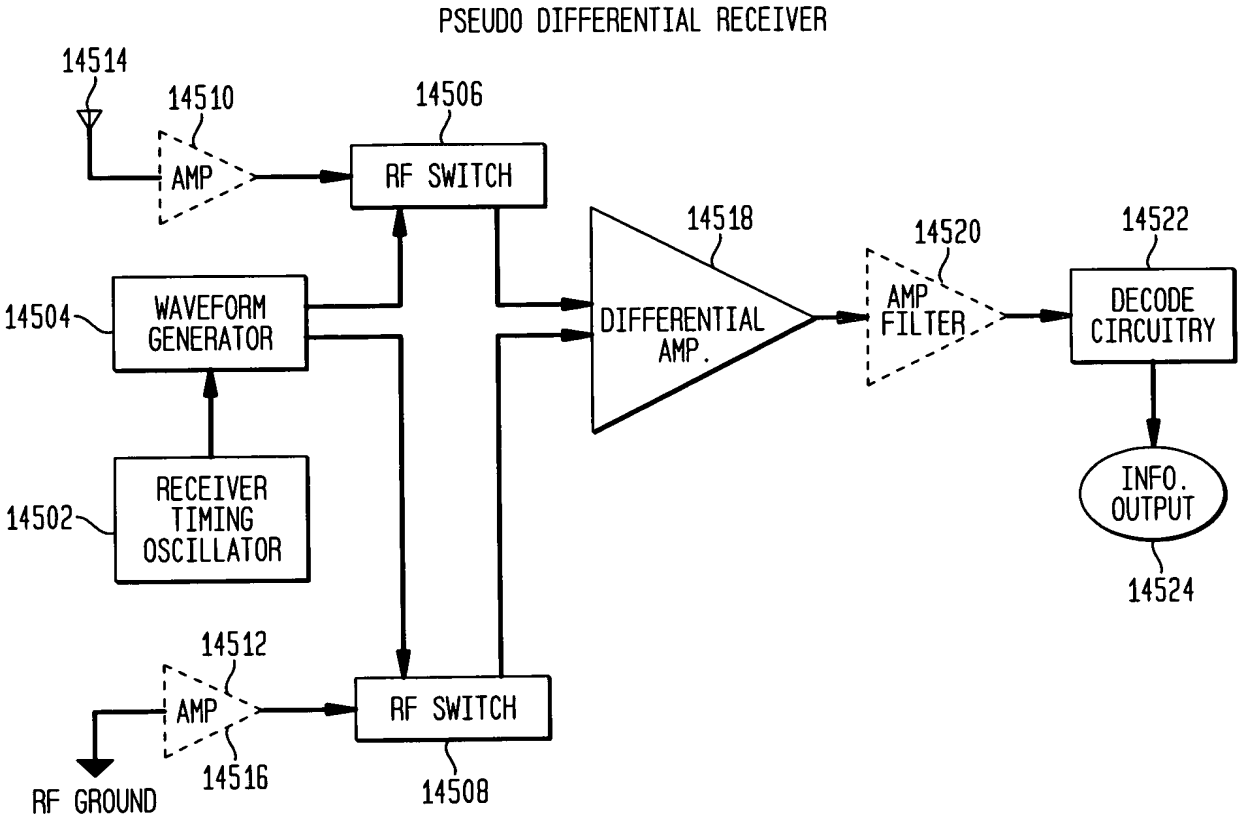


FIG. 145


PSEUDO DIFFERENTIAL RECEIVER
14514
14510
AMP
14506
RF SWITCH
14518
DIFFERENTIAL AMP.
14520
AMP FILTER
14522
DECODE CIRCUITRY
INFO. OUTPUT
14524
14504
WAVEFORM GENERATOR
14502
RECEIVER TIMING OSCILLATOR
14512
AMP
14516
RF GROUND
RF SWITCH
14508

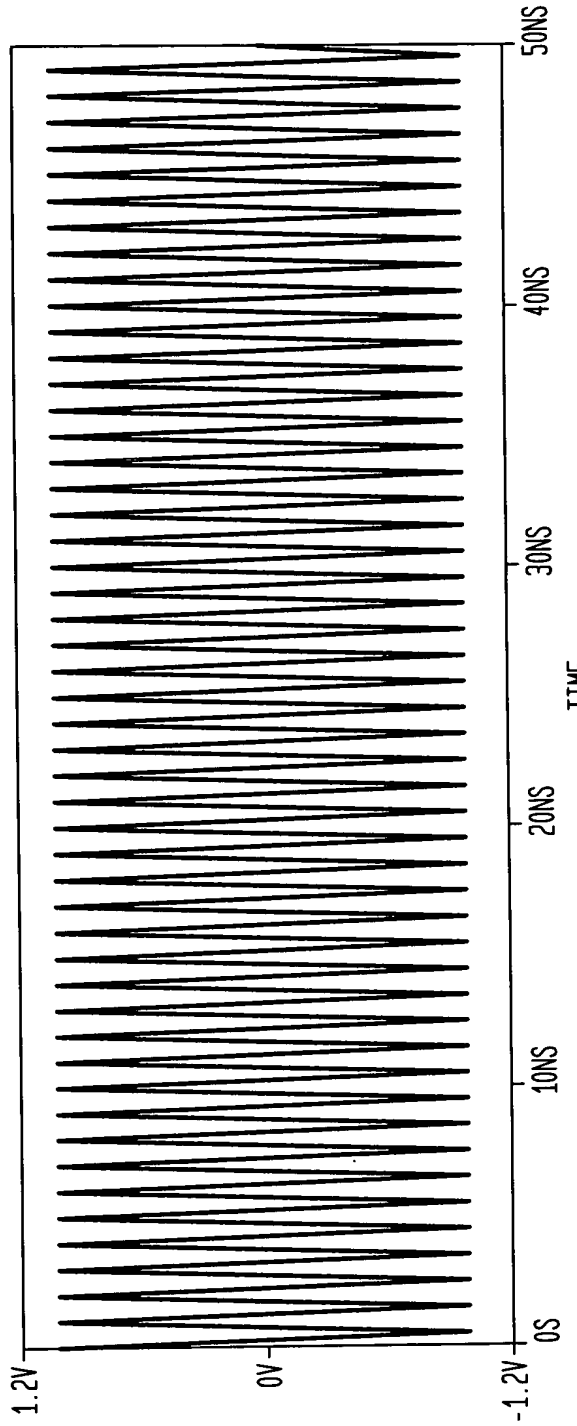



FIG. 146

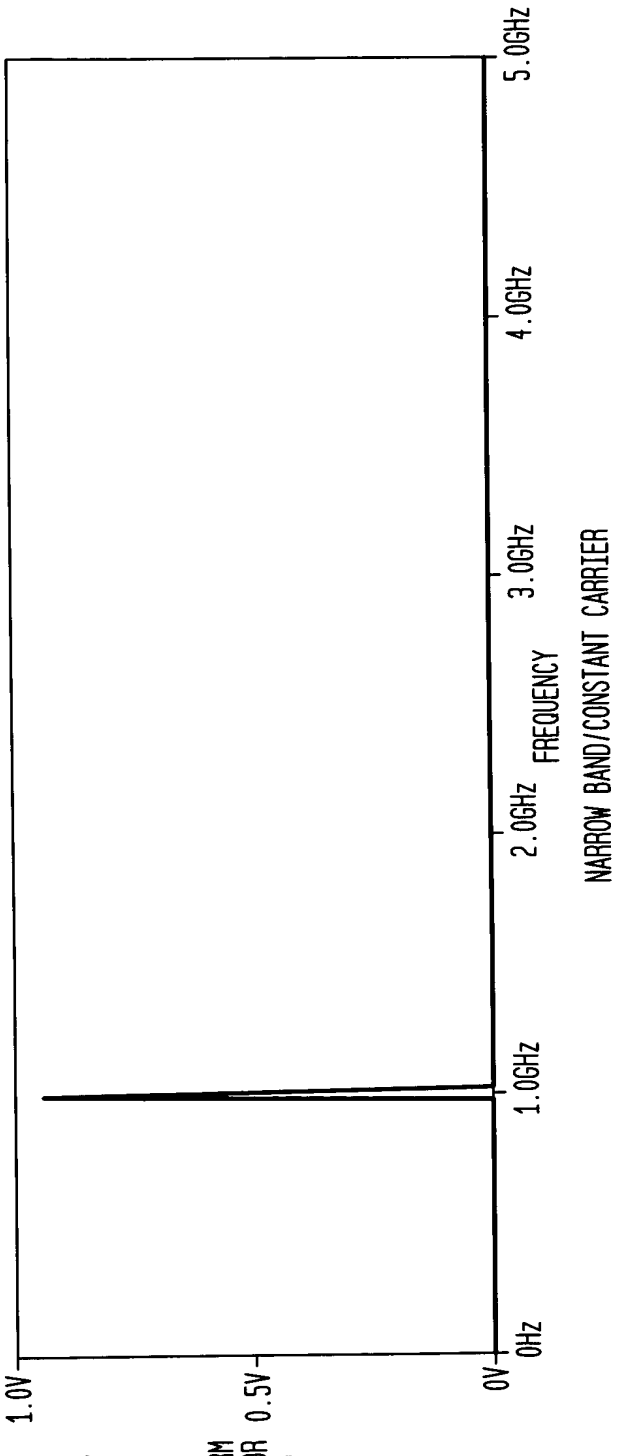



FIG. 147

FIG. 148

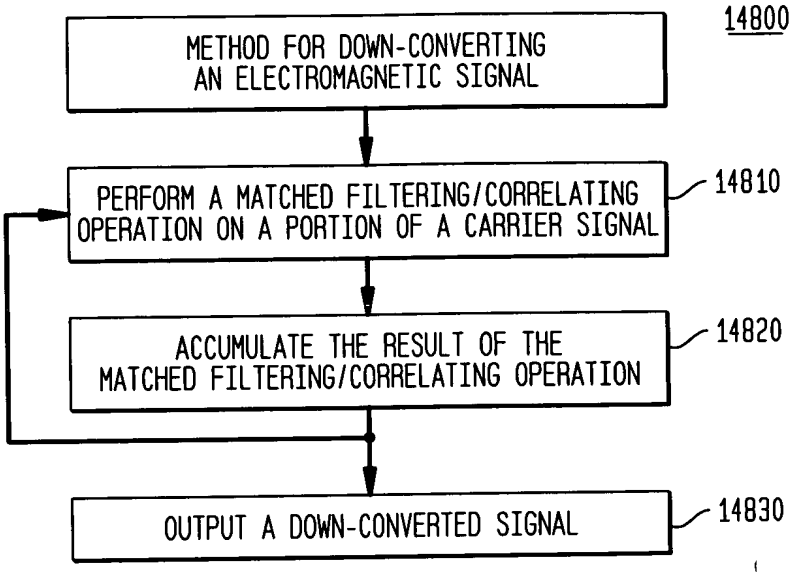



FIG. 149

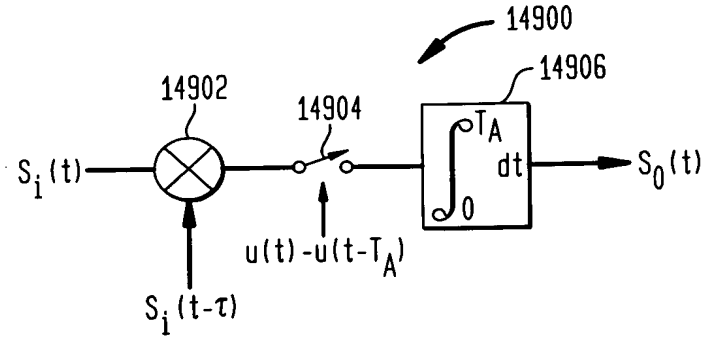


FIG. 150

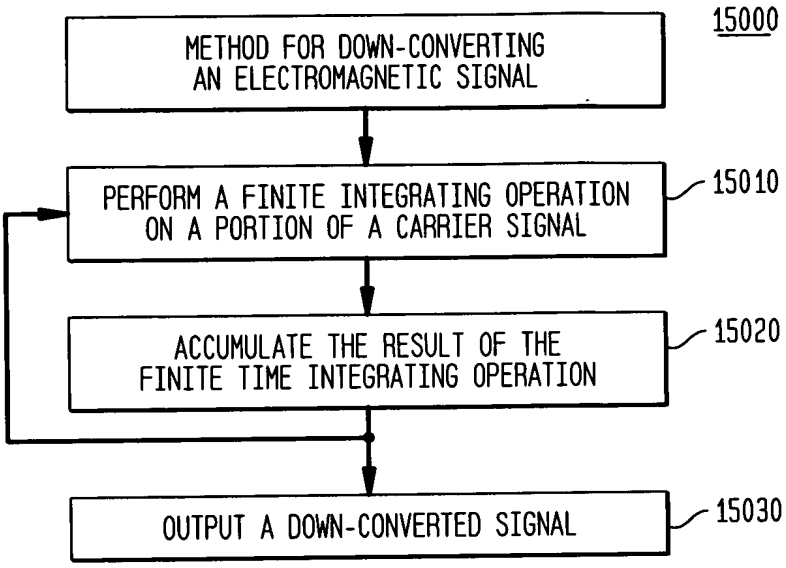



FIG. 151

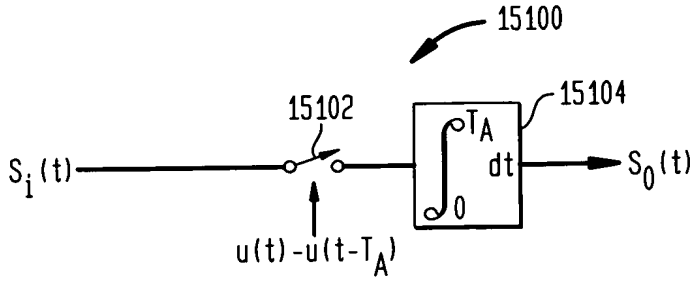


FIG. 152

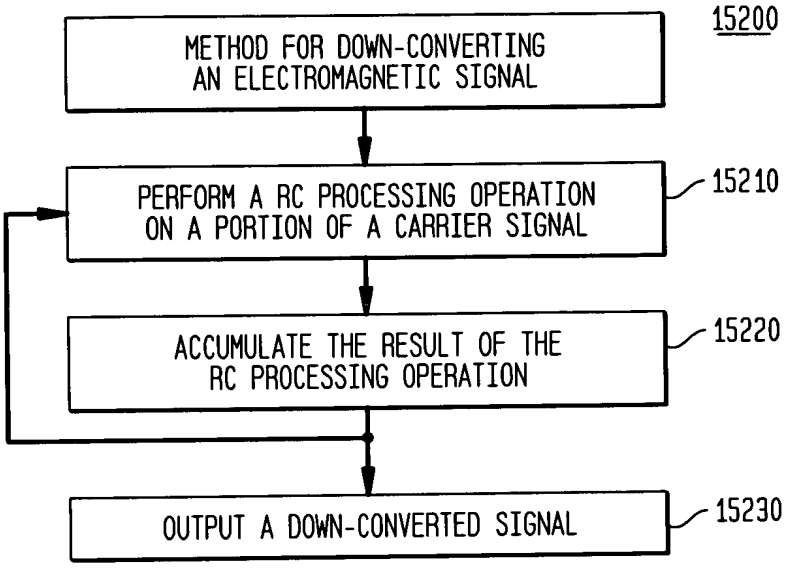



FIG. 153

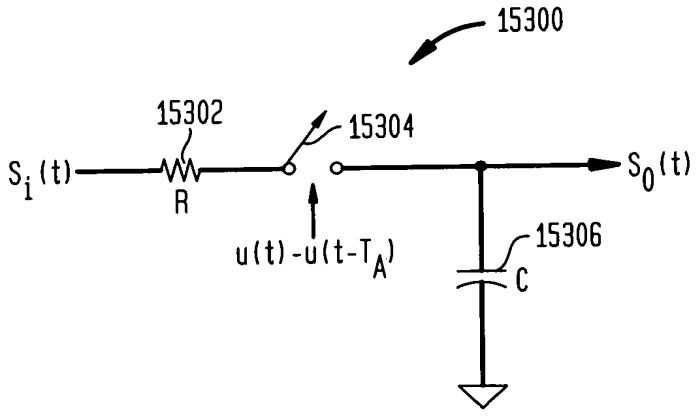


FIG. 154

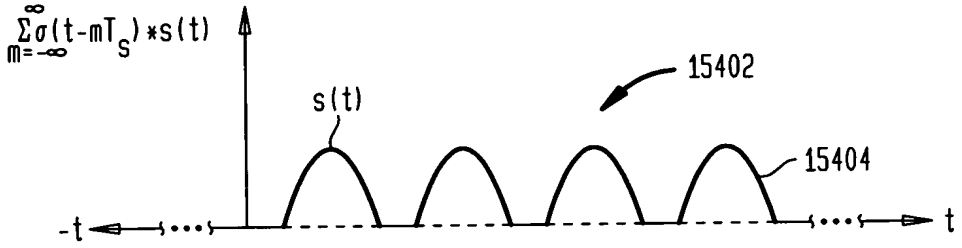



FIG. 155

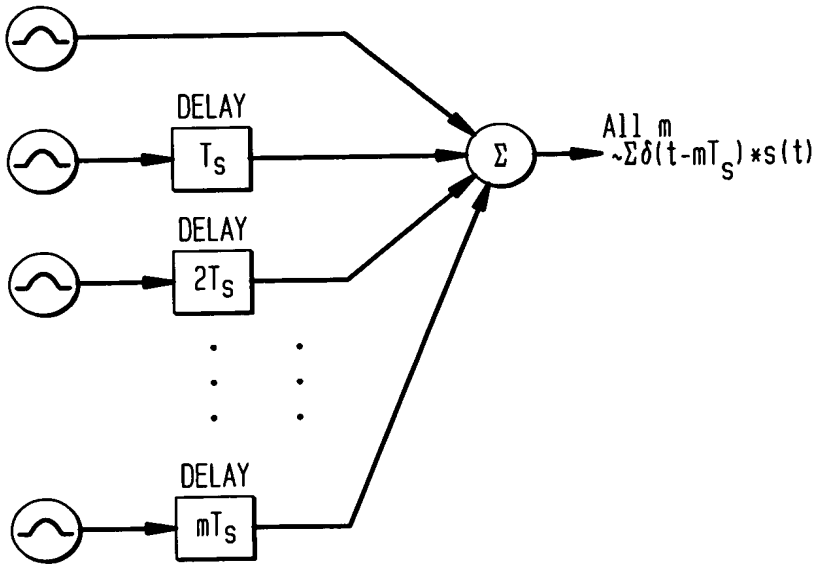


FIG. 156

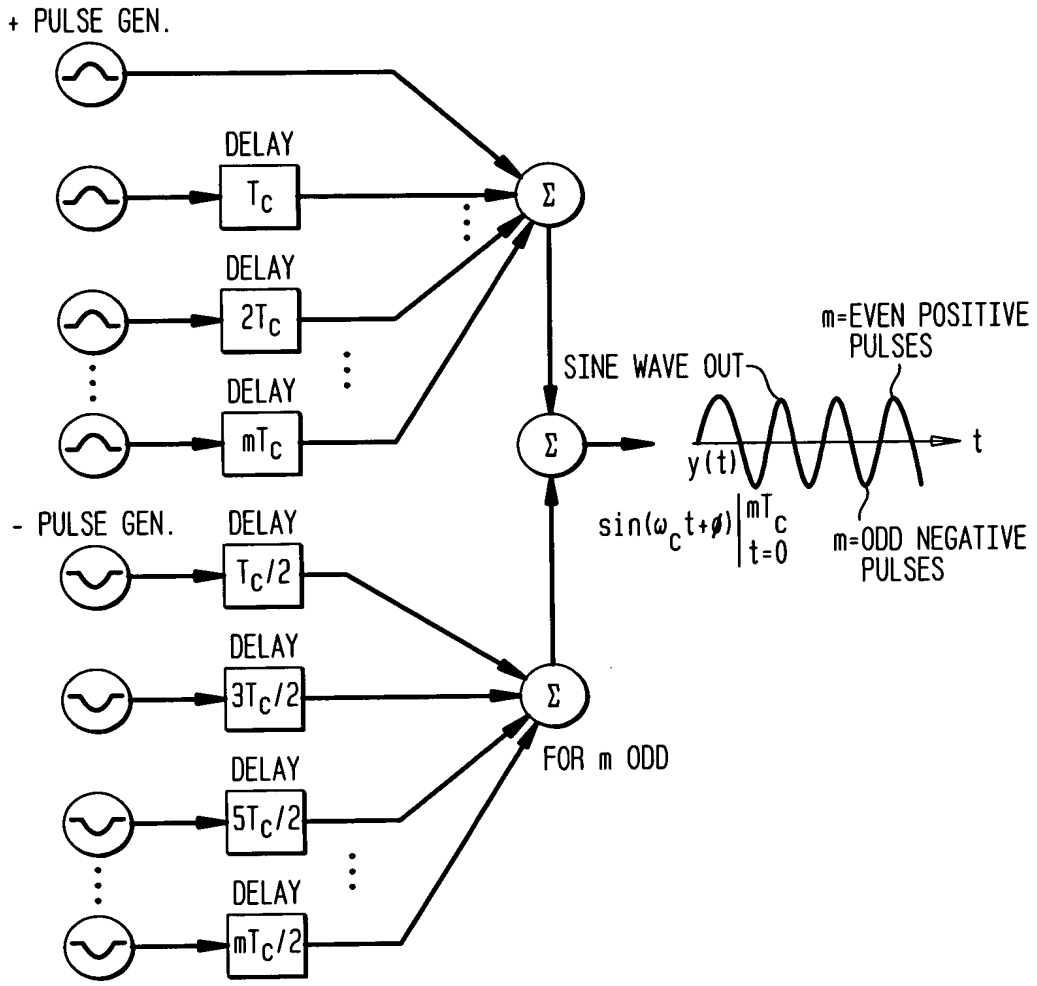
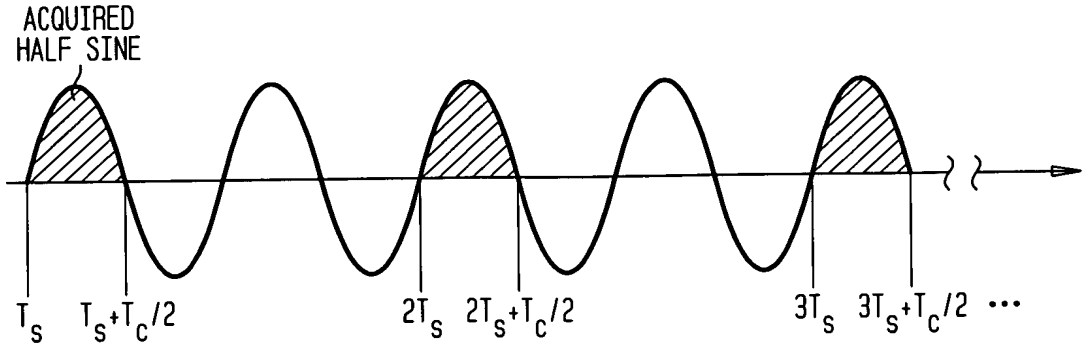



FIG. 157




CARRIER PROCESSED BY 3RD HARMONIC UFT PROCESSOR

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Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
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FIG. 158

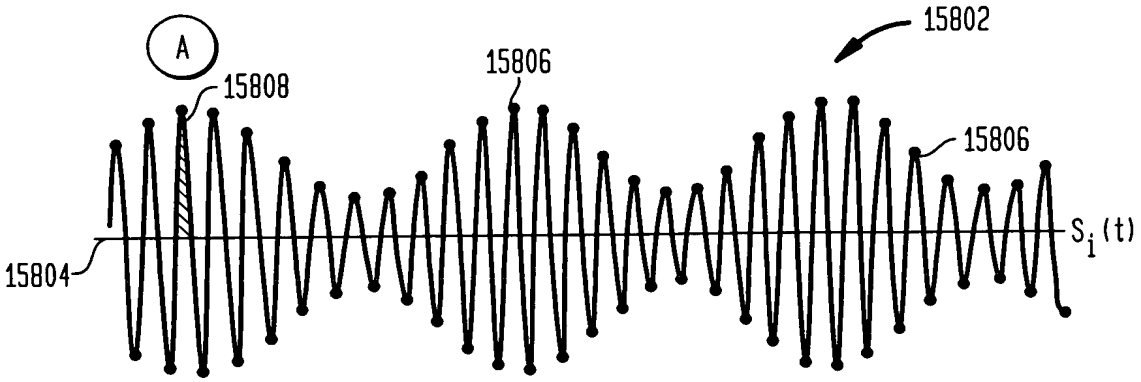



FIG. 159

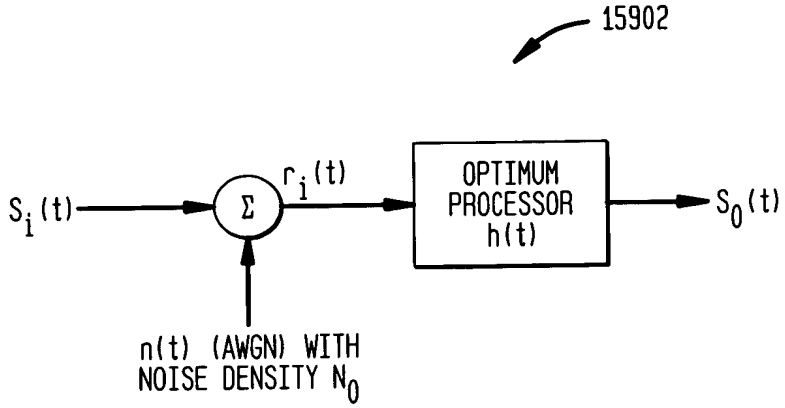
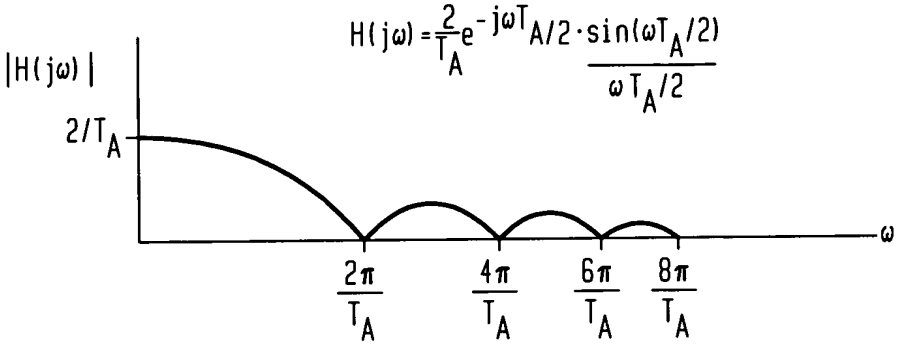
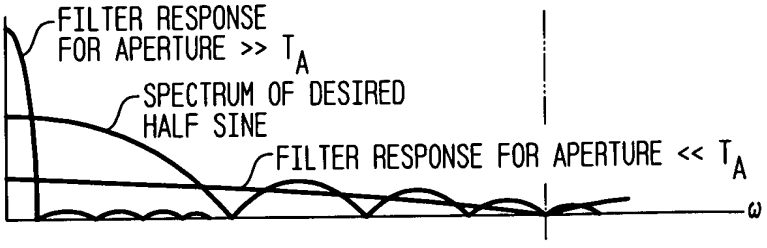


FIG. 160




MAG FREQUENCY RESPONSE OF
SAMPLING APERTURE WAVEFORM

FIG. 161




APERTURE FREQUENCY DOMAIN REPRESENTATION

FIG. 162

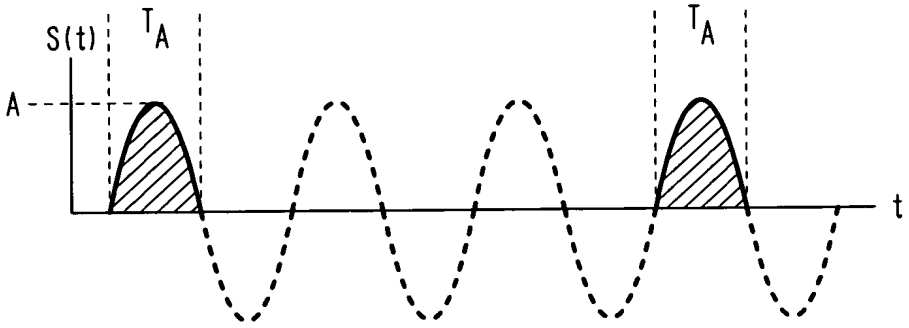
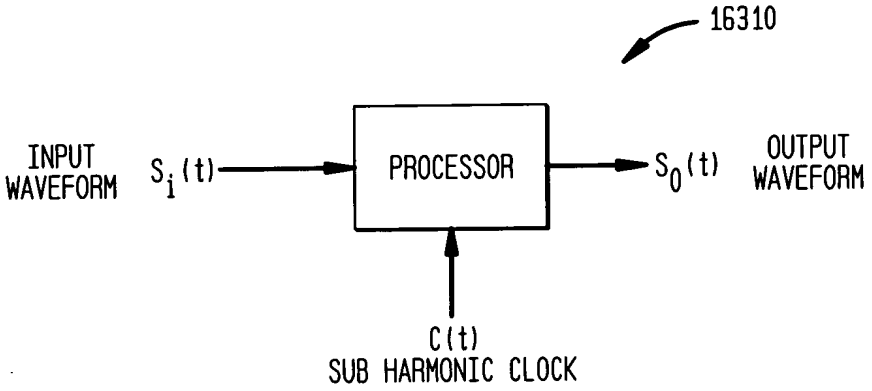



FIG. 163



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For: Method and System for Down-Converting an
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FIG. 164A

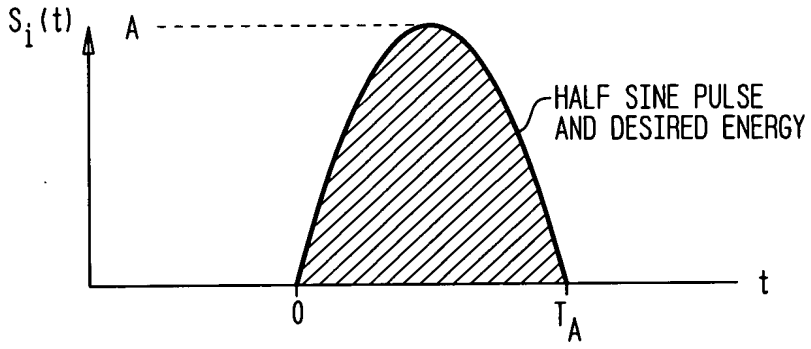


FIG. 164B

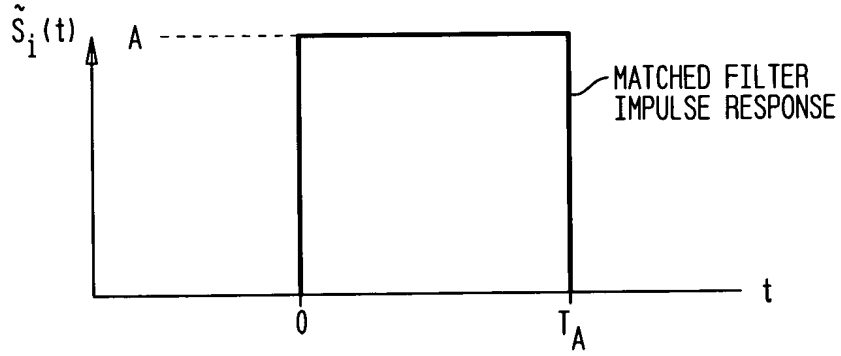


FIG. 164C

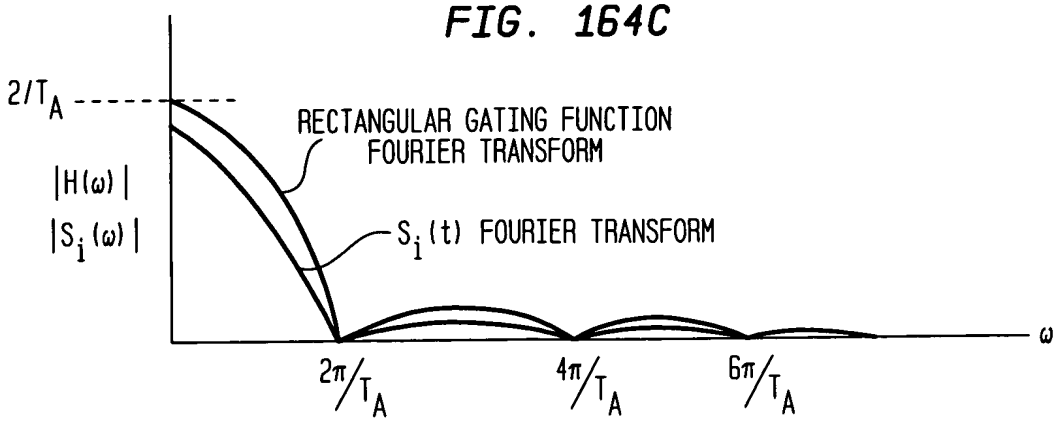

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FIG. 165

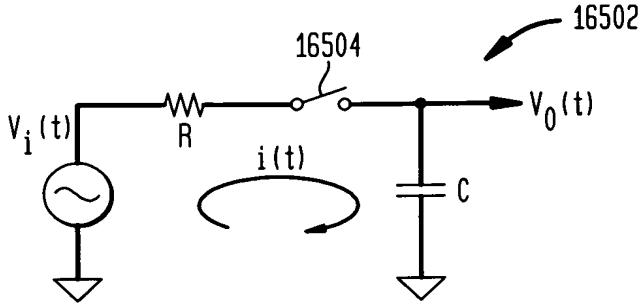



FIG. 166

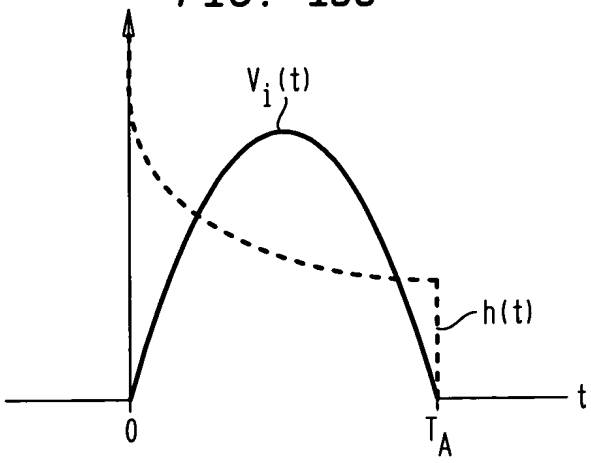



FIG. 167

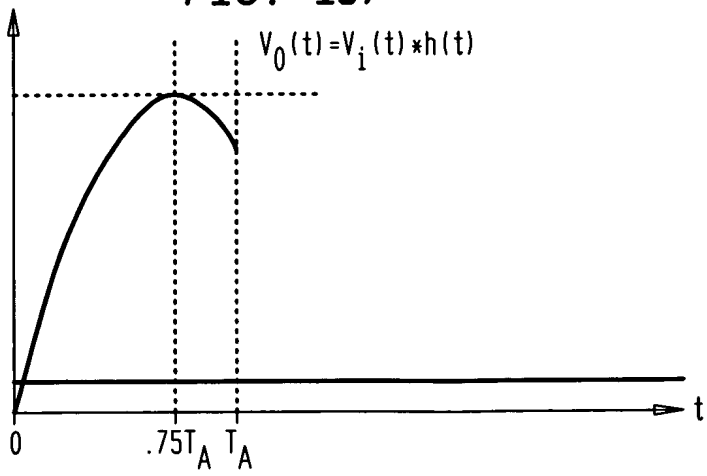


FIG. 168

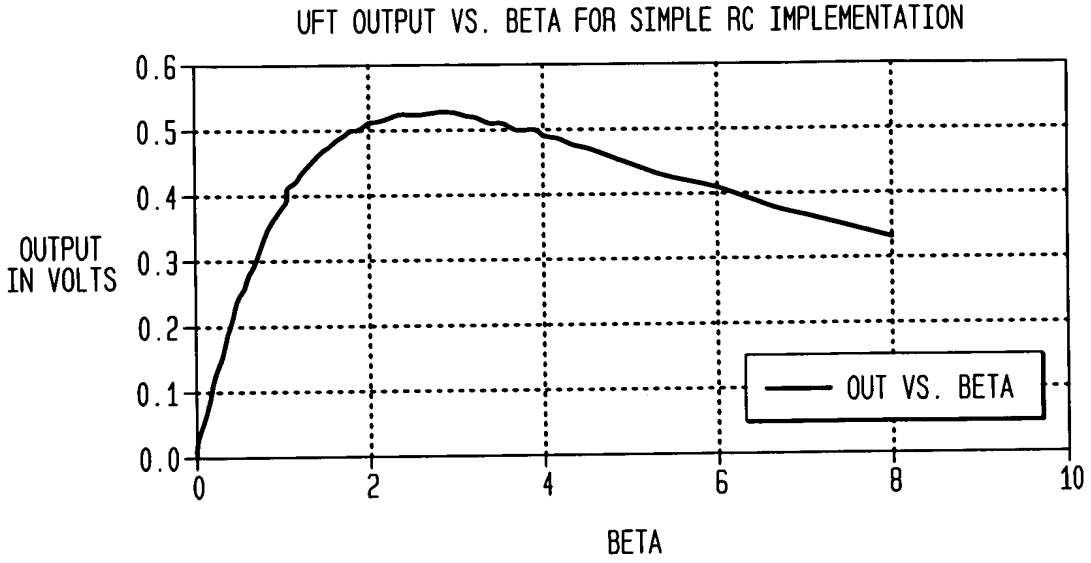



FIG. 169

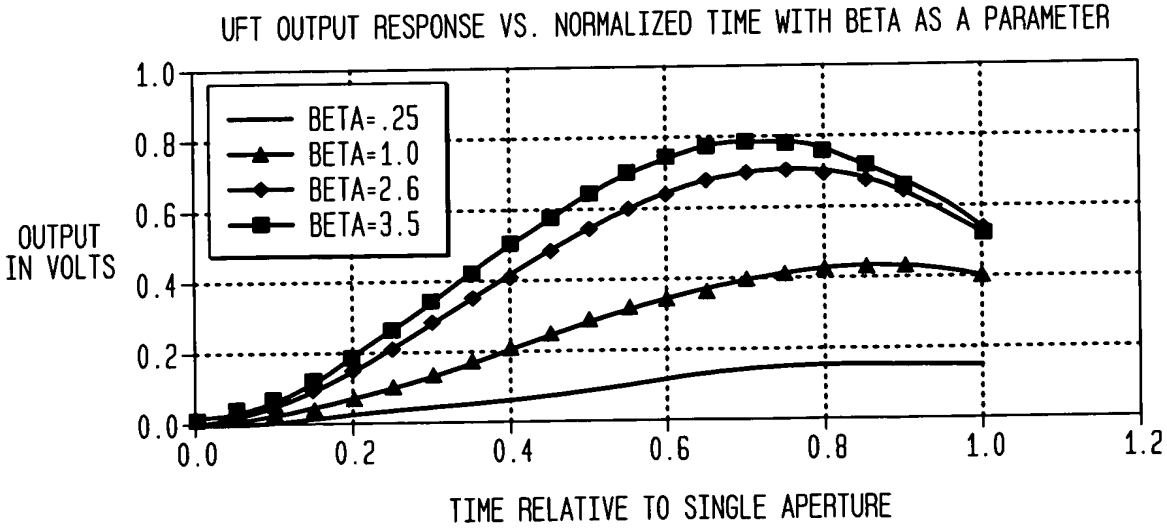


FIG. 170

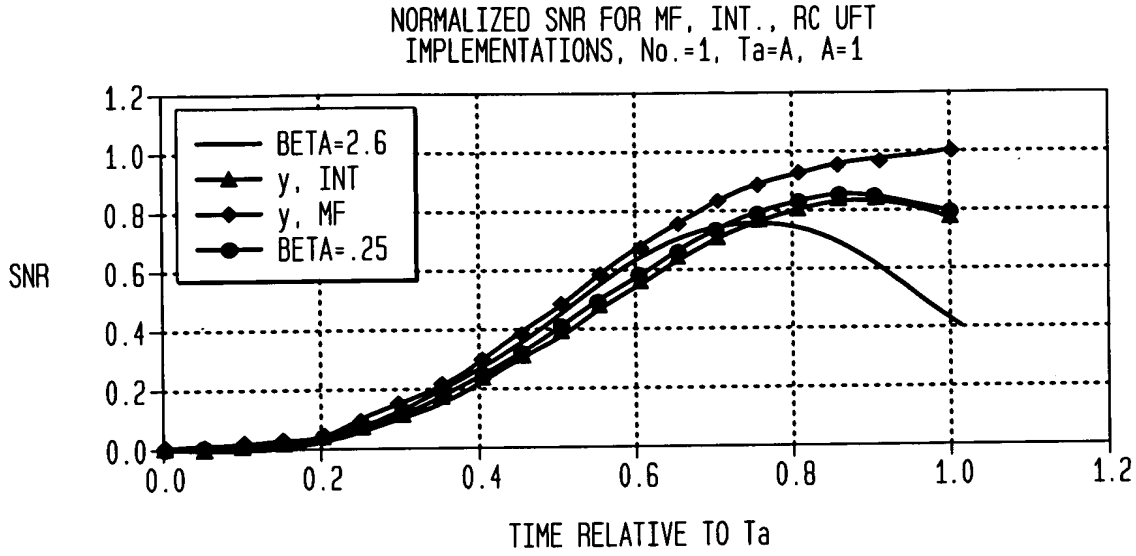



FIG. 171

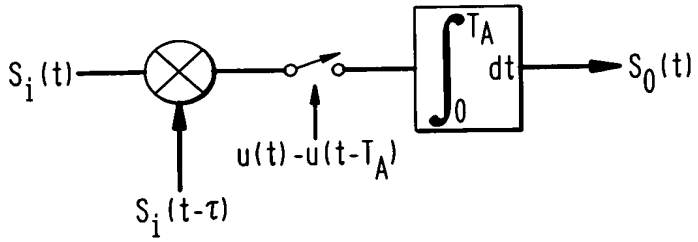


FIG. 172

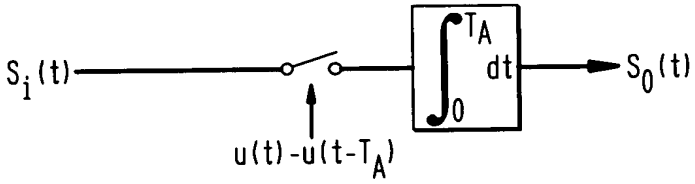



FIG. 173

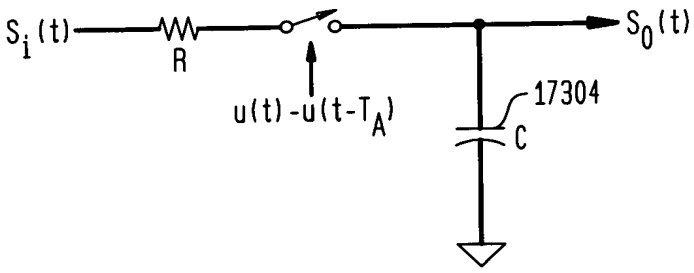


FIG. 174

UFT OUTPUT CHARGE TRANSFER

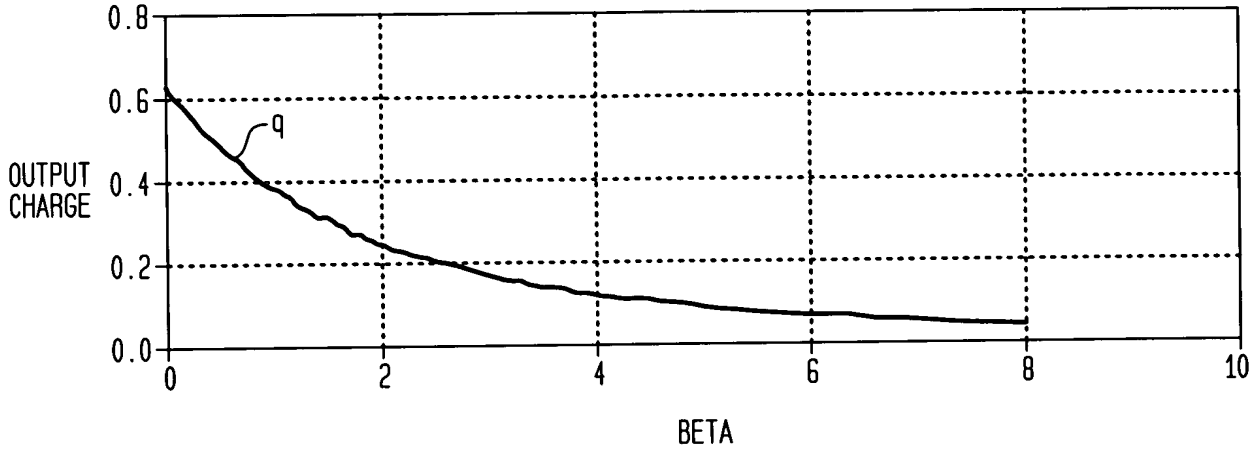



FIG. 175A

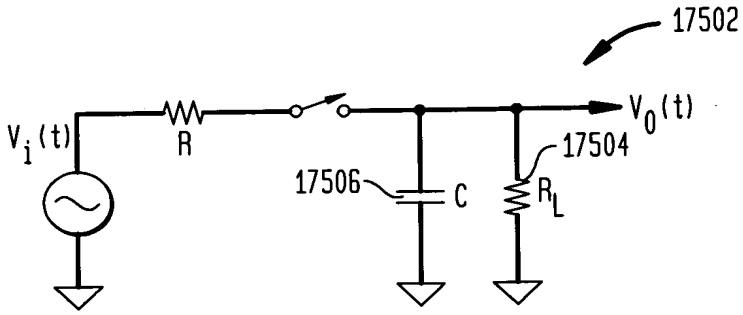


FIG. 175B

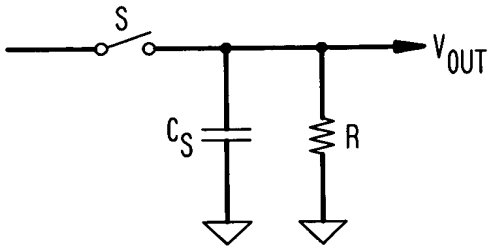



FIG. 175C

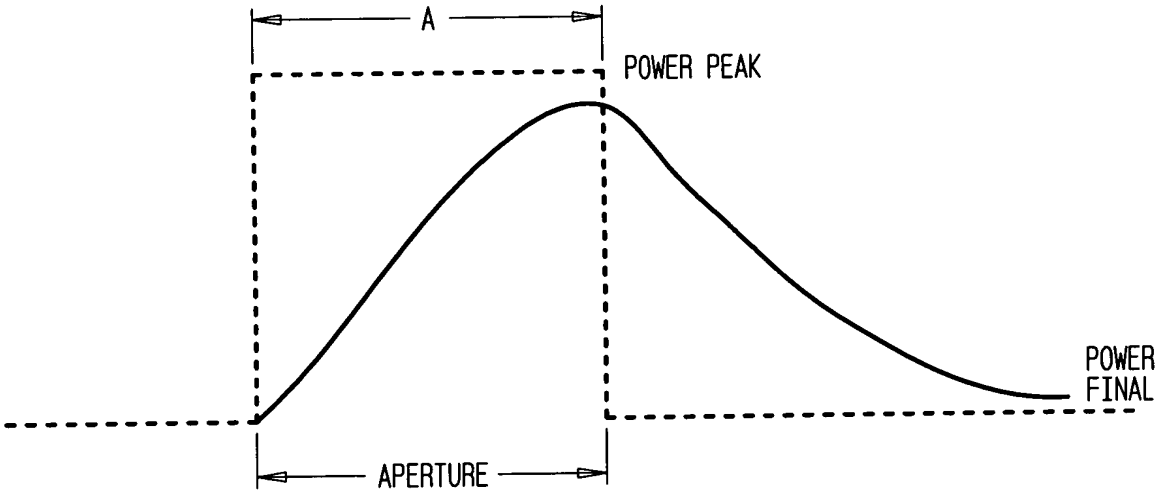



FIG. 175D

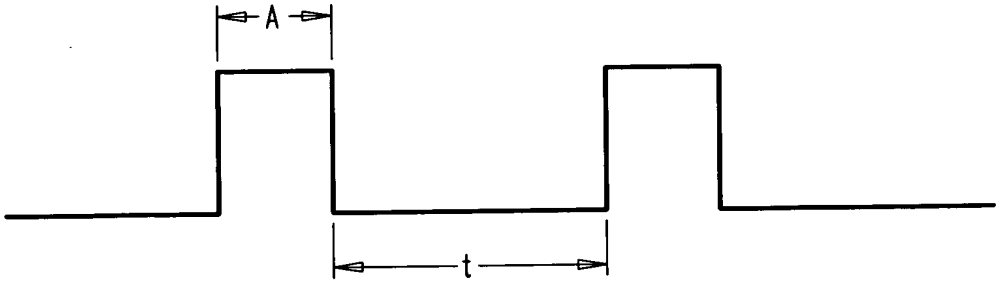


FIG. 176

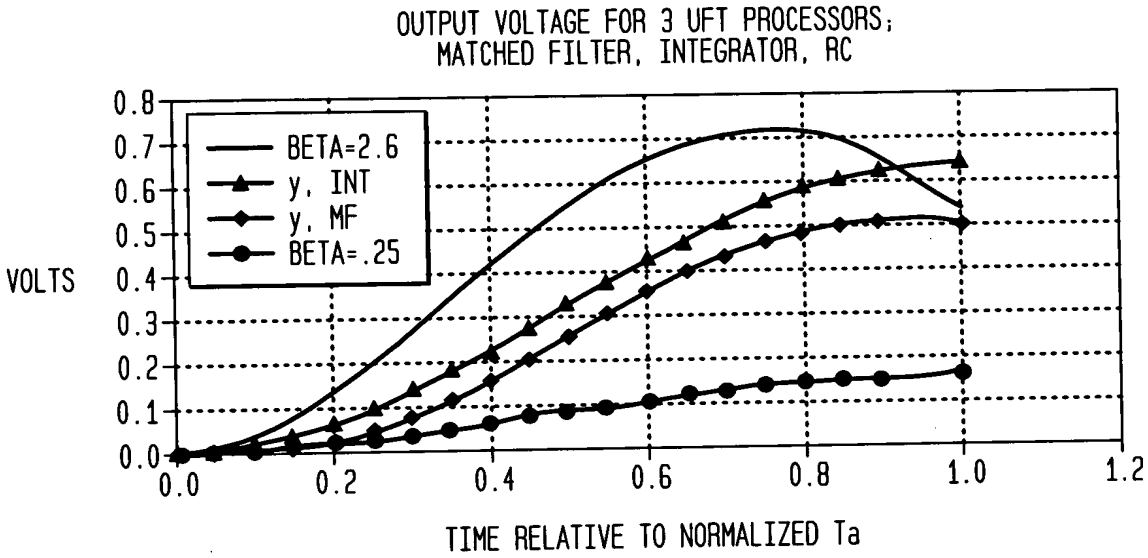
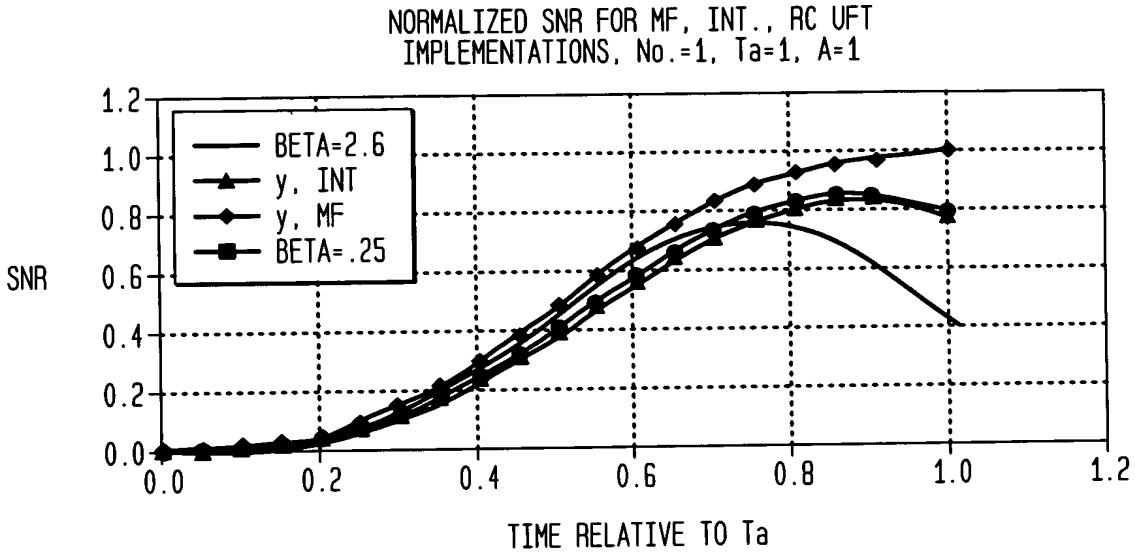

OUTPUT VOLTAGE FOR 3 UFT PROCESSORS;
MATCHED FILTER, INTEGRATOR, RC
VOLTS
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
BETA=2.6
y, INT
y, MF
BETA=.25
0.0
0.2
0.4
0.6
0.8
1.0
1.2
TIME RELATIVE TO NORMALIZED Ta

*FIG. 177A*


NORMALIZED SNR FOR MF, INT., RC UFT
IMPLEMENTATIONS, No.=1, Ta=1, A=1
SNR
1.2
1.0
0.8
0.6
0.4
0.2
0.0
BETA=2.6
y, INT
y, MF
BETA=.25
0.0
0.2
0.4
0.6
0.8
1.0
1.2
TIME RELATIVE TO Ta

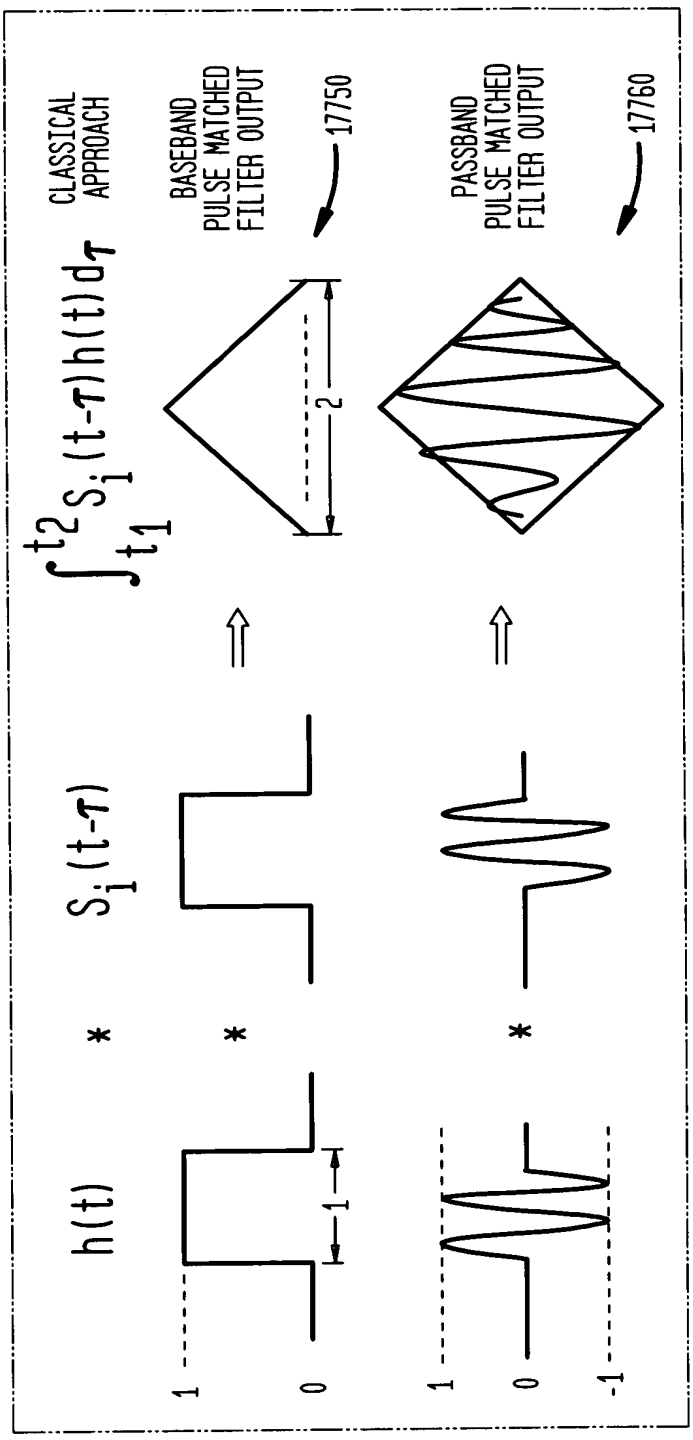



FIG. 177B

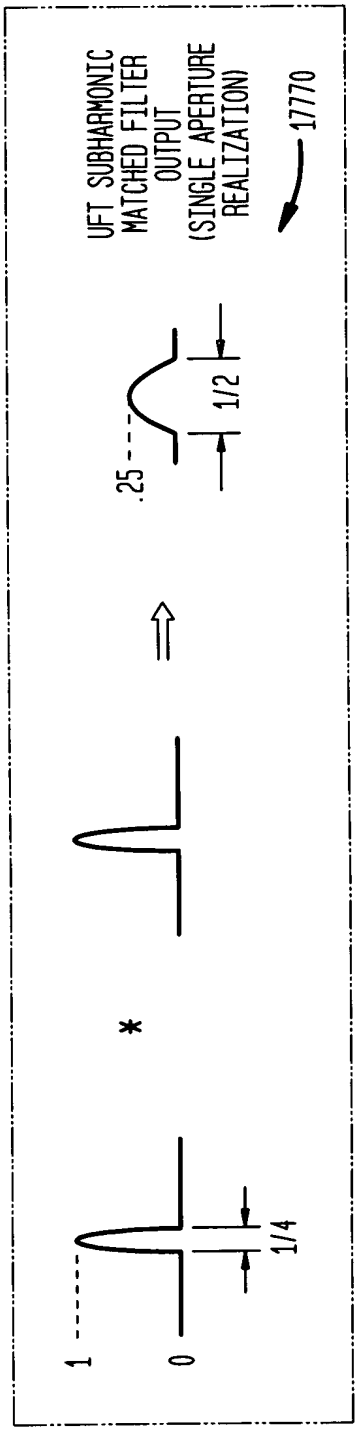



FIG. 177C

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FIG. 177D

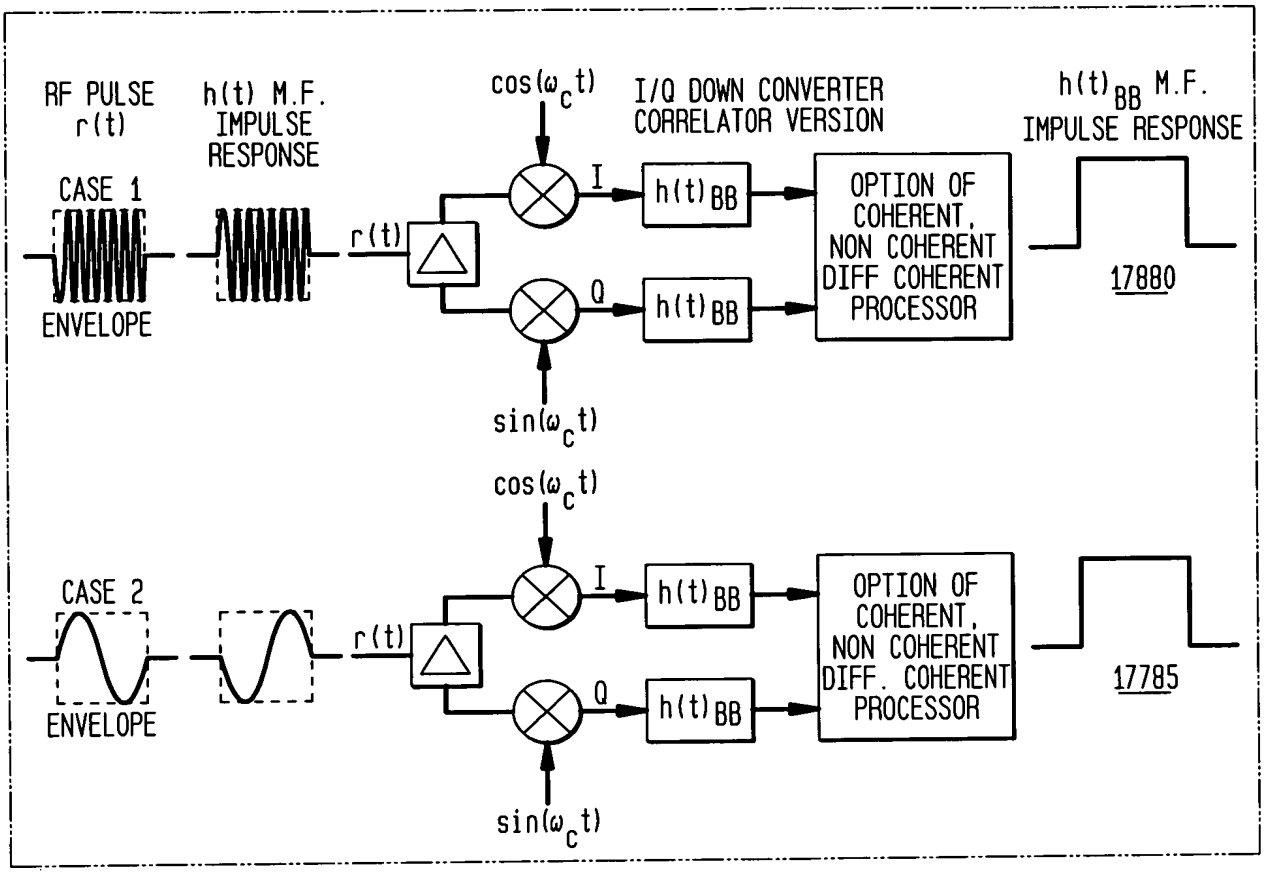


FIG. 177E

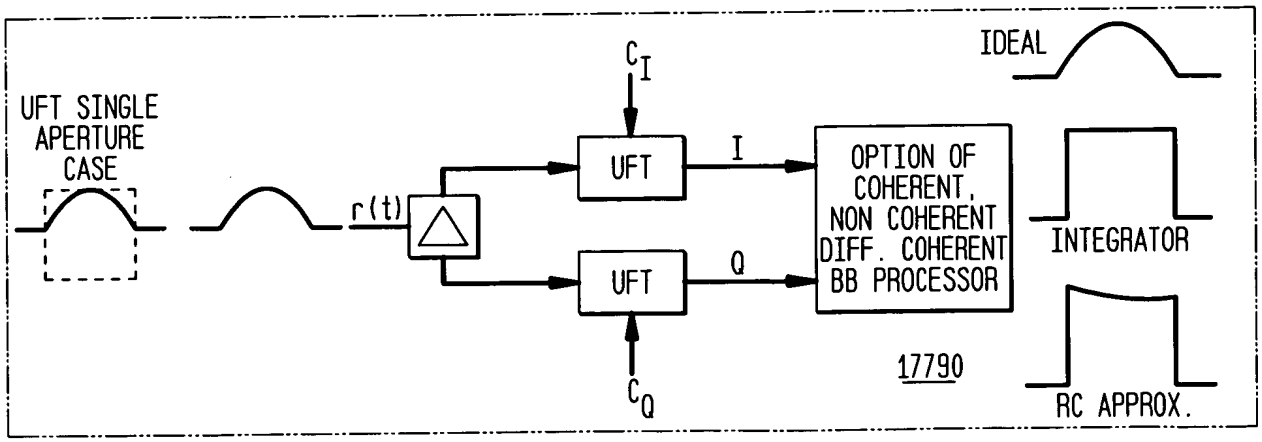

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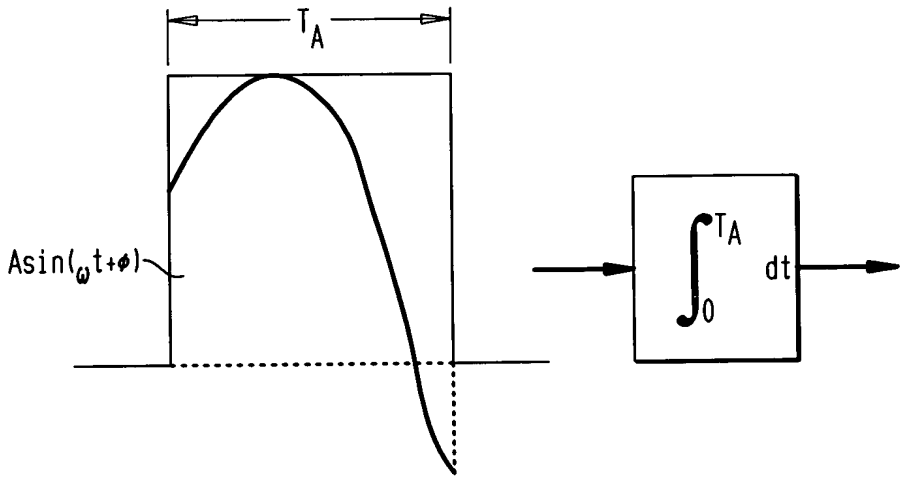
FIG. 177F




$$\int_0^{T_A} Au(t-T_A)\sin(\omega t+\phi)\,dt = \int_0^{T_A} A(u(t-T_A)\cos\phi\sin(\omega t)+u(t-T_A)\sin\phi\cos(\omega t))\,dt$$

$$= A\cos(\phi)\underbrace{\int_0^{T_A} u(t-T_A)\sin(\omega t)\,dt}_{\text{CONSTANT}\quad \text{UFT CORRELATOR KERNEL}} + A\sin(\phi)\underbrace{\int_0^{T_A} u(t-T_A)\cos(\omega t)\,dt}_{\text{CONSTANT}\qquad =0}$$

$$= A\cos(\phi)\int_0^{T_A} u(t-T_A)\sin(\omega t)\,dt$$

- A IS CONSTANT ON A SINE TO SINE BASIS
- $\phi$ IS CONSTANT ON A SINE TO SINE BASIS
- i.e., THE MODULATION RATE DUE TO INFORMATION FOR PHASE AND AMPLITUDE IS VERY SLOW COMPARED TO CARRIER FREQUENCY

FIG. 178A

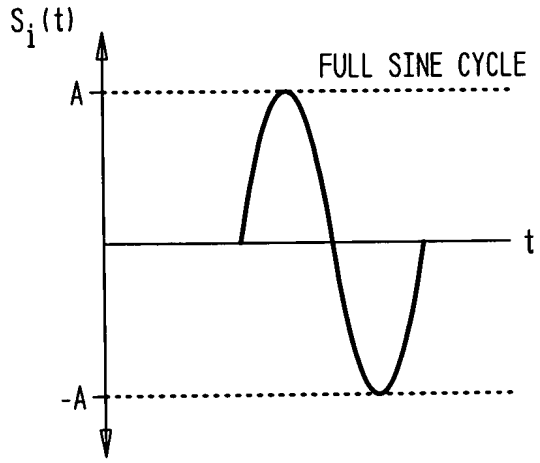



FIG. 178B

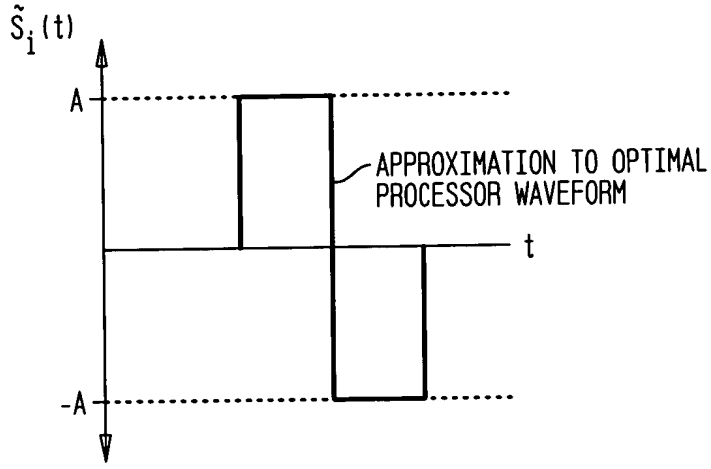


FIG. 179

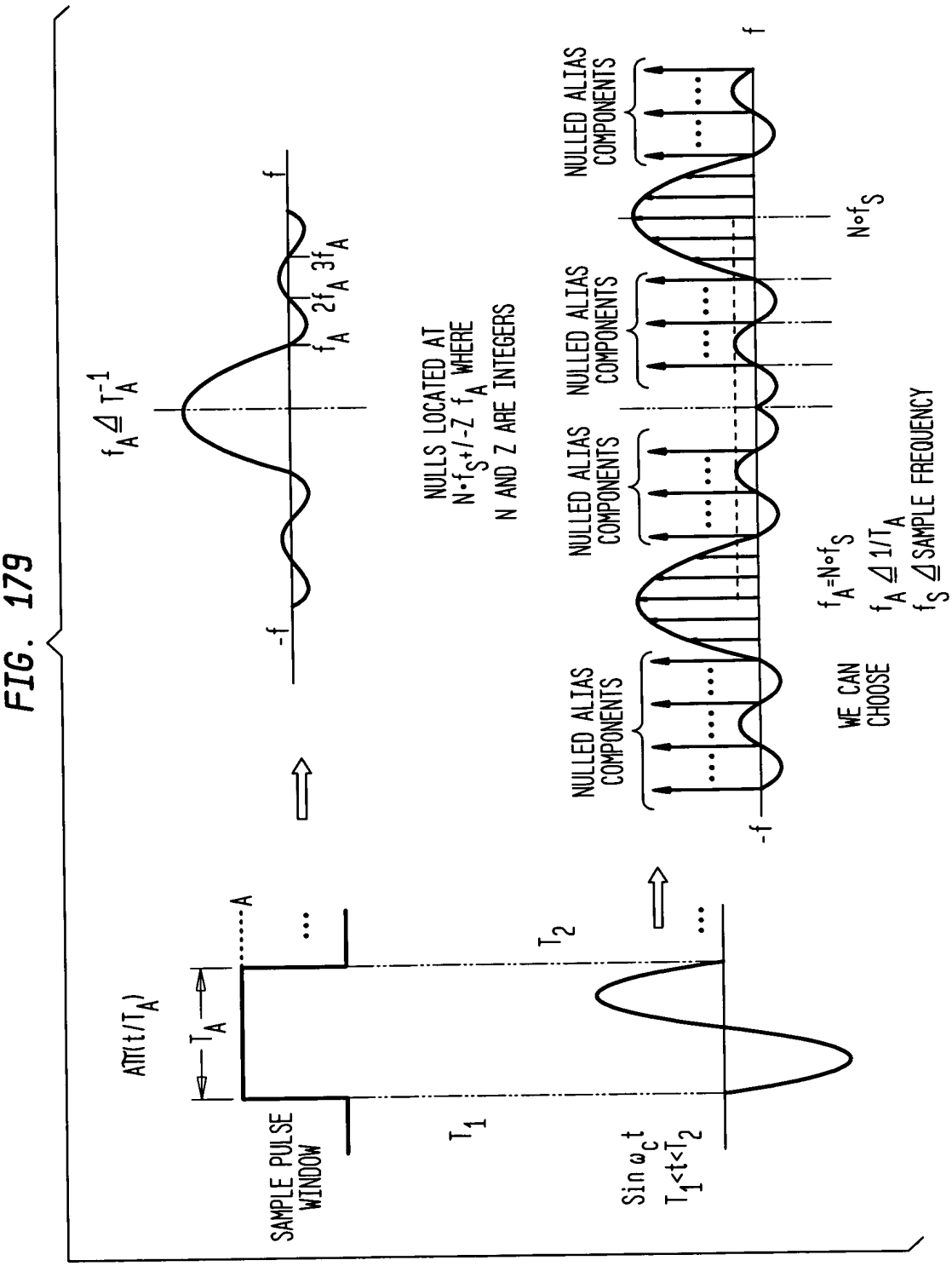
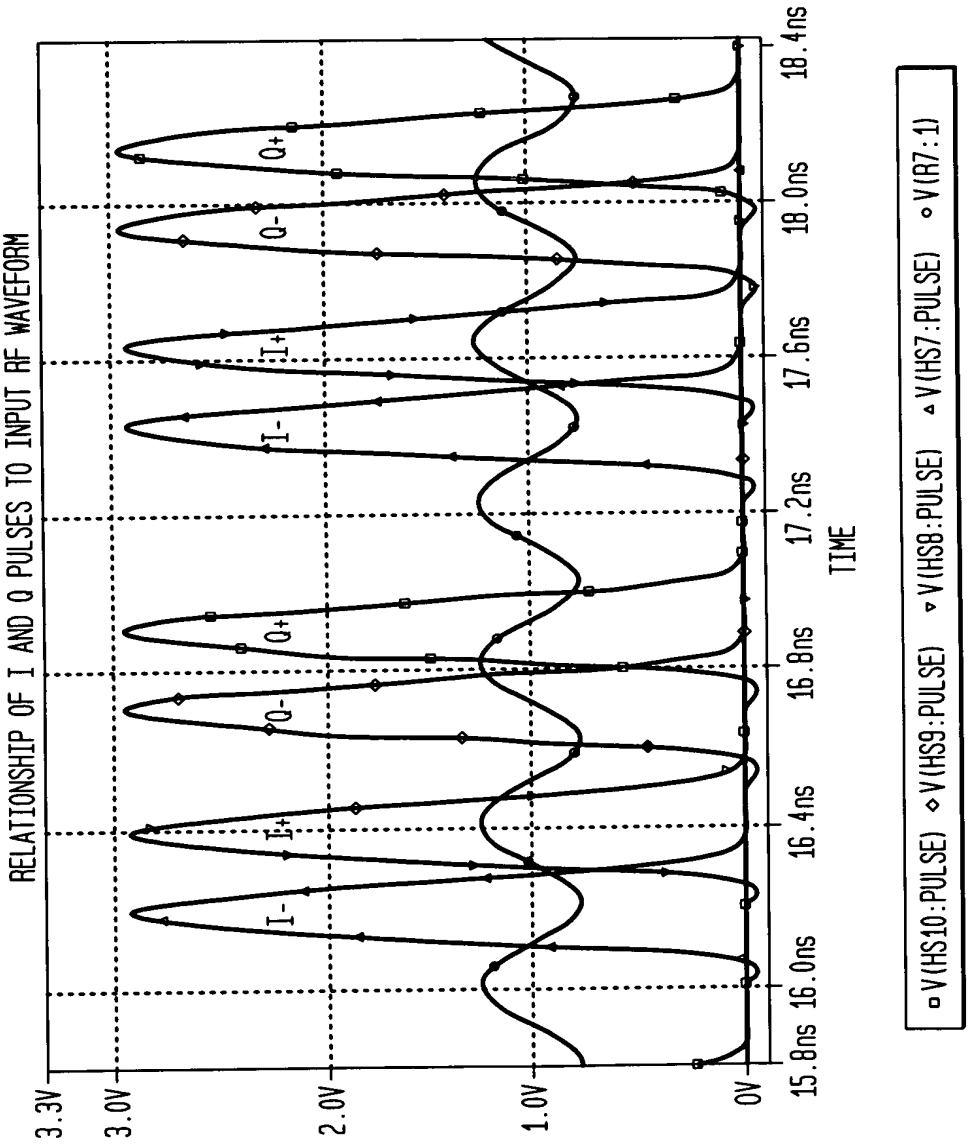

$f_A \triangleq T_A^{-1}$
$-f$
$f$
$f_A$ $2f_A$ $3f_A$
NULLS LOCATED AT
$N \cdot f_S +/- Z f_A$ WHERE
N AND Z ARE INTEGERS
NULLED ALIAS COMPONENTS
NULLED ALIAS COMPONENTS
NULLED ALIAS COMPONENTS
NULLED ALIAS COMPONENTS
$N \cdot f_S$
$f_A = N \cdot f_S$
WE CAN CHOOSE
$f_A \triangleq 1/T_A$
$f_S \triangleq$ SAMPLE FREQUENCY
$A\Pi(t/T_A)$
$T_A$
A
$T_1$
$T_2$
SAMPLE PULSE WINDOW
$\sin \omega_c t$
$T_1 < t < T_2$

FIG. 180


RELATIONSHIP OF I AND Q PULSES TO INPUT RF WAVEFORM
3.3V
3.0V
2.0V
1.0V
0V
15.8ns
16.0ns
16.4ns
16.8ns
17.2ns
17.6ns
18.0ns
18.4ns
TIME
I-
I+
Q-
Q+
V(HS10:PULSE)
V(HS9:PULSE)
V(HS8:PULSE)
V(HS7:PULSE)
V(R7:1)

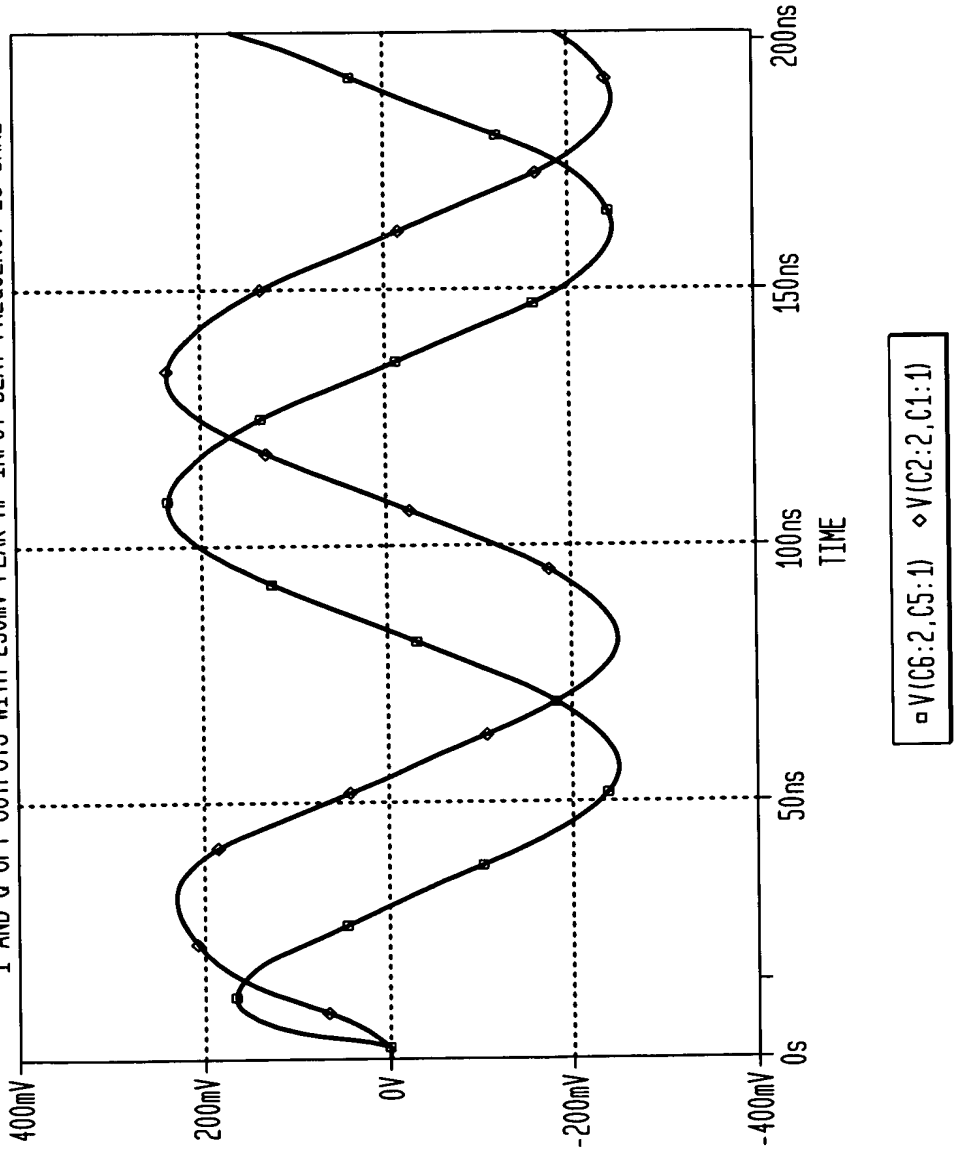

I AND Q UFT OUTPUTS WITH 250mV PEAK RF INPUT BEAT FREQUENCY IS 9MHz
400mV
200mV
0V
-200mV
-400mV
0s
50ns
100ns
150ns
200ns
TIME
V(C6:2,C5:1)
V(C2:2,C1:1)

FIG. 181

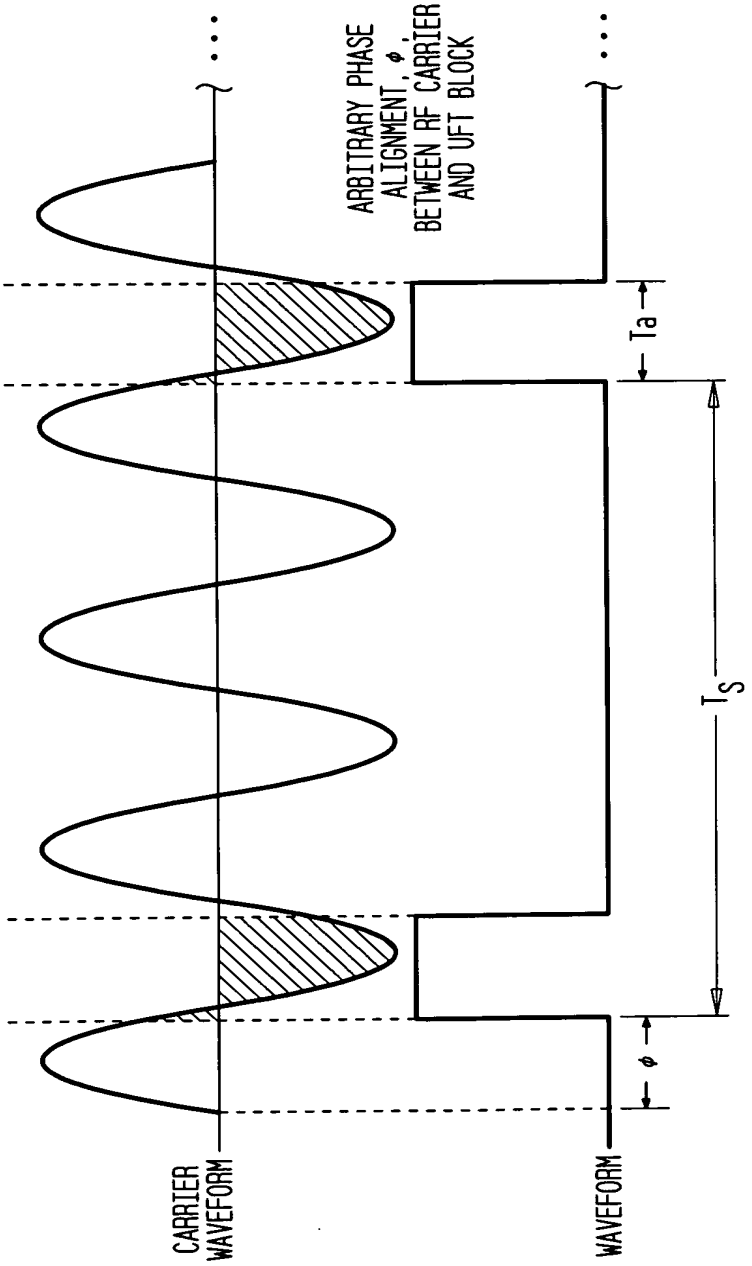

ARBITRARY PHASE
ALIGNMENT, ϕ,
BETWEEN RF CARRIER
AND UFT BLOCK
Ta
Ts
ϕ
CARRIER
WAVEFORM
WAVEFORM

FIG. 182

FIG. 183

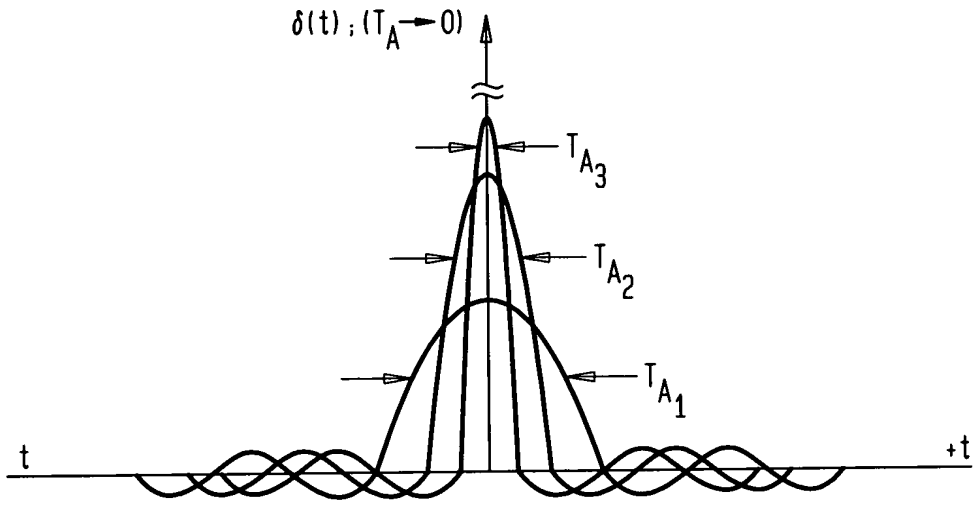



FIG. 184

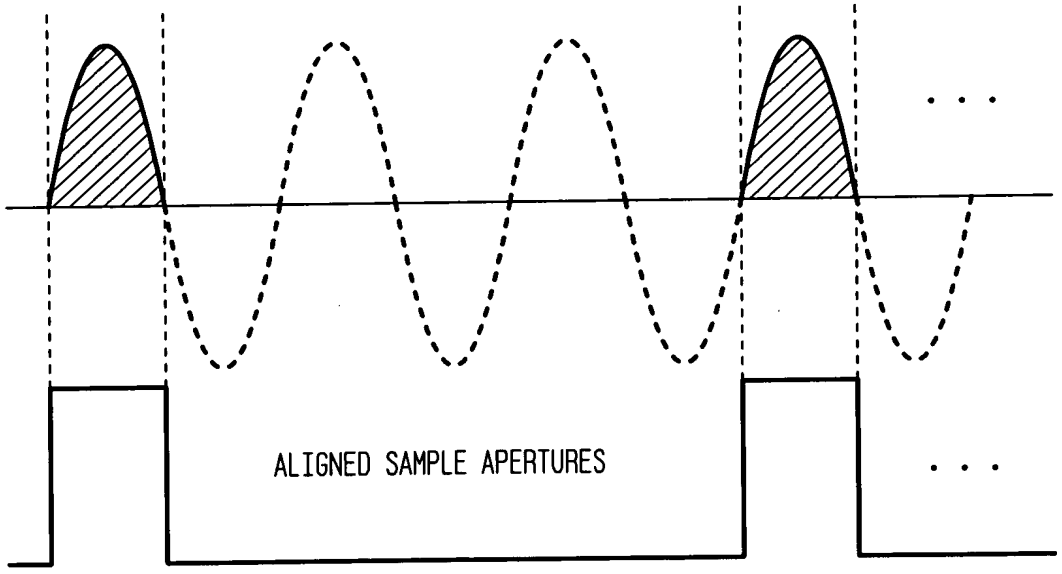


FIG. 185

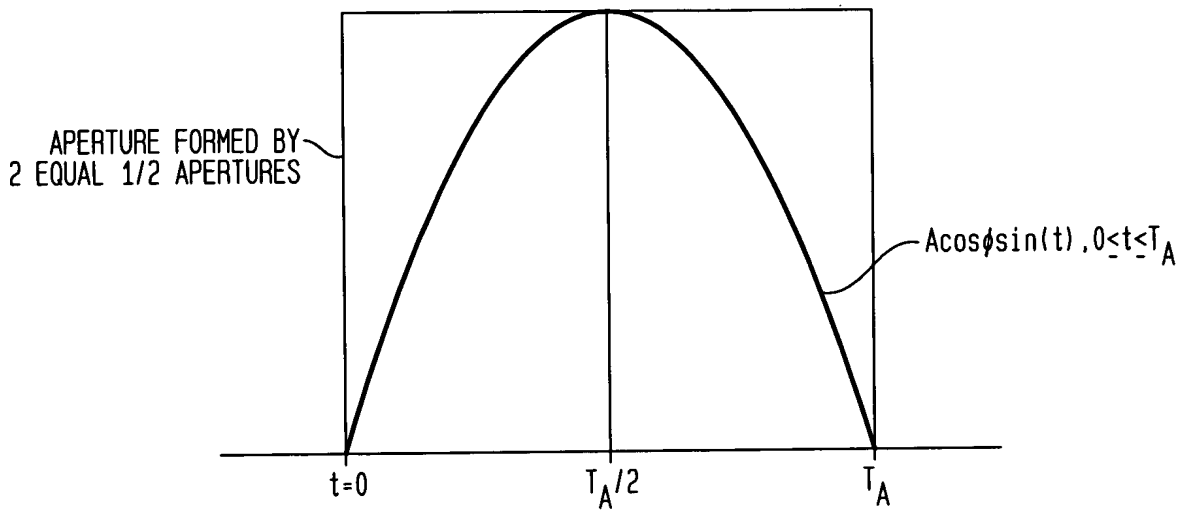



FIG. 186

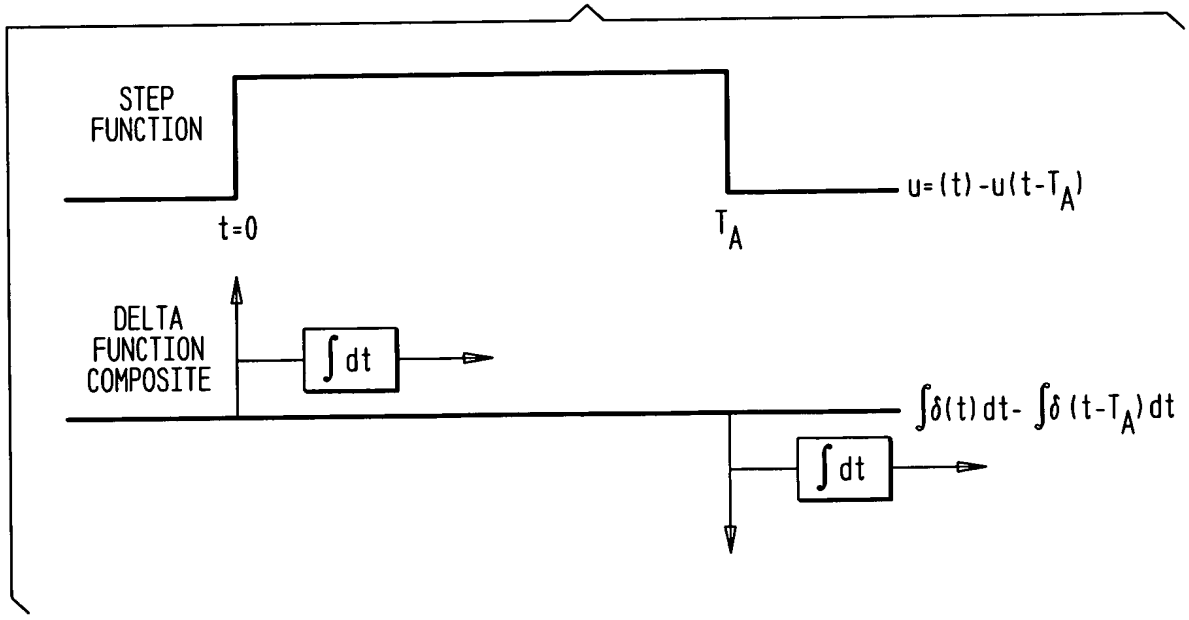


FIG. 187

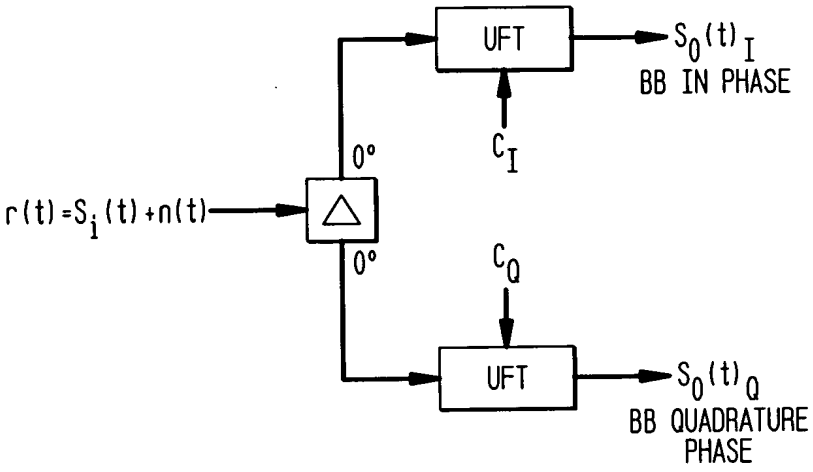



FIG. 188

$$C_I(t)=\sum_{m=-\infty}^{\infty}\delta(t-mT_S)*p_C(t)=\sum_{m=-\infty}^{\infty}p(t-mT_S) \qquad 18802$$

$$C_I(t)=\sum_{m=-\infty}^{\infty}(u(t)-u(t-T_A))*\delta(t-mT_S) \qquad 18804$$

$$C_Q(t)=\sum_{m=-\infty}^{\infty}(u[t-T_A/2]-u[t-3T_A/2])*\delta(t-(mT_S+T_A/2)) \qquad 18806$$

FIG. 189

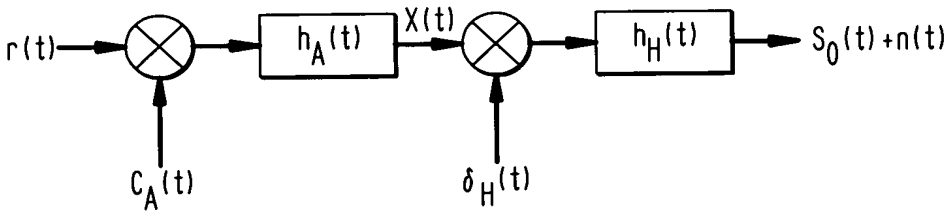


FIG. 190

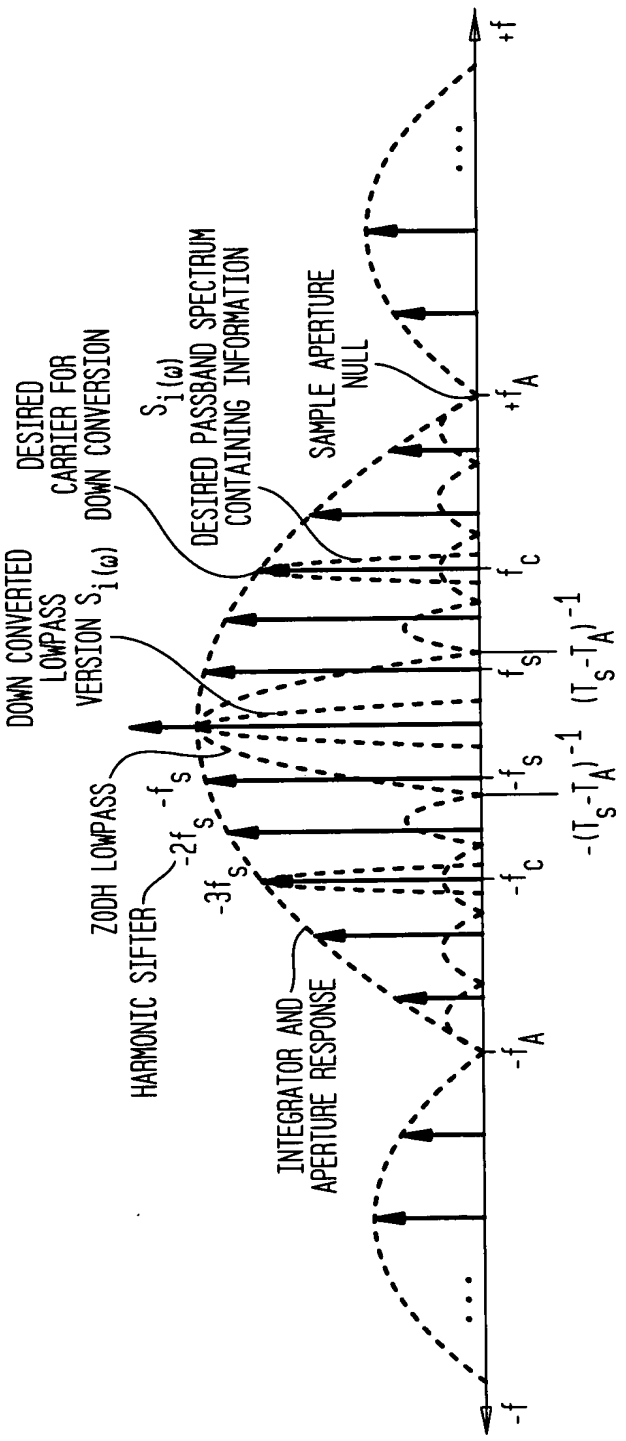

DESIRED CARRIER FOR DOWN CONVERSION
$S_{i(\omega)}$ DESIRED PASSBAND SPECTRUM CONTAINING INFORMATION
SAMPLE APERTURE NULL
DOWN CONVERTED LOWPASS VERSION $S_{i(\omega)}$
ZODH LOWPASS
HARMONIC SIFTER
INTEGRATOR AND APERTURE RESPONSE
+f
$+f_A$
$f_c$
$f_s$
$-f_s$
$-2f_s$
$-3f_s$
$-f_c$
$-f_A$
-f
$-(T_s-T_A)^{-1}$
$(T_s-T_A)^{-1}$

FIG. 191

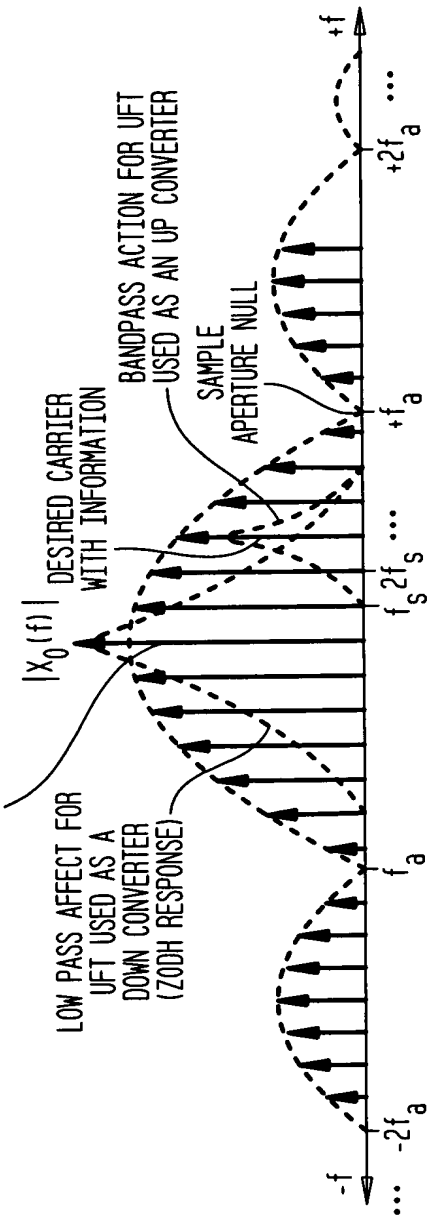



FIG. 192

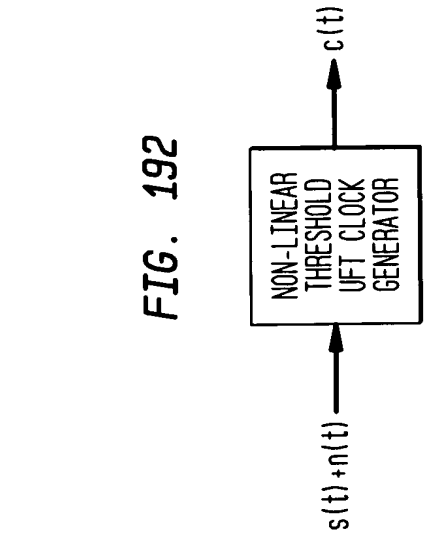
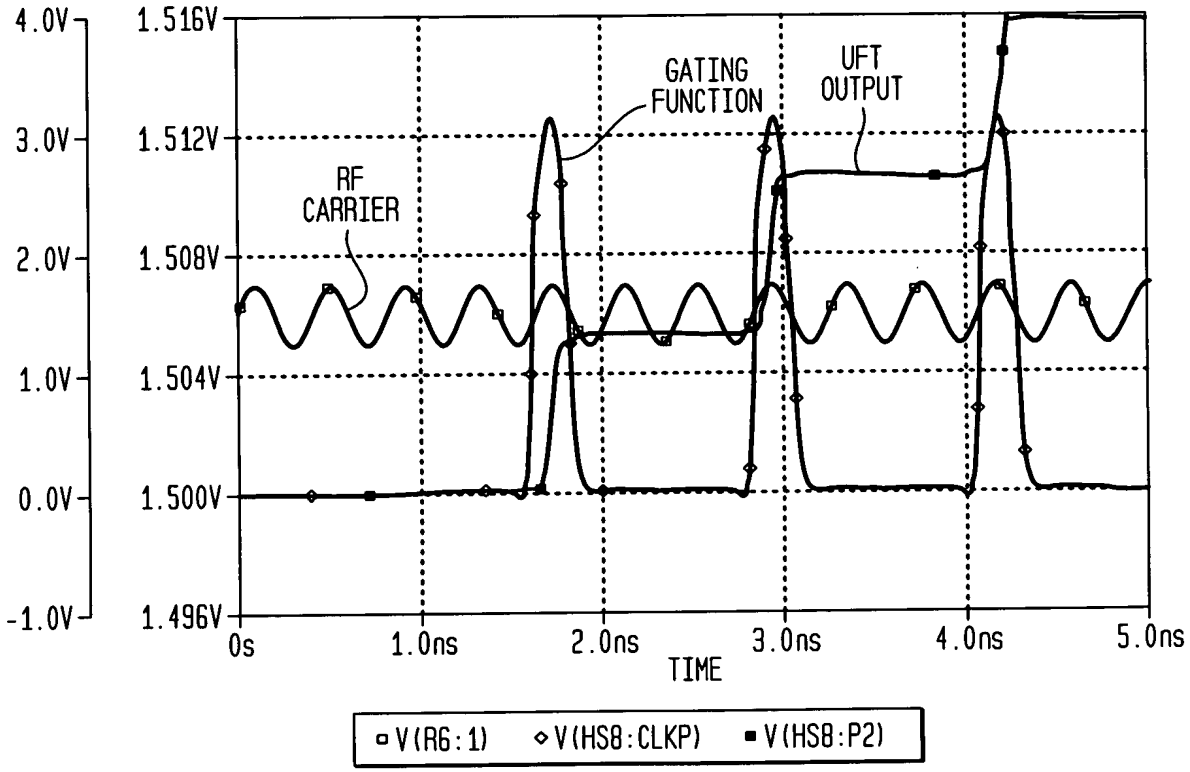


FIG. 193


4.0V
3.0V
2.0V
1.0V
0.0V
-1.0V
1.516V
1.512V
1.508V
1.504V
1.500V
1.496V
GATING FUNCTION
UFT OUTPUT
RF CARRIER
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
TIME
V(R6:1)
V(HS8:CLKP)
V(HS8:P2)

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Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 194

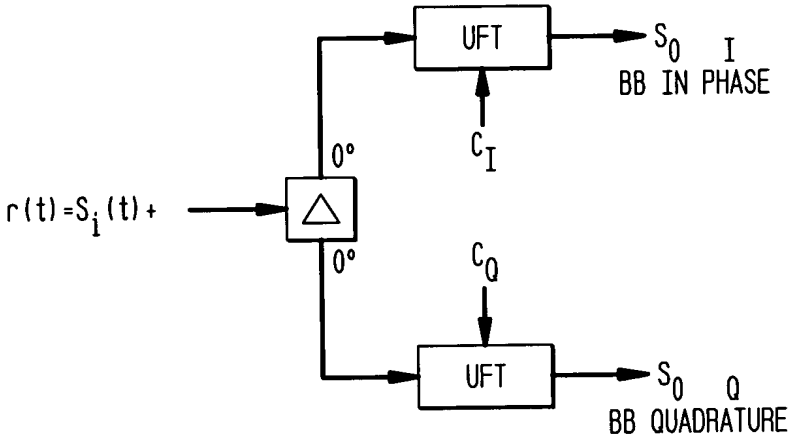


FIG. 195

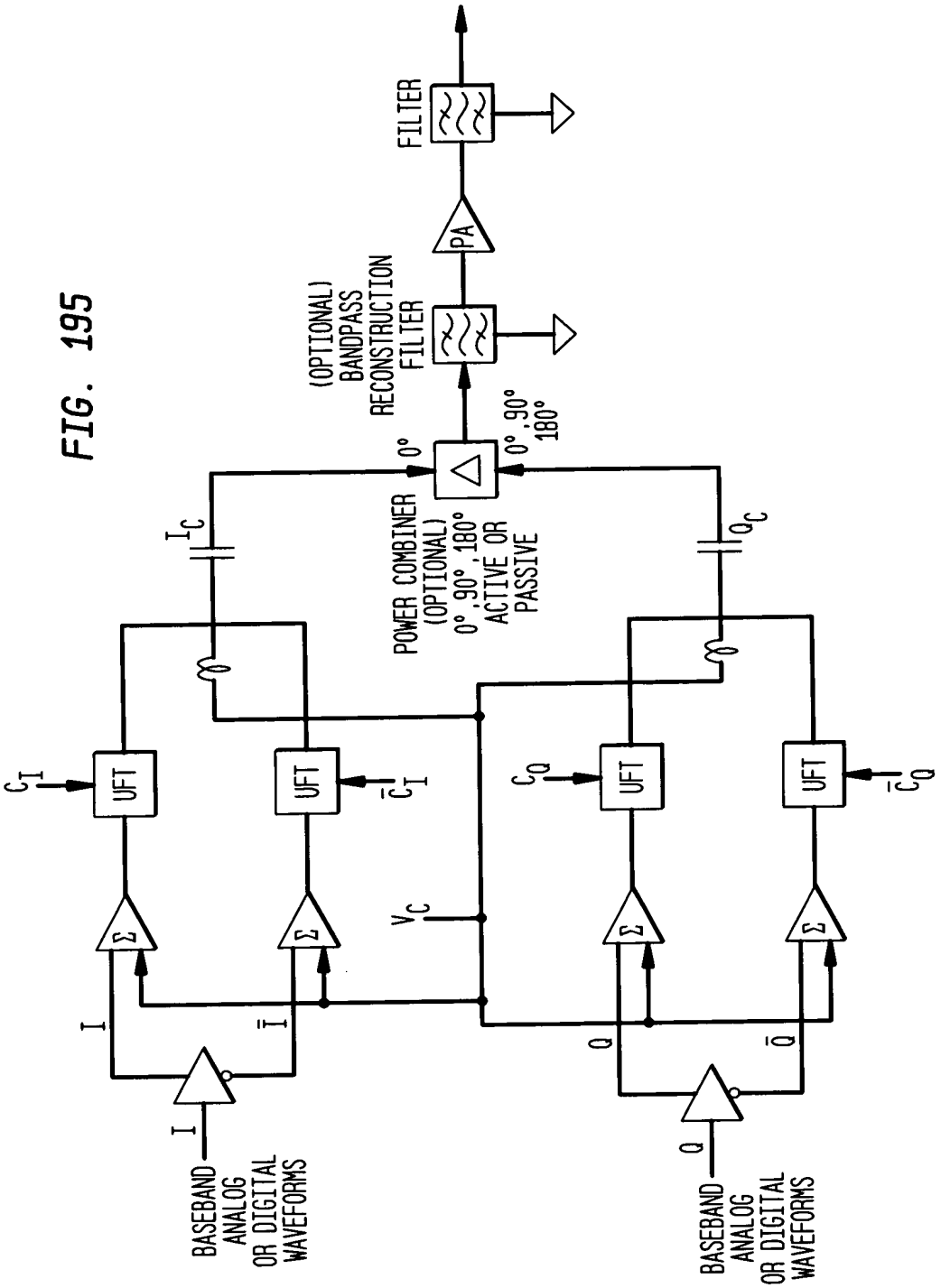

FILTER
PA
(OPTIONAL) BANDPASS RECONSTRUCTION FILTER
0°
0°,90° 180°
POWER COMBINER (OPTIONAL) 0°,90°,180° ACTIVE OR PASSIVE
$I_C$
$Q_C$
$C_I$
UFT
$\bar{C}_I$
$C_Q$
$\bar{C}_Q$
$V_C$
Σ
I
$\bar{I}$
Q
$\bar{Q}$
BASEBAND ANALOG OR DIGITAL WAVEFORMS

FIG. 196

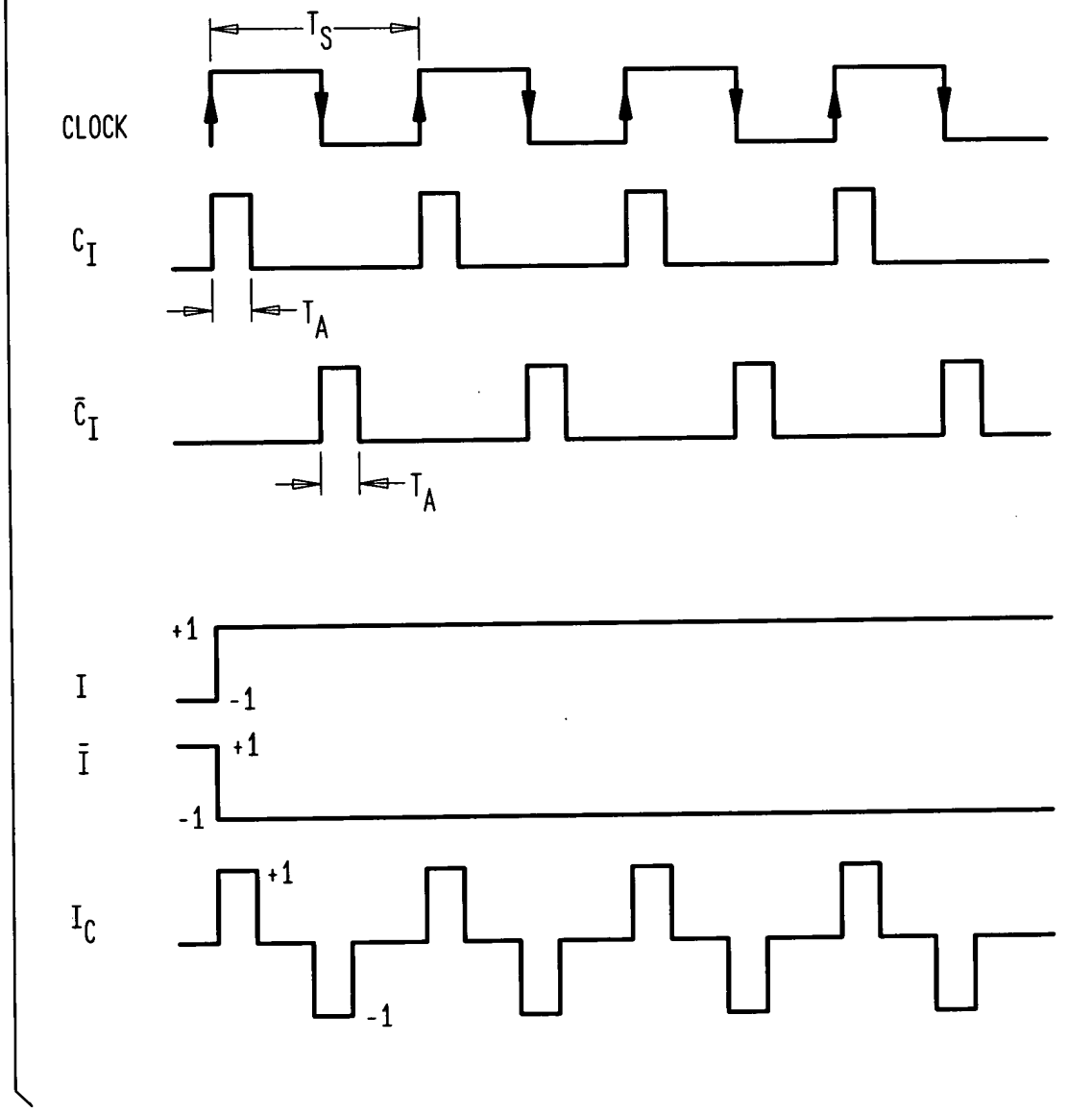


FIG. 197

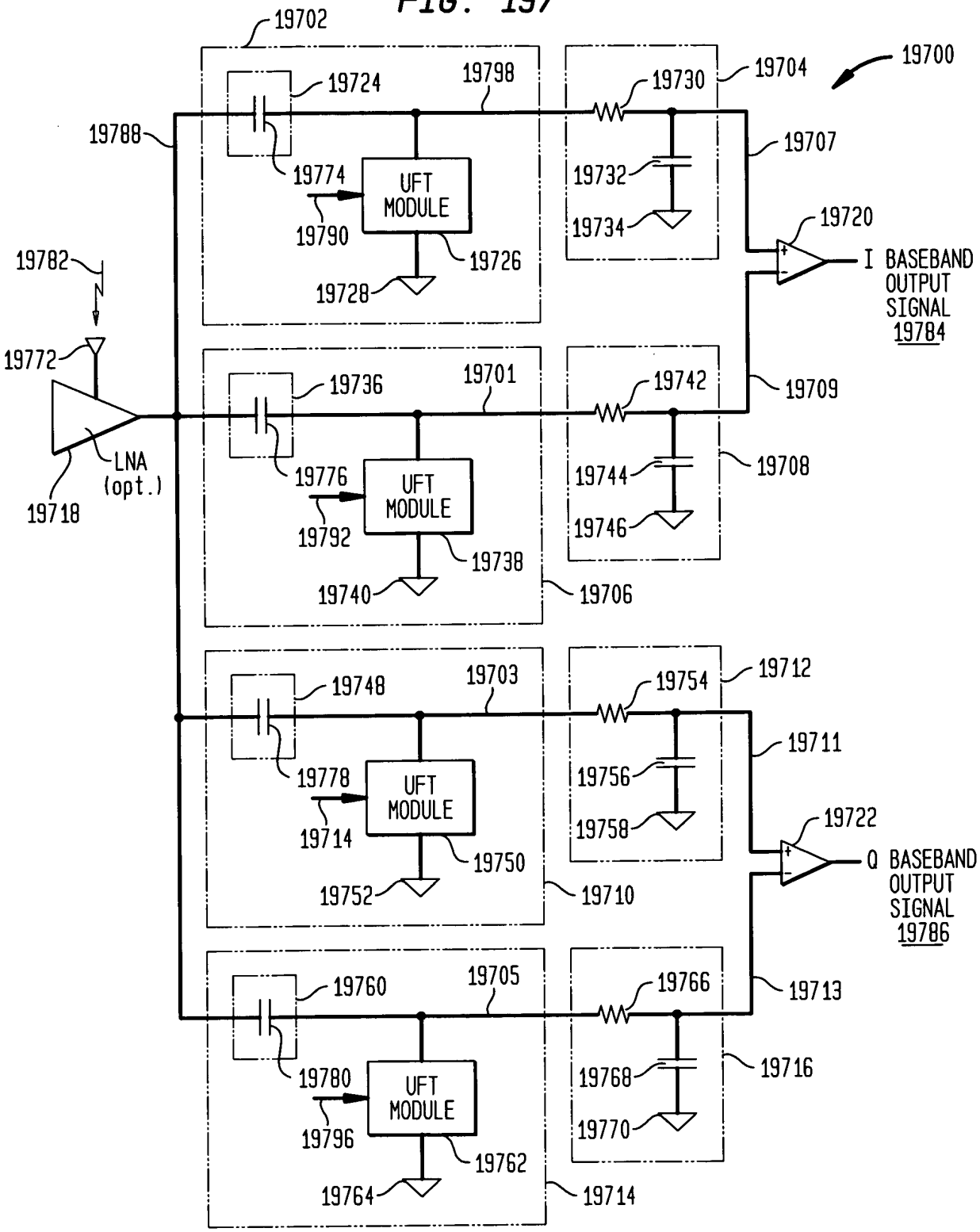

19700
19702
19704
19706
19707
19708
19709
19710
19711
19712
19713
19714
19716
19718
19720
19722
19724
19726
19728
19730
19732
19734
19736
19738
19740
19742
19744
19746
19748
19750
19752
19754
19756
19758
19760
19762
19764
19766
19768
19770
19772
19774
19776
19778
19780
19782
19784
19786
19788
19790
19792
19796
19798
19701
19703
19705
UFT MODULE
LNA (opt.)
I BASEBAND OUTPUT SIGNAL
Q BASEBAND OUTPUT SIGNAL

FIG. 198

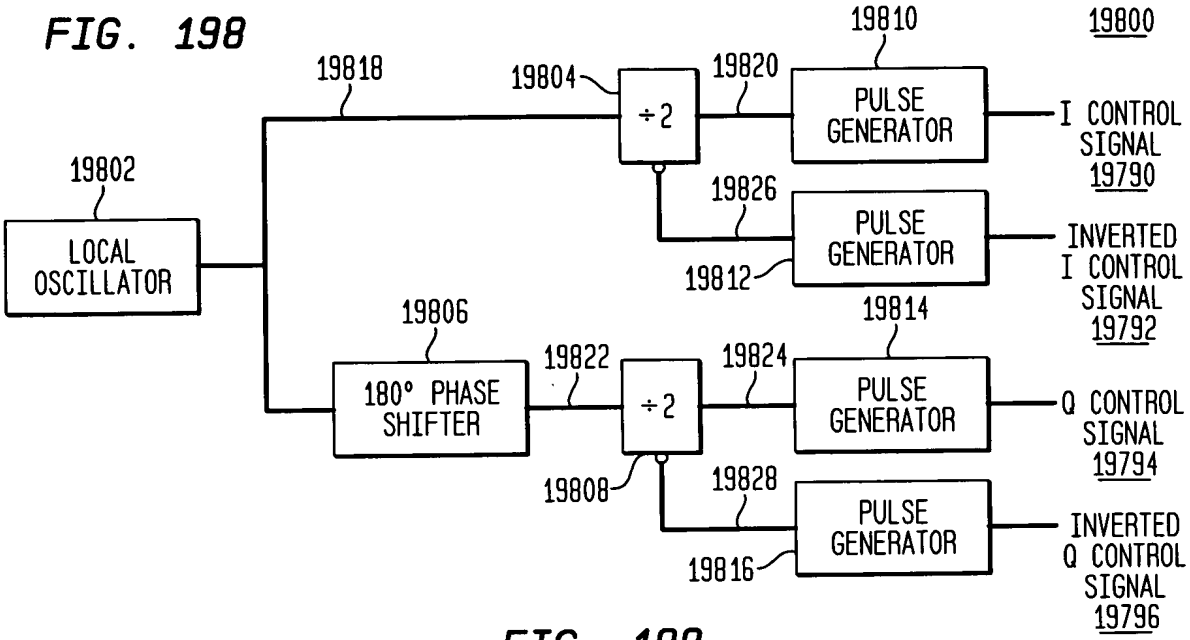



FIG. 199

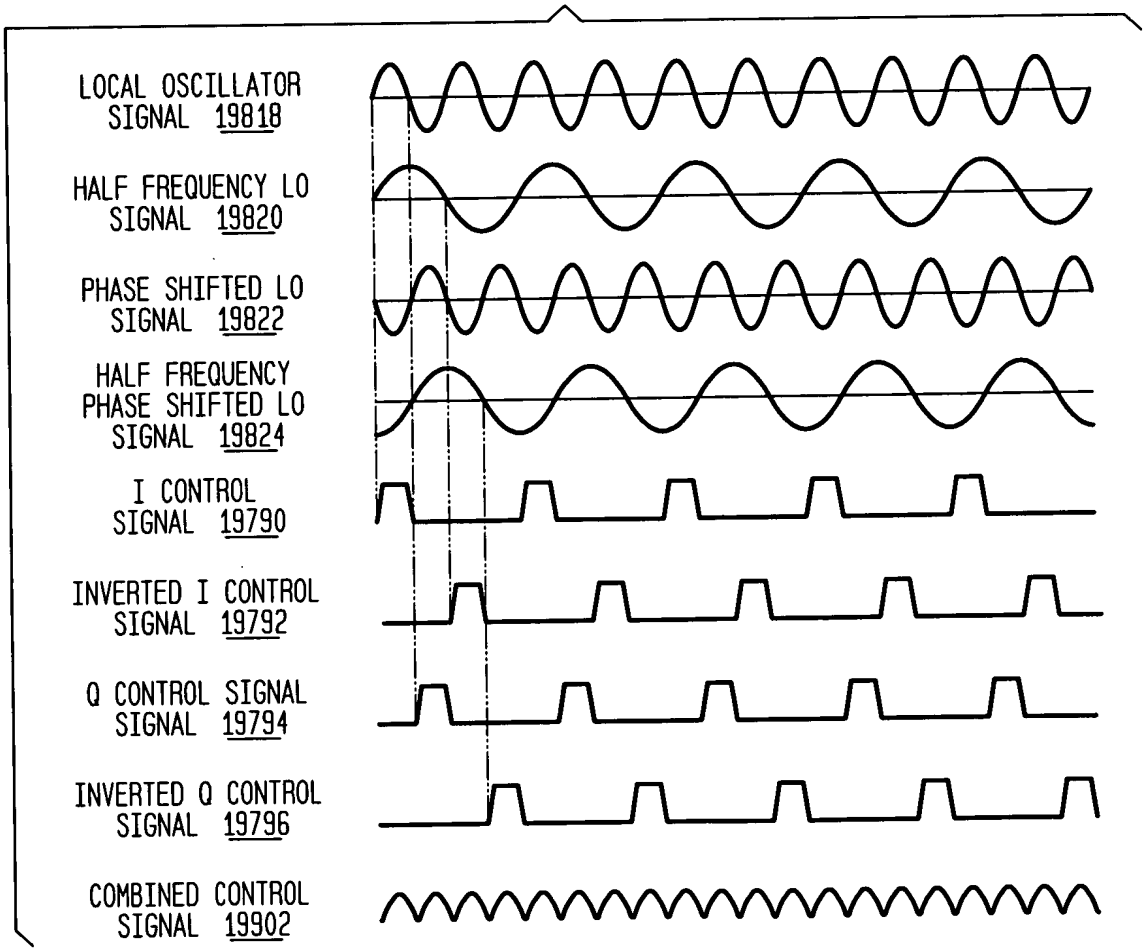
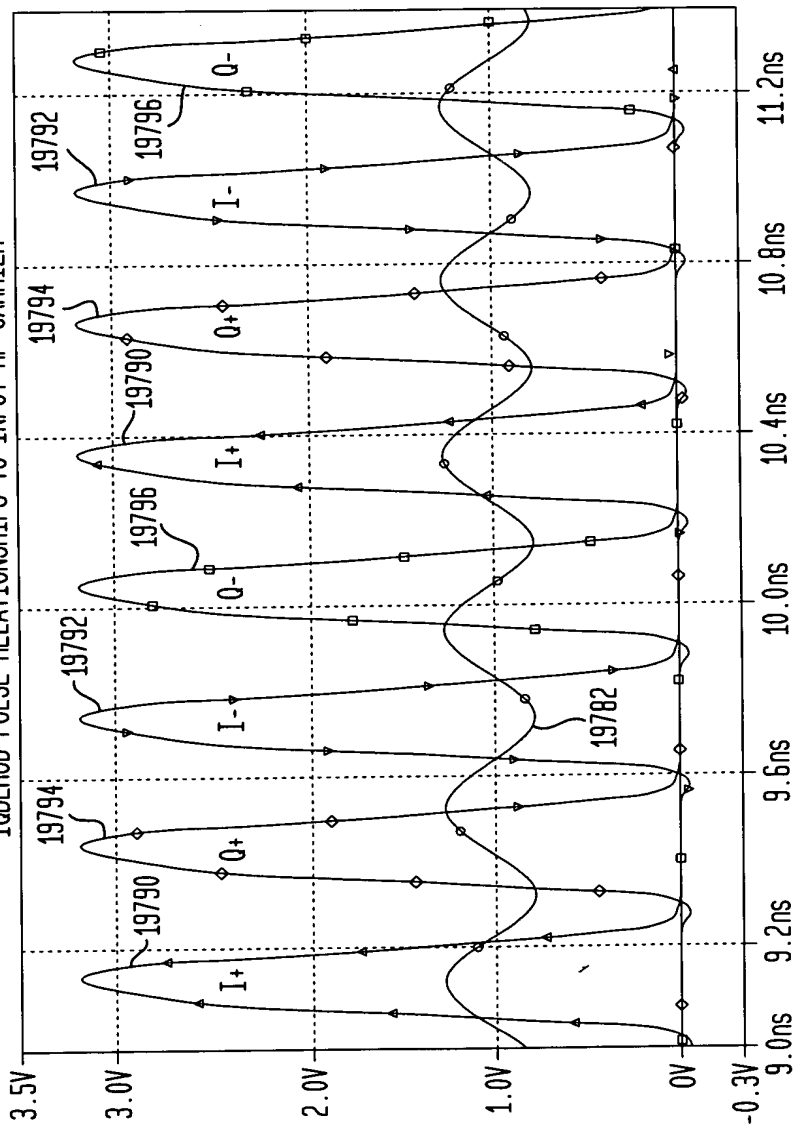


FIG. 200


IQDEMOD PULSE RELATIONSHIPS TO INPUT RF CARRIER
3.5V
3.0V
2.0V
1.0V
0V
-0.3V
9.0ns
9.2ns
9.6ns
10.0ns
10.4ns
10.8ns
11.2ns
19790
19792
19794
19796
19782
I+
I-
Q+
Q-

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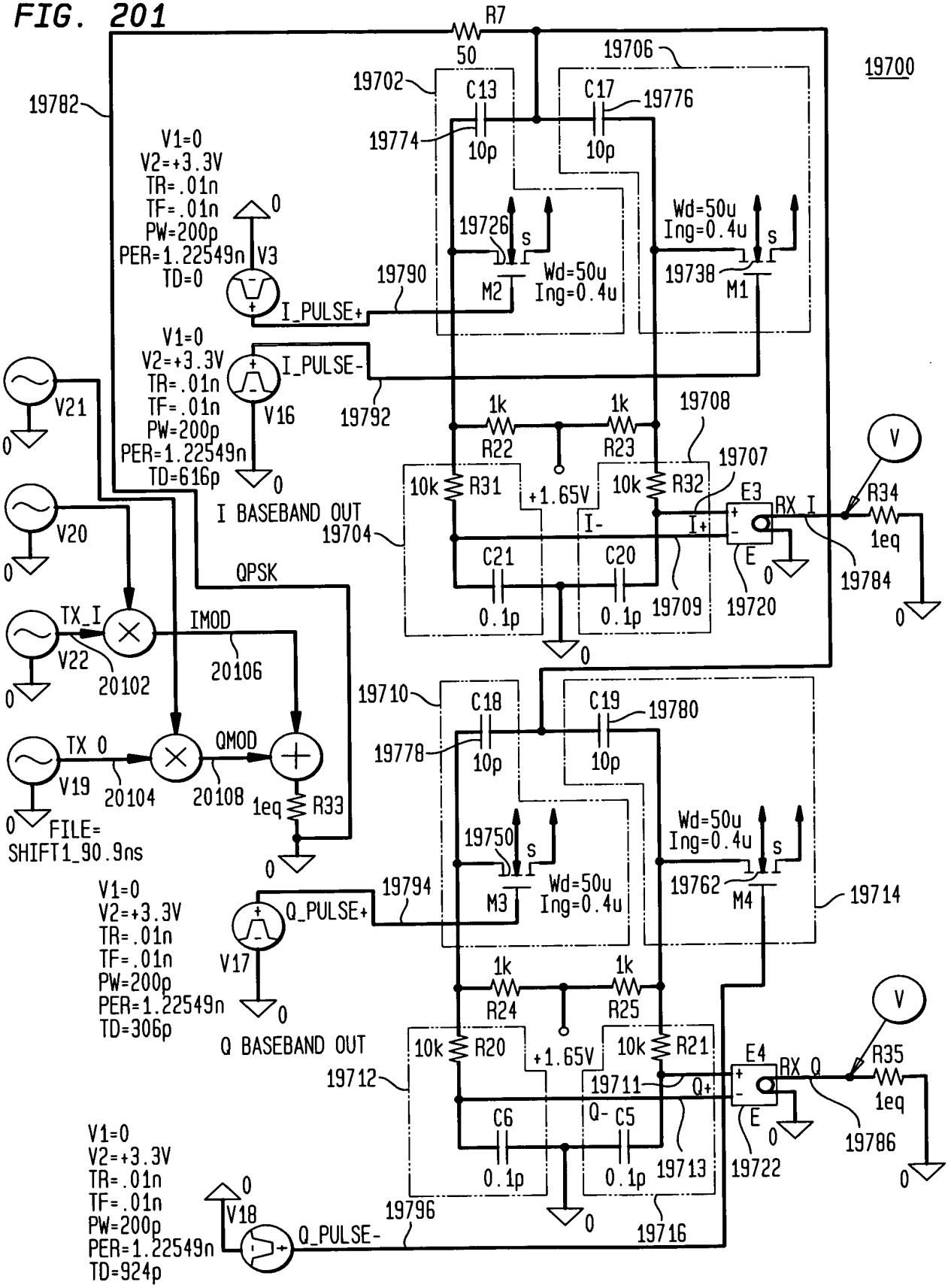
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 201



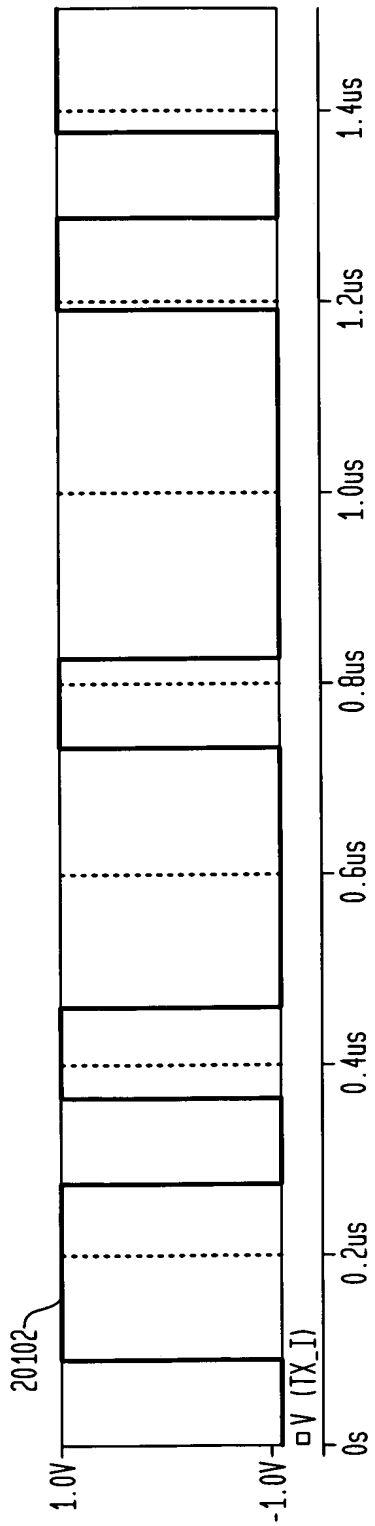



FIG. 202

IQDEMOD SHOWING TIME RELATIONSHIP OF TX_I DATA

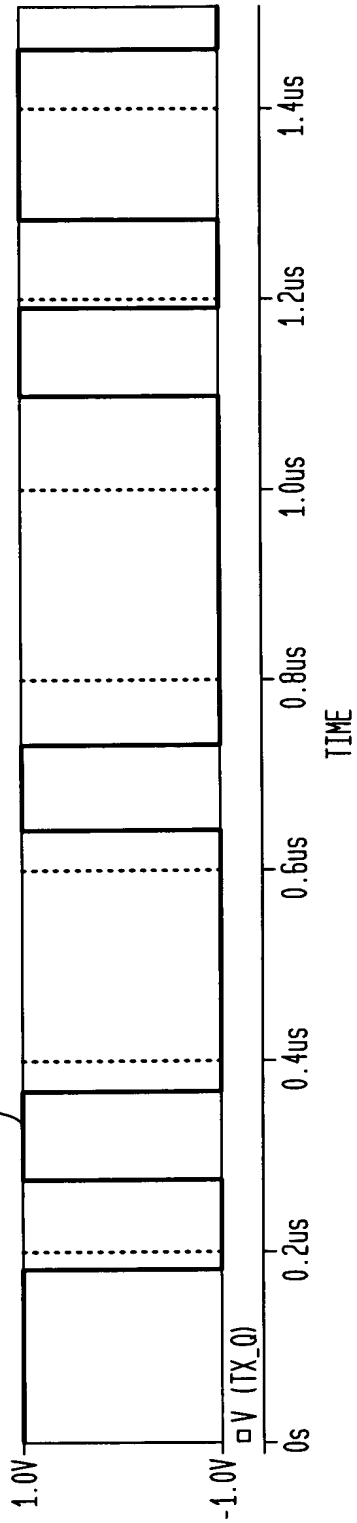



FIG. 203

IQDEMOD SHOWING TIME RELATIONSHIP OF TX_Q DATA

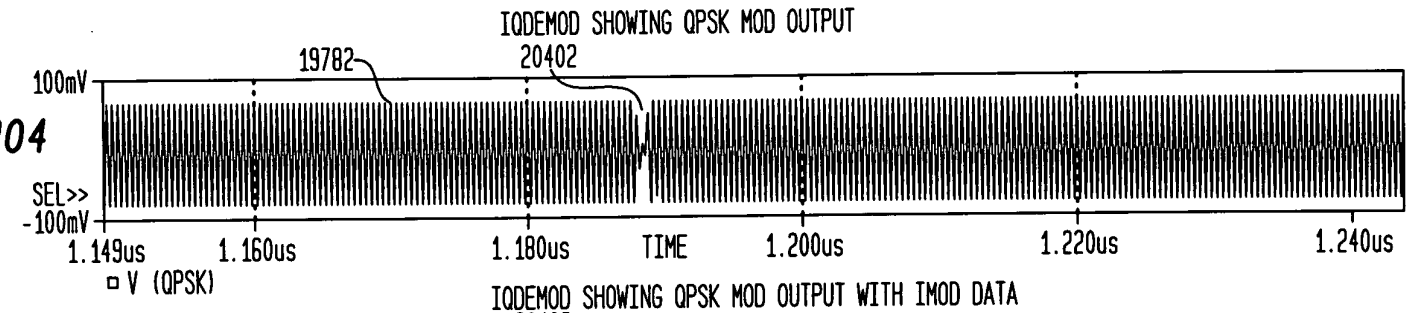



FIG. 204

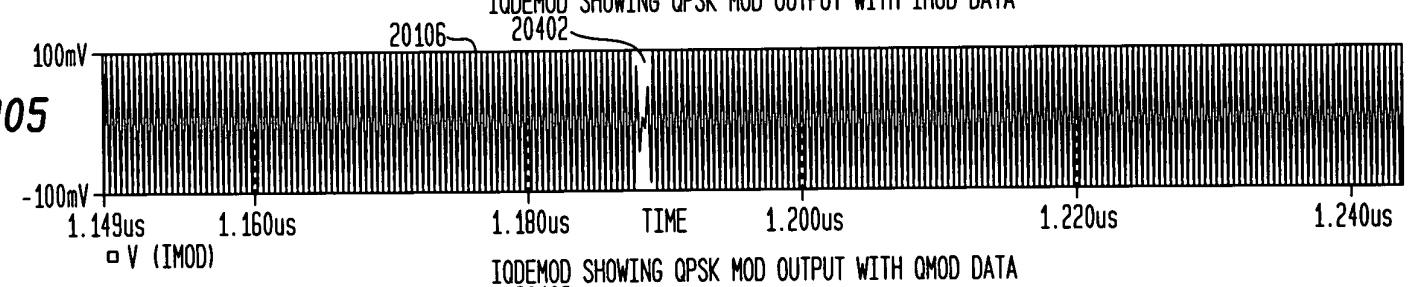



FIG. 205

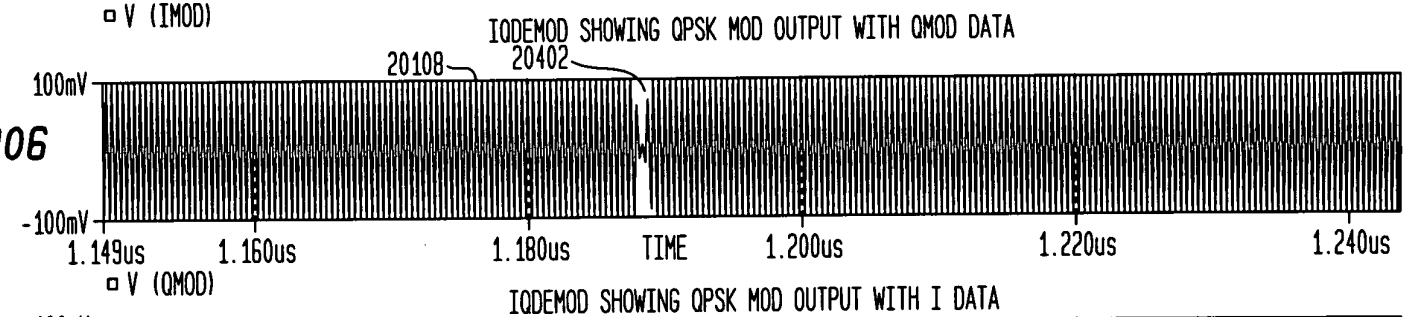



FIG. 206

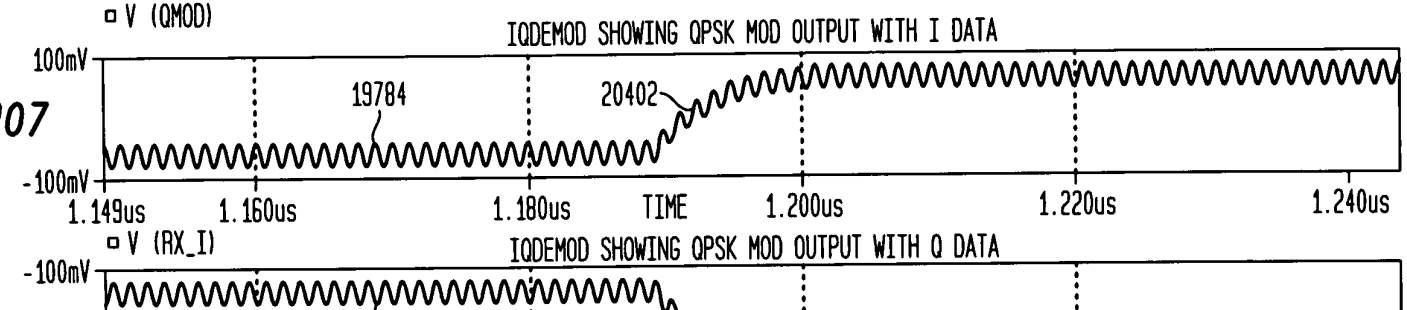



FIG. 207

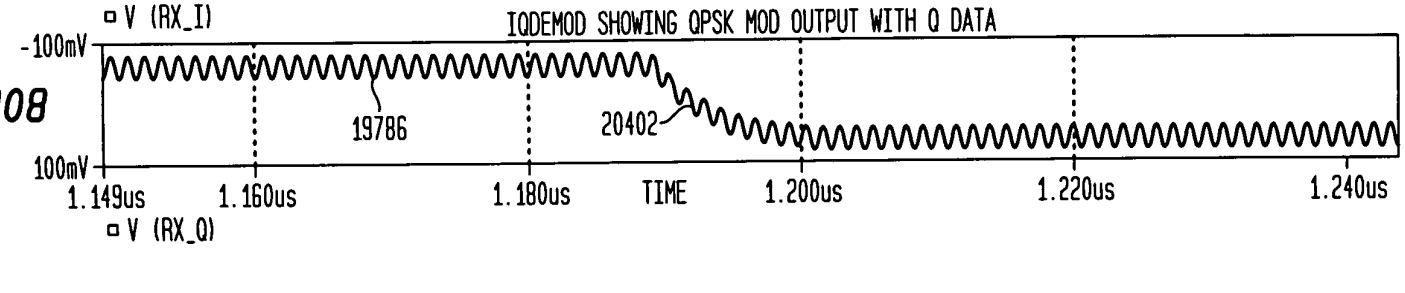



FIG. 208

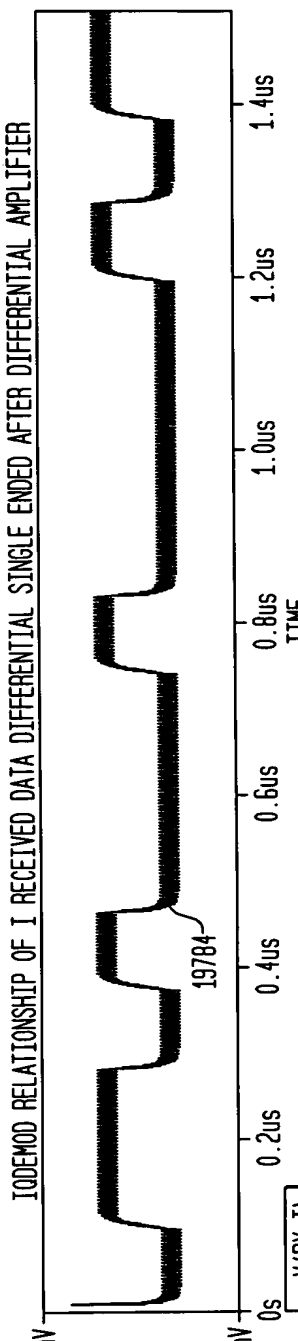



FIG. 209




FIG. 210




FIG. 211




FIG. 212

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Tel. No.: 202-371-2600
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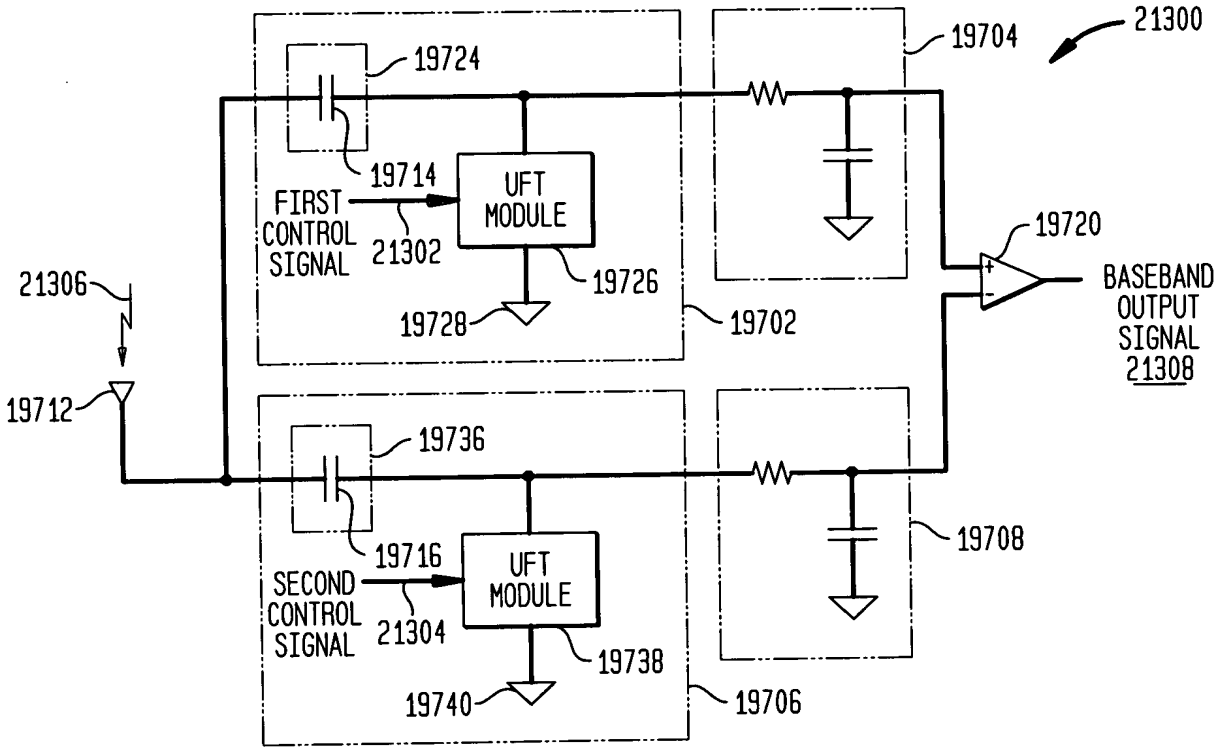
FIG. 213



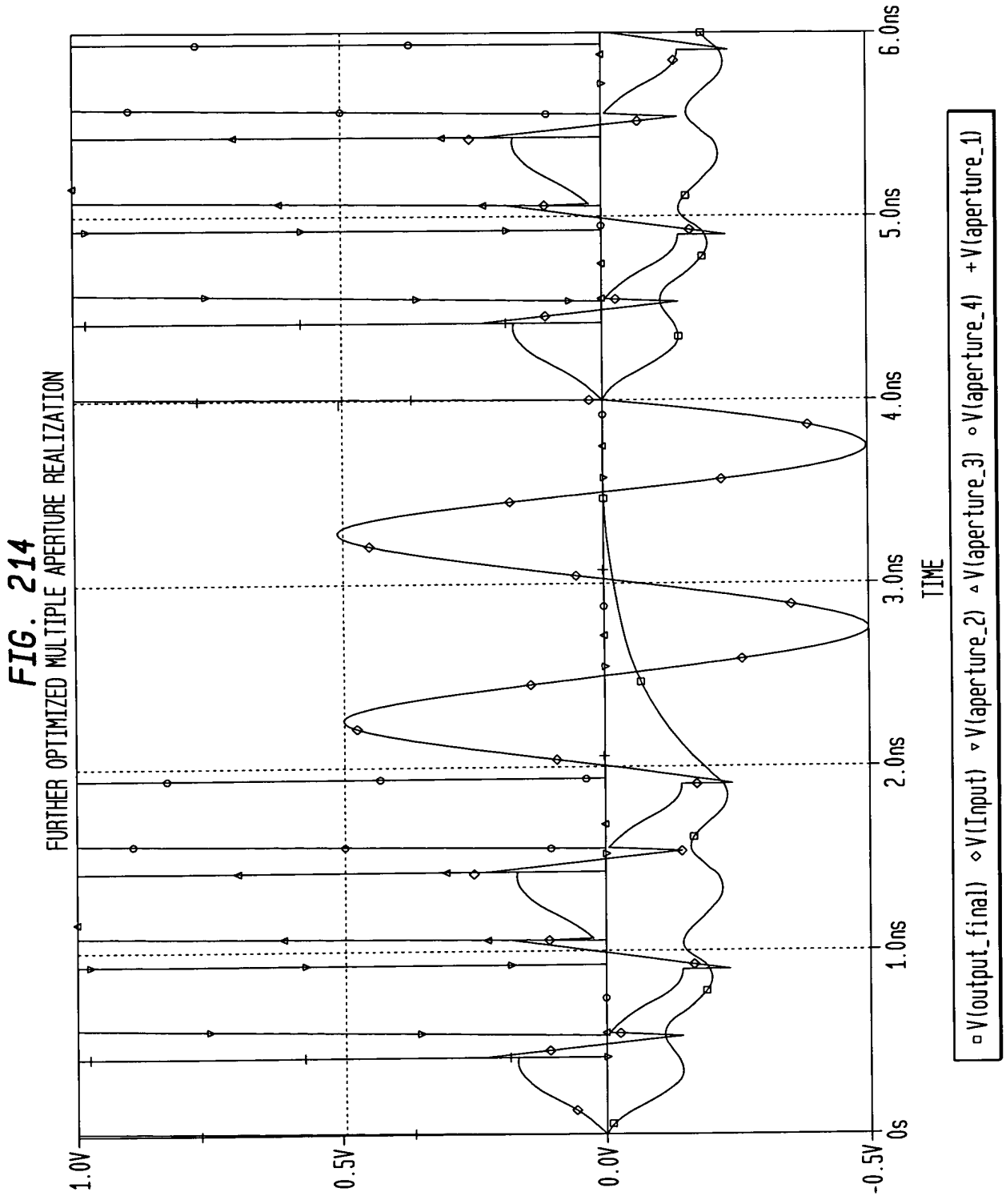

FURTHER OPTIMIZED MULTIPLE APERTURE REALIZATION
1.0V
0.5V
0.0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final)
V(Input)
V(aperture_2)
V(aperture_3)
V(aperture_4)
V(aperture_1)

FIG. 214

FIG. 215

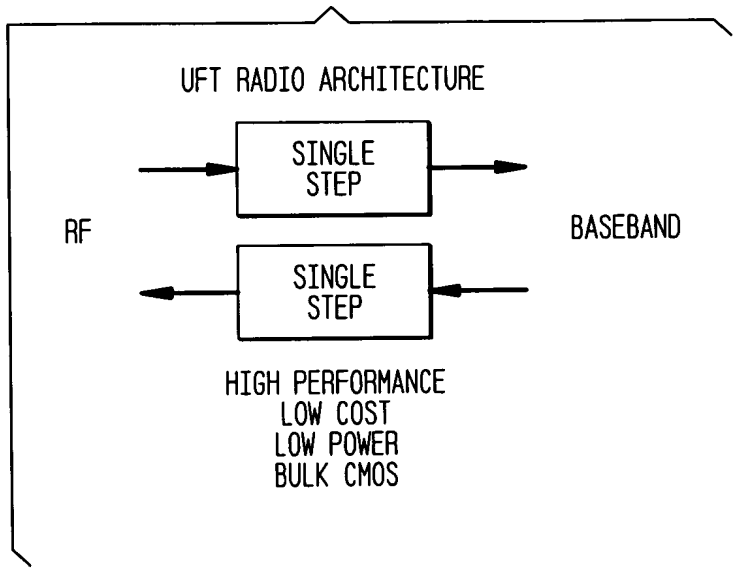
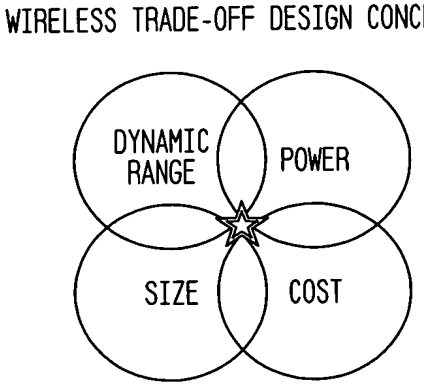



FIG. 216



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# FIG. 217

NOISE FIGURE CALCULATIONS BASED ON RMS
VOLTAGE AND CURRENT NOISE SPECIFICATIONS

ENTER, THE VOLTAGE NOISE DENSITY, $e_n$, AND THE
CURRENT NOISE DENSITY, $i_n$, FOR THE AMPLIFIER CHOSEN:

$e_n := 6 \cdot 10^{-9}$ V/sqrt(Hz)
$i_n := 1 \cdot 10^{-12}$ A/sqrt(Hz)

ENTER THE SOURCE RESISTANCE DRIVING THE AMPLIFIER:

$K := 1.38 \cdot 10^{-23}$ J/K  $T := 290K$

$PARALELL(x,y) := \frac{x \cdot y}{x+y}$  $NF(R_S) := 20 \cdot \log\left(\sqrt{\frac{e_n^2 + 4 \cdot K \cdot T \cdot R_S + i_n^2 \cdot R_S^2}{4 \cdot K \cdot T \cdot R_S}}\right)$

IF WE PLOT NOISE FIGURE VERSUS SOURCE RESISTANCE WE CAN GET
AN IDEA OF WHAT IS THE OPTIMUM SOURCE RESISTANCE.
IT IS NOT NECESSARILY THE LOWEST RESISTANCE!

$R_S := 100, 200 \ldots 100 \cdot 10^3$

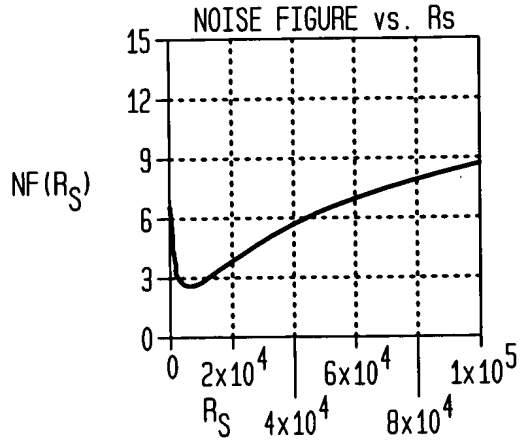

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FIG. 218A

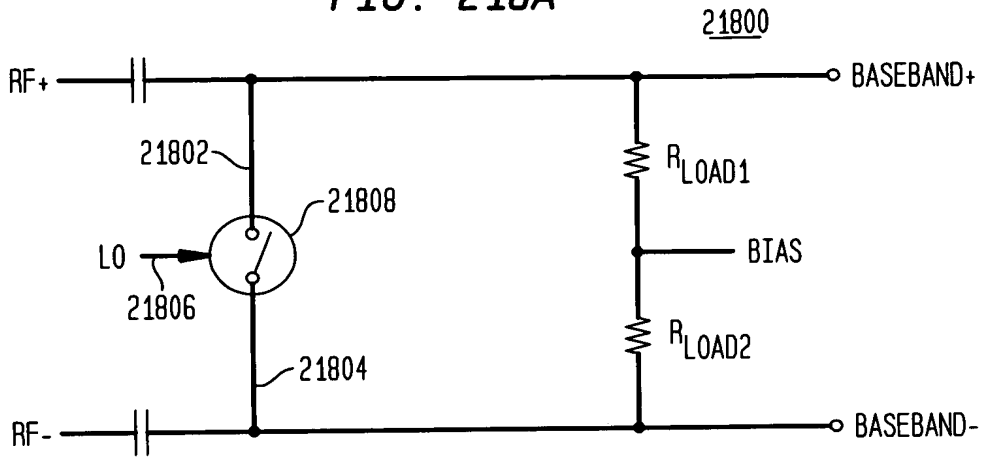



FIG. 218B

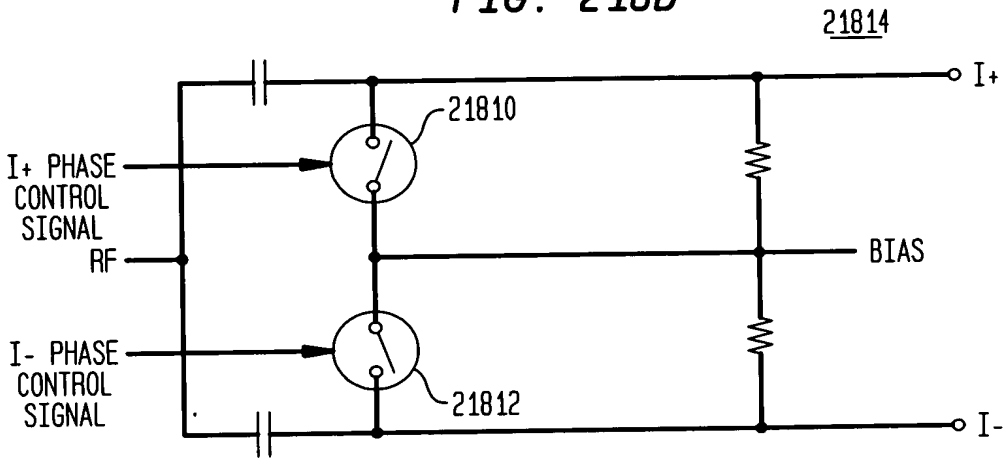



FIG. 218C

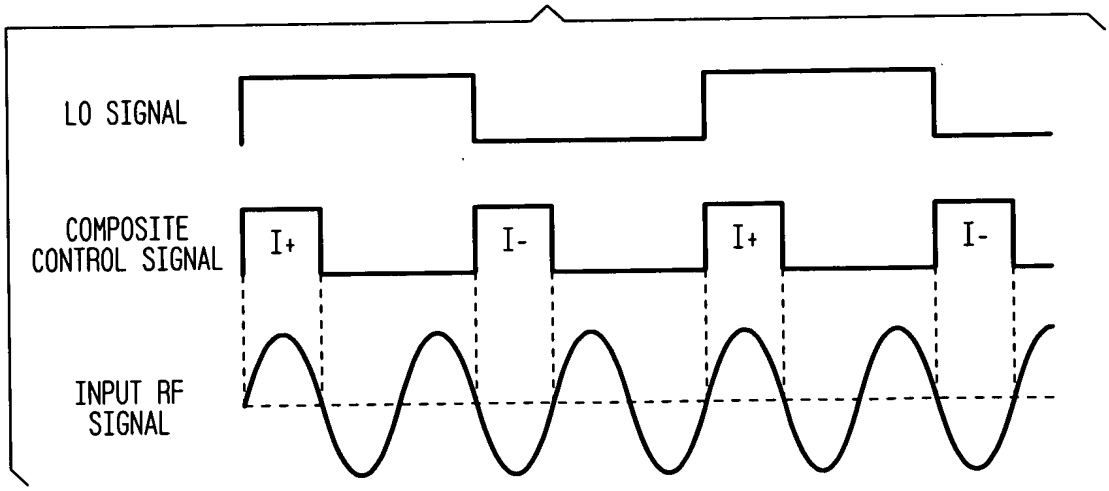


FIG. 218D

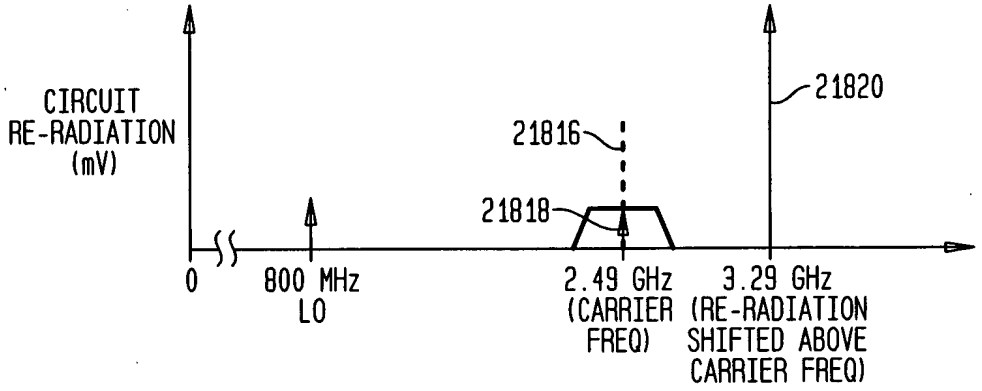



FIG. 218F

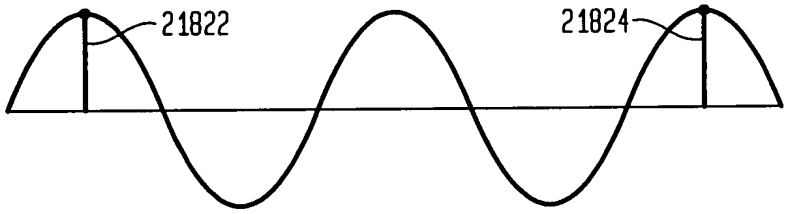



FIG. 218G

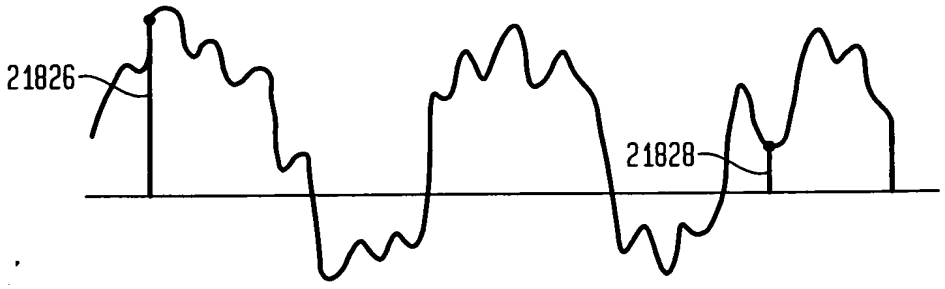


FIG. 218E

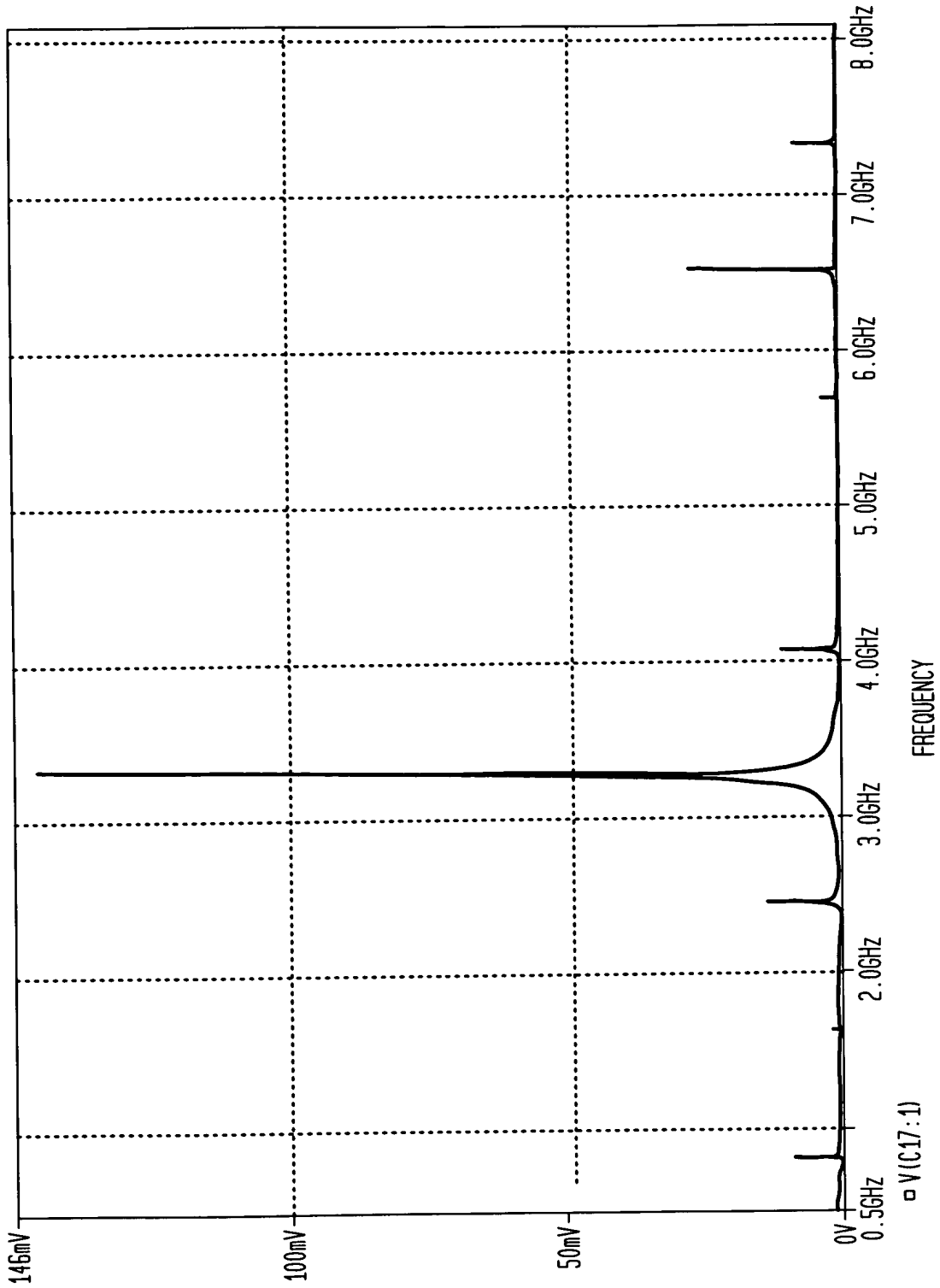

146mV
100mV
50mV
0V
0.5GHz
2.0GHz
3.0GHz
4.0GHz
5.0GHz
6.0GHz
7.0GHz
8.0GHz
FREQUENCY
V(C17:1)

FIG. 219

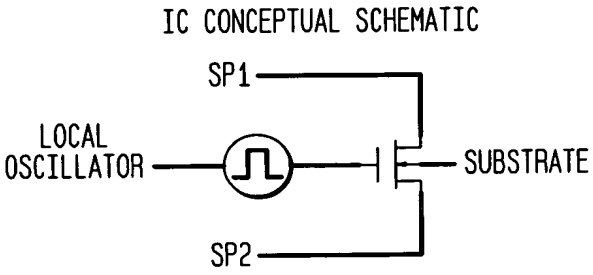
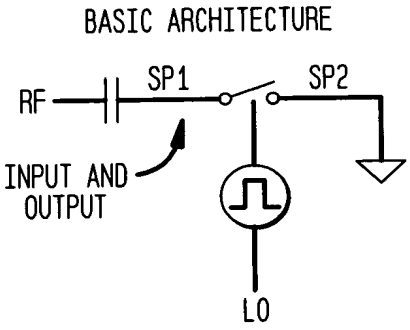



FIG. 220



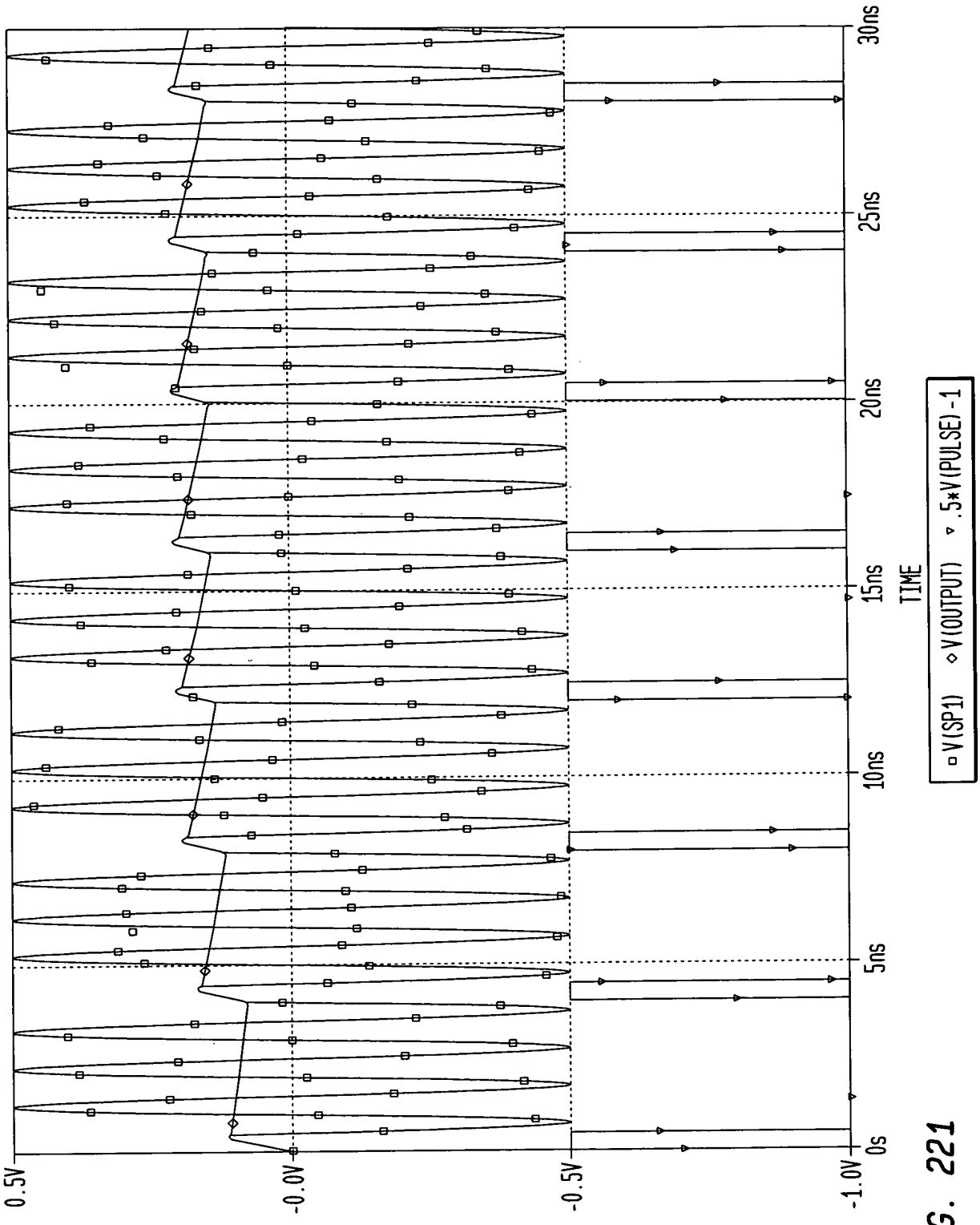

0.5V
-0.0V
-0.5V
-1.0V
0s
5ns
10ns
15ns
20ns
25ns
30ns
TIME
V(SP1)
V(OUTPUT)
.5*V(PULSE)-1

FIG. 221

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Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 222

DC EQUATIONS

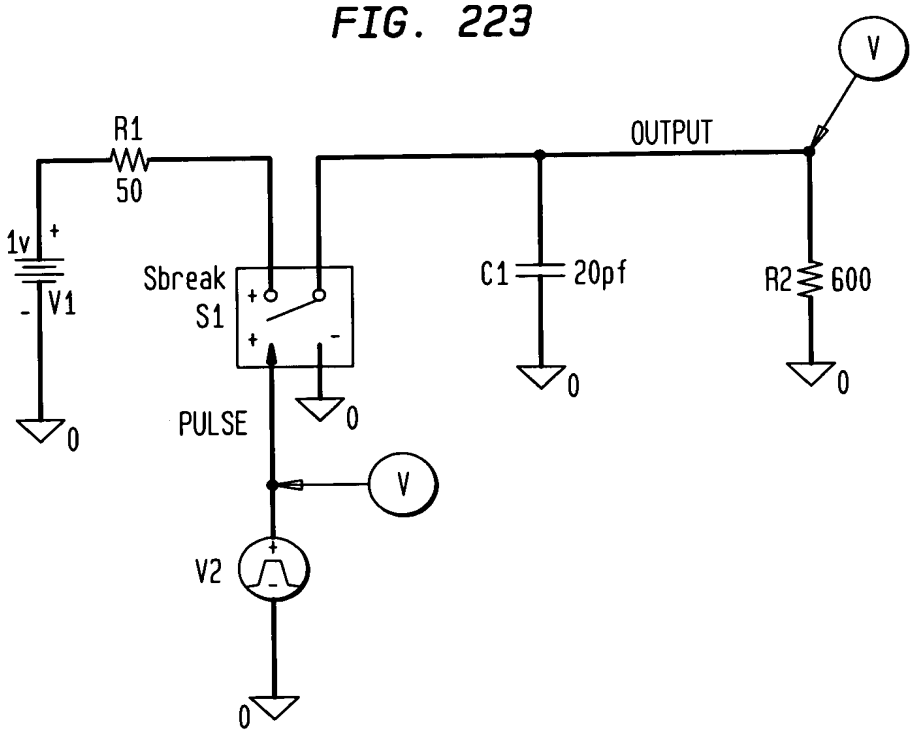
$$Vin = V \cdot \frac{Rout}{Rin + Rout}$$

$$Vc = Vin - (Vin - Vinit) \cdot \exp\left(\frac{-tc}{Rin \cdot C}\right)$$

$$Vd = Vc \cdot \exp\left(\frac{-td}{Rout \cdot C}\right)$$

DEFINITIONS:
- Rin - INPUT RESISTANCE
- Rout - OUTPUT RESISTANCE
- C - CAPACITOR
- tc - CHARGE TIME OR APERATURE
- td - DISCHARGE TIME OR LO PERIOD-tc
- V - INPUT VOLTAGE
- Vinit - INITIAL CAPACITOR VOLTAGE
- Vc - FINAL CHARGE CAPACITOR VOLTAGE
- Vd - FINAL DISCHARGE CAPACITOR VOLTAGE

FIG. 223



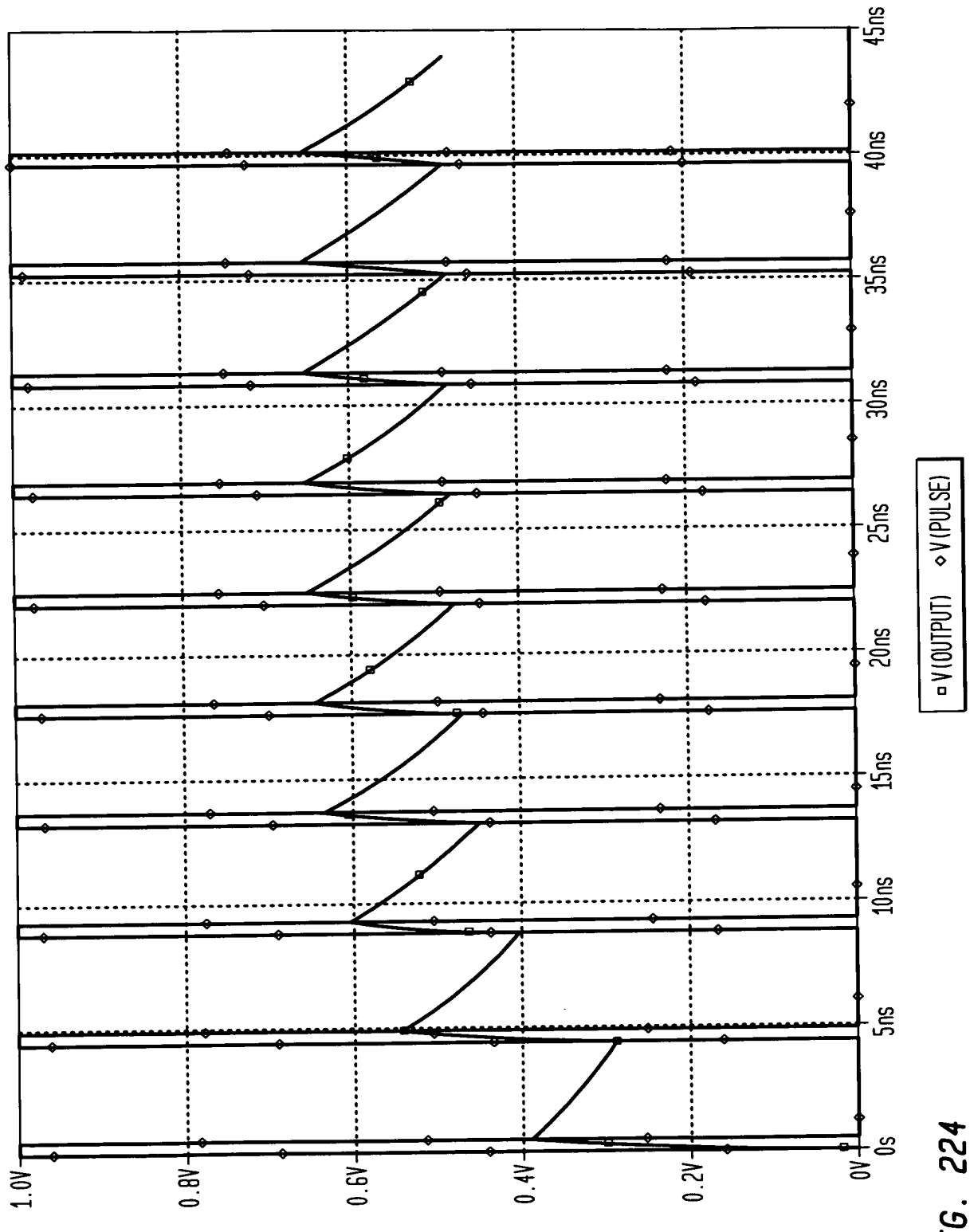
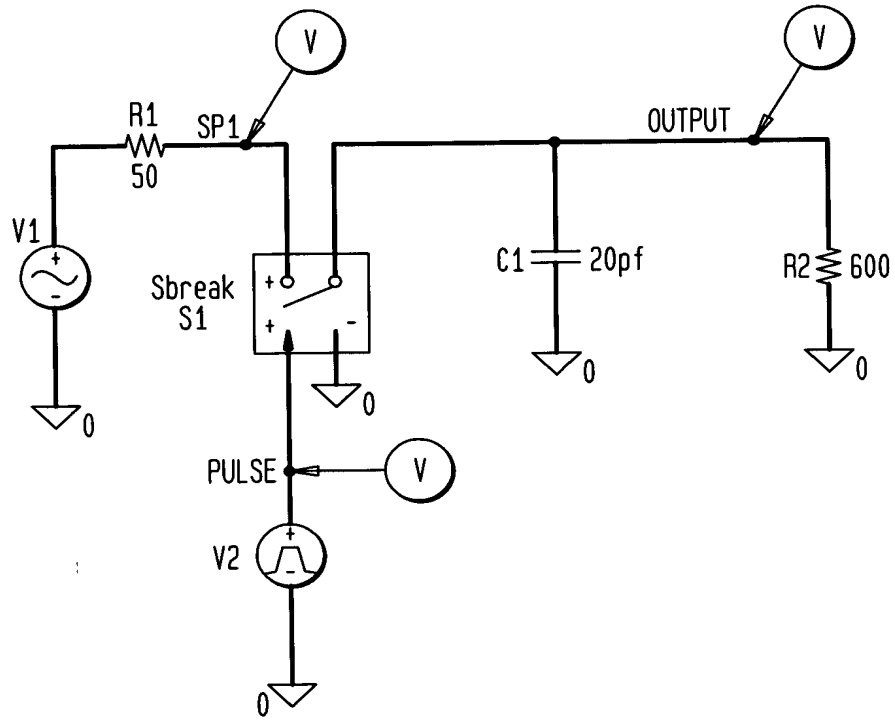

45ns
40ns
35ns
30ns
25ns
20ns
15ns
10ns
5ns
0s
1.0V
0.8V
0.6V
0.4V
0.2V
0V
V(OUTPUT)
V(PULSE)

FIG. 224

FIG. 225



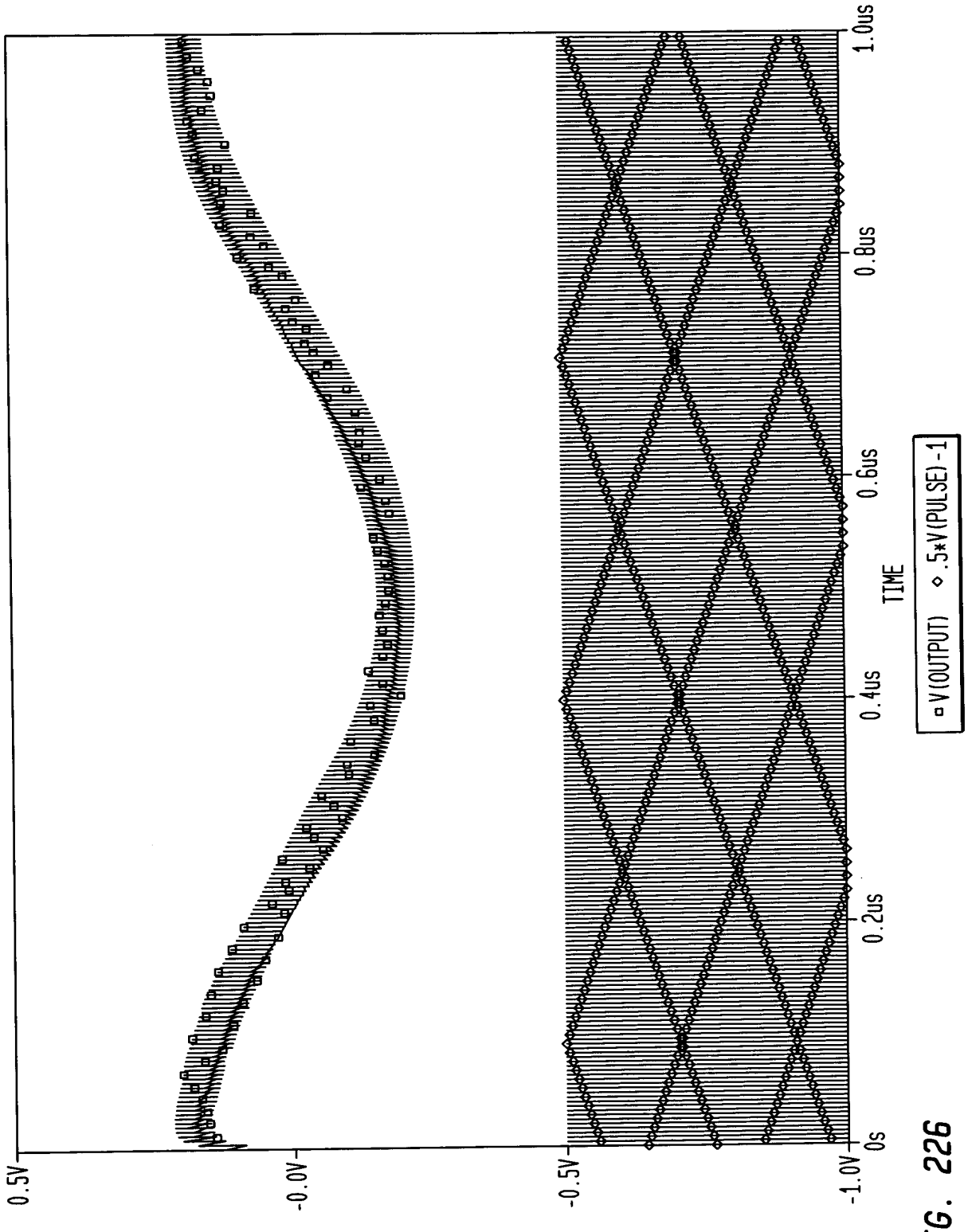

0.5V
-0.0V
-0.5V
-1.0V
0s
0.2us
0.4us
0.6us
0.8us
1.0us
TIME
V(OUTPUT)
.5*V(PULSE)-1

FIG. 226

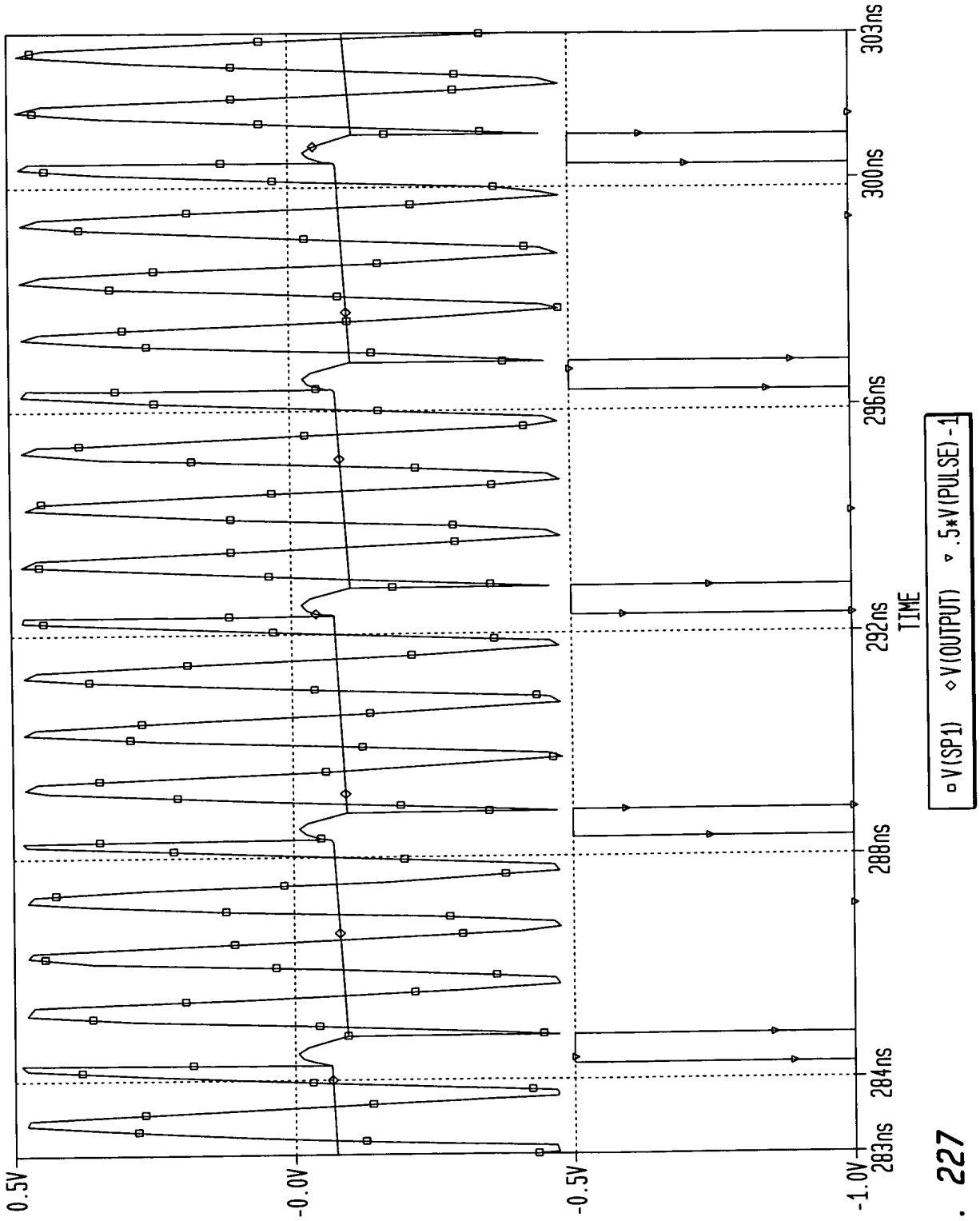
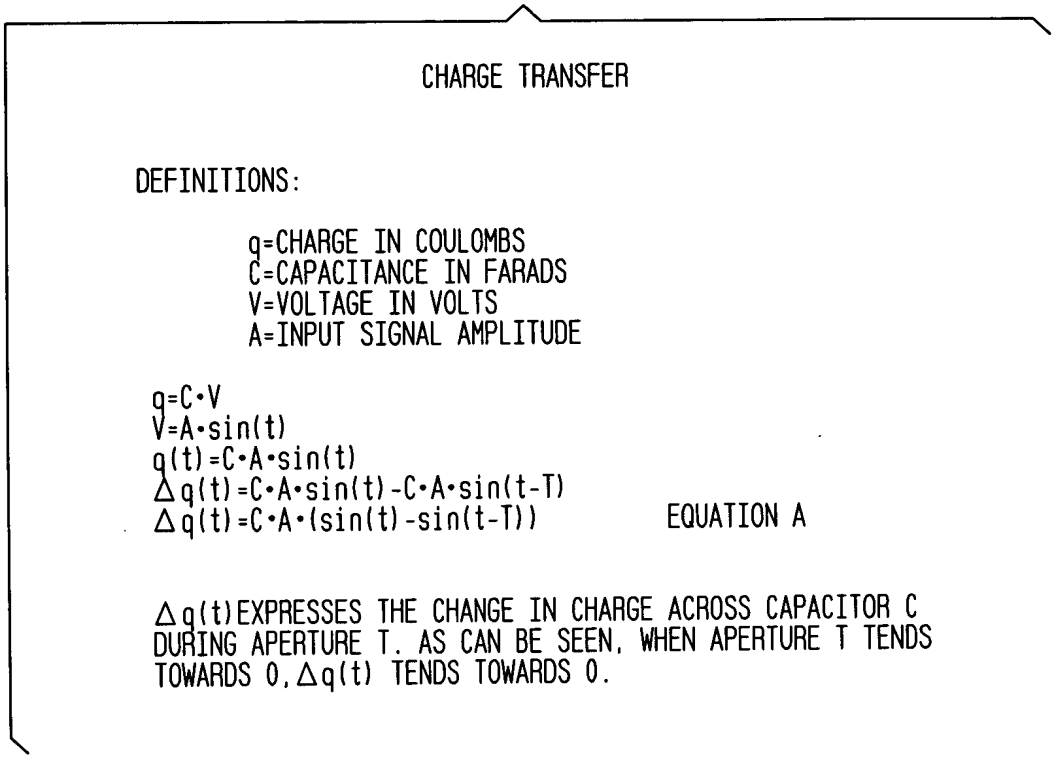

303ns
300ns
296ns
292ns
288ns
284ns
283ns
TIME
0.5V
-0.0V
-0.5V
-1.0V
V(SP1)
V(OUTPUT)
.5*V(PULSE)-1

FIG. 227

FIG. 228


CHARGE TRANSFER
DEFINITIONS:
q=CHARGE IN COULOMBS
C=CAPACITANCE IN FARADS
V=VOLTAGE IN VOLTS
A=INPUT SIGNAL AMPLITUDE
q=C•V
V=A•sin(t)
q(t)=C•A•sin(t)
Δq(t)=C•A•sin(t)-C•A•sin(t-T)
Δq(t)=C•A•(sin(t)-sin(t-T))
EQUATION A
Δq(t) EXPRESSES THE CHANGE IN CHARGE ACROSS CAPACITOR C DURING APERTURE T. AS CAN BE SEEN, WHEN APERTURE T TENDS TOWARDS 0, Δq(t) TENDS TOWARDS 0.

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# FIG. 229

USING THE SUM TO PRODUCT TRIGONOMETRIC IDENTITY,

$$\sin(\alpha)-\sin(\beta)=2\cdot\sin\left(\frac{\alpha-\beta}{2}\right)\cdot\cos\left(\frac{\alpha+\beta}{2}\right) \qquad \text{IDENTITY 1}$$

EQUATION 1 CAN BE RE-WRITTEN AS:

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left[\frac{t-(t-T)}{2}\right]\cdot\cos\left[\frac{t+(t-T)}{2}\right]$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left(\frac{1}{2}\cdot T\right)\cdot\cos\left(t-\frac{1}{2}\cdot T\right) \qquad \text{EQUATION B}$$

THE sin TERM IN EQUATION B IS A FUNCTION OF APERTURE T ONLY. IT IS EASILY SEEN THAT $\Delta q(t)$ WILL OBTAIN A MAXIMUM VALUE WHEN T IS EQUAL TO AN ODD MULTIPLE OF $\pi$ i.e., $\pi$ 3 $\pi$ 5 $\pi$.. THEREFORE, CAPACITOR C EXPERIENCES THE GREATEST CHANGE IN CHARGE WHEN THE APERTURE HAS A VALUE OF $\pi$ OR A TIME INTERVAL REPRESENTATIVE OF 180 DEGREES OF THE INPUT SINUSOID. CONVERSELY, WHEN T IS EQUAL TO $2\pi$, $4\pi$, $6\pi$....MINIMAL CHARGE IS TRANSFERRED.

FIG. 230

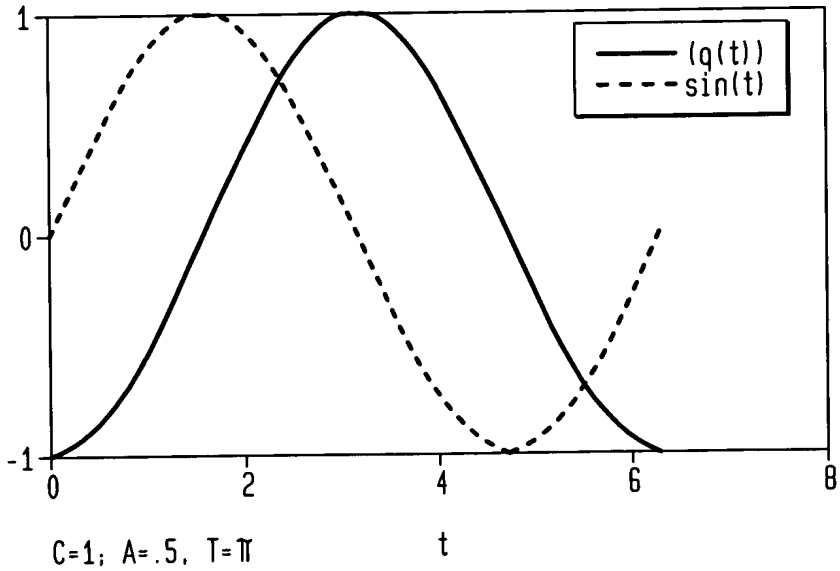
SOLVING FOR q(t) BY INTEGRATING EQUATION A ALLOWS THE CHARGE ON C WITH RESPECT TO TIME TO BE GRAPHED ON THE SAME AXIS AS THE INPUT SINUSOID sin(t).

$$q(t)=\int C\cdot A\cdot(\sin(t)-\sin(t-T))\,dt$$

$$q(t)=-\cos(t)\cdot C\cdot A+\cos(t-T)\cdot C\cdot A$$

$$q(t)=C\cdot A\cdot(\cos(t-T)-\cos(t)) \qquad \text{EQUATION C}$$

FIG. 231




GRAPH 1

C=1; A=.5, T=π

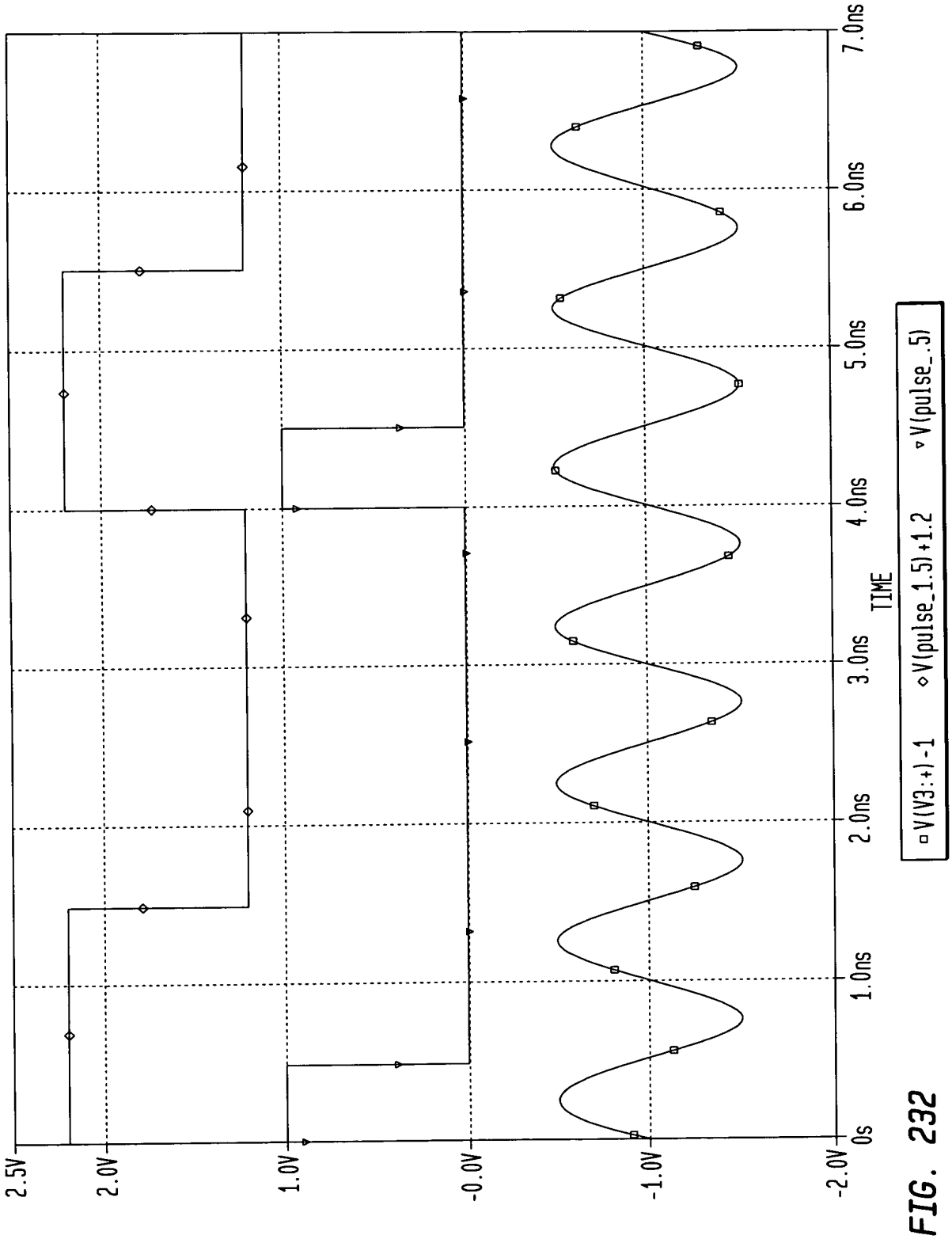

2.5V
2.0V
1.0V
-0.0V
-1.0V
-2.0V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
7.0ns
TIME
V(V3:+)-1
V(pulse_1.5)+1.2
V(pulse_.5)

FIG. 232

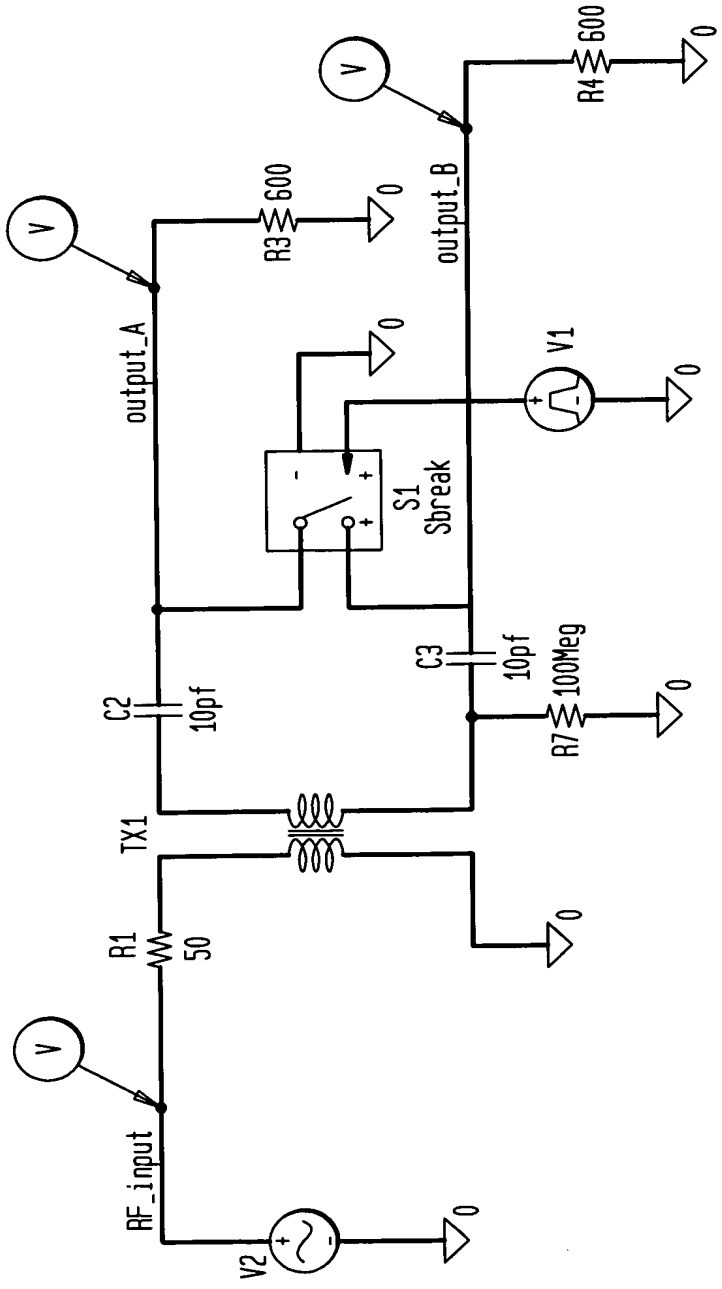

R4
600
0
output_B
R3
600
0
output_A
0
V1
0
S1
Sbreak
C3
10pf
R7
100Meg
0
C2
10pf
TX1
0
R1
50
RF_input
V2
0

FIG. 233

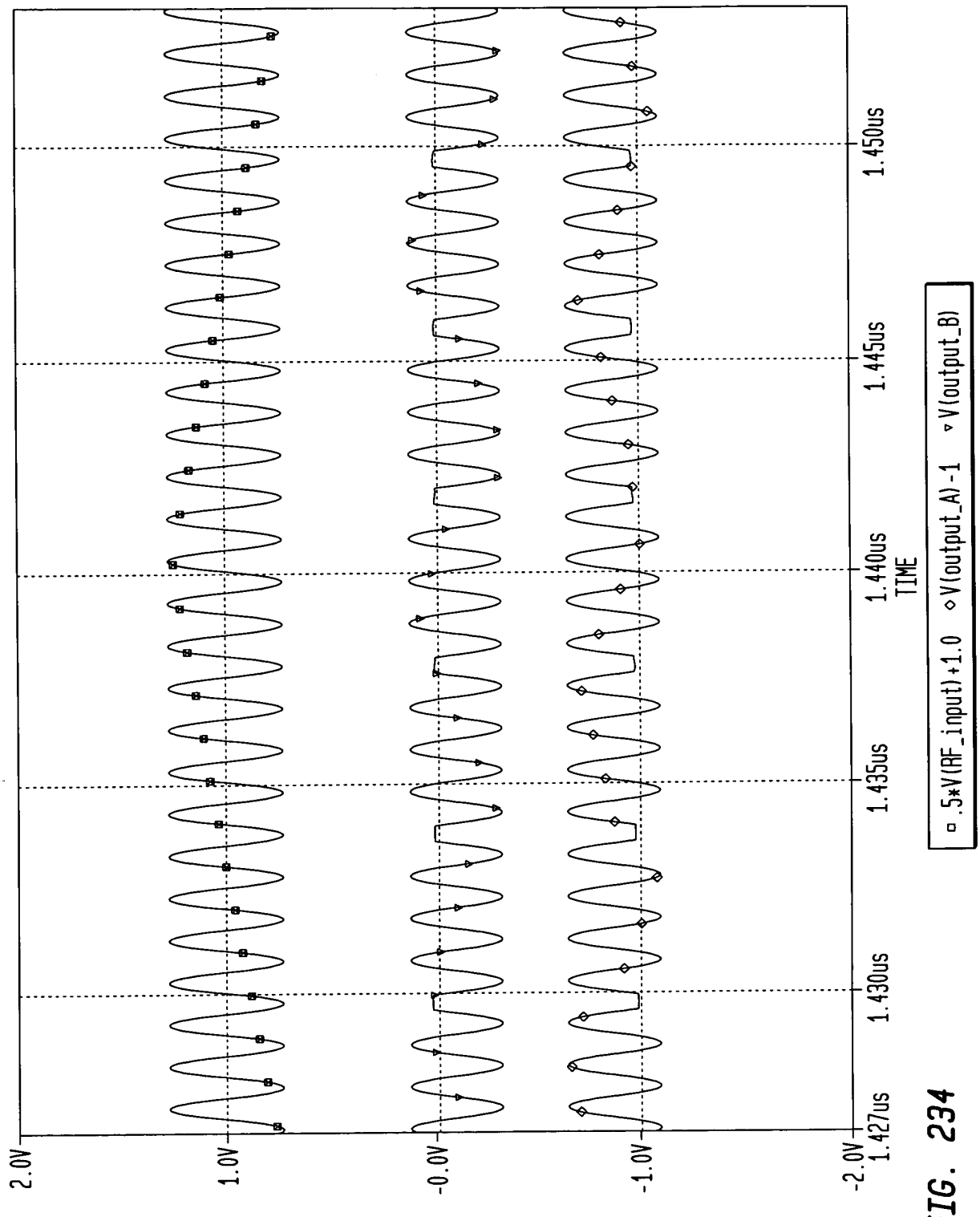

2.0V
1.0V
-0.0V
-1.0V
-2.0V
1.427us
1.430us
1.435us
1.440us
1.445us
1.450us
TIME
□ .5*V(RF_input)+1.0
◇ V(output_A)-1
▽ V(output_B)

FIG. 234

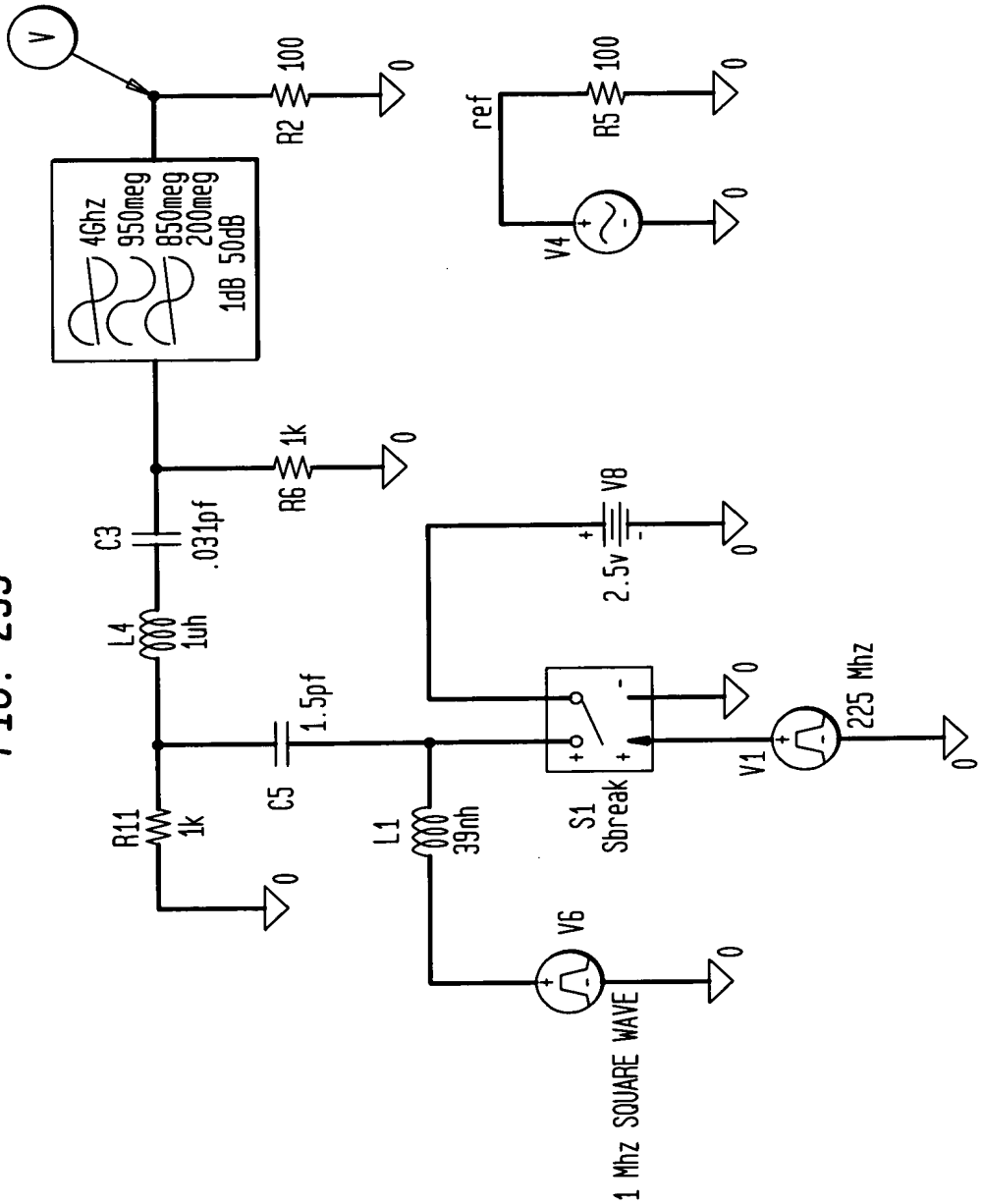

V
R2
100
0
4Ghz
950meg
850meg
200meg
1dB 50dB
ref
R5
100
V4
R6
1k
C3
.031pf
L4
1uh
V8
2.5v
1.5pf
C5
R11
1k
L1
39nh
S1
Sbreak
V1
225 Mhz
V6
1 Mhz SQUARE WAVE

FIG. 235

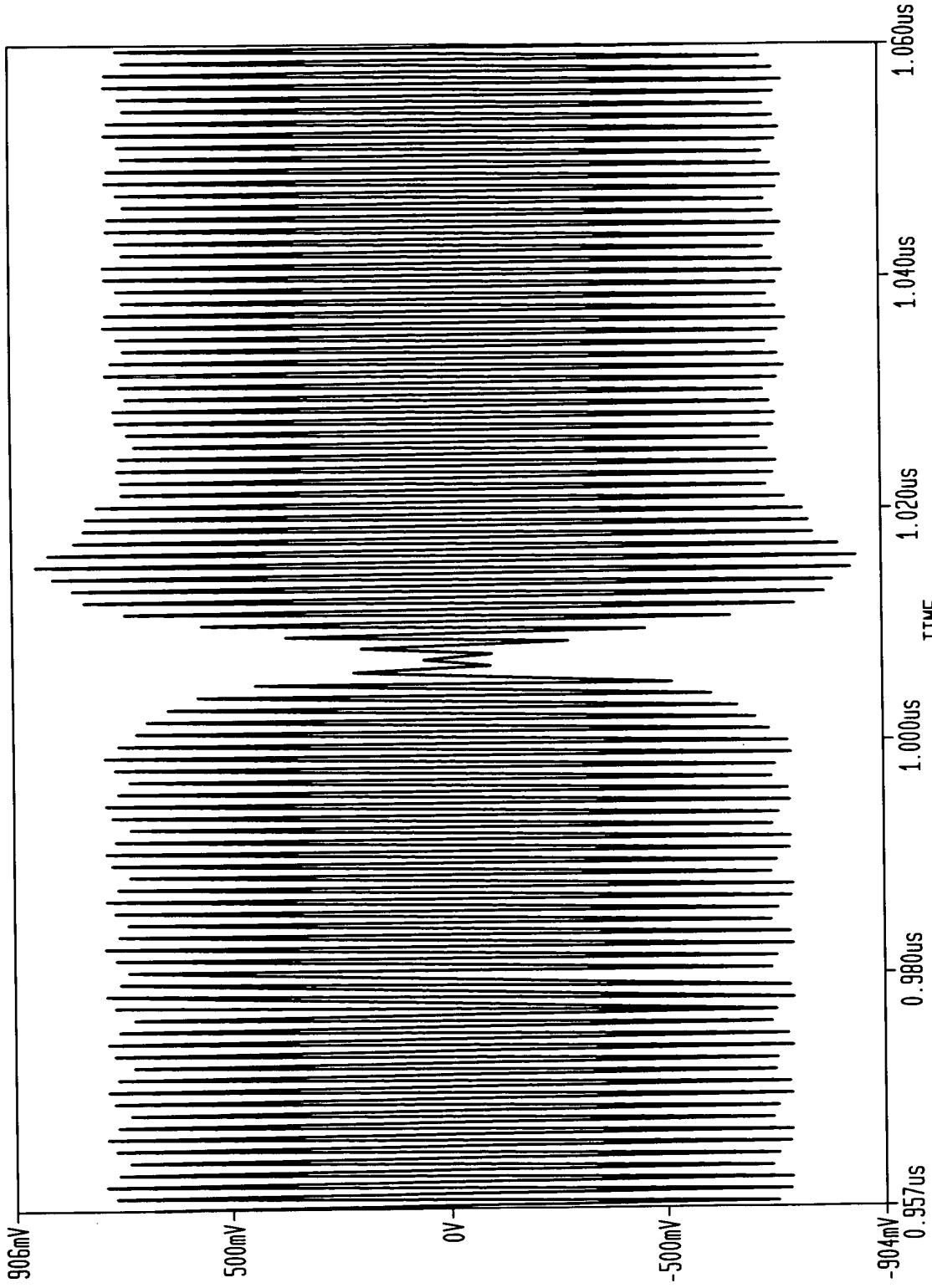

906mV
500mV
0V
-500mV
-904mV
0.957us
0.980us
1.000us
1.020us
1.040us
1.060us
TIME
V(R2:2)

FIG. 236

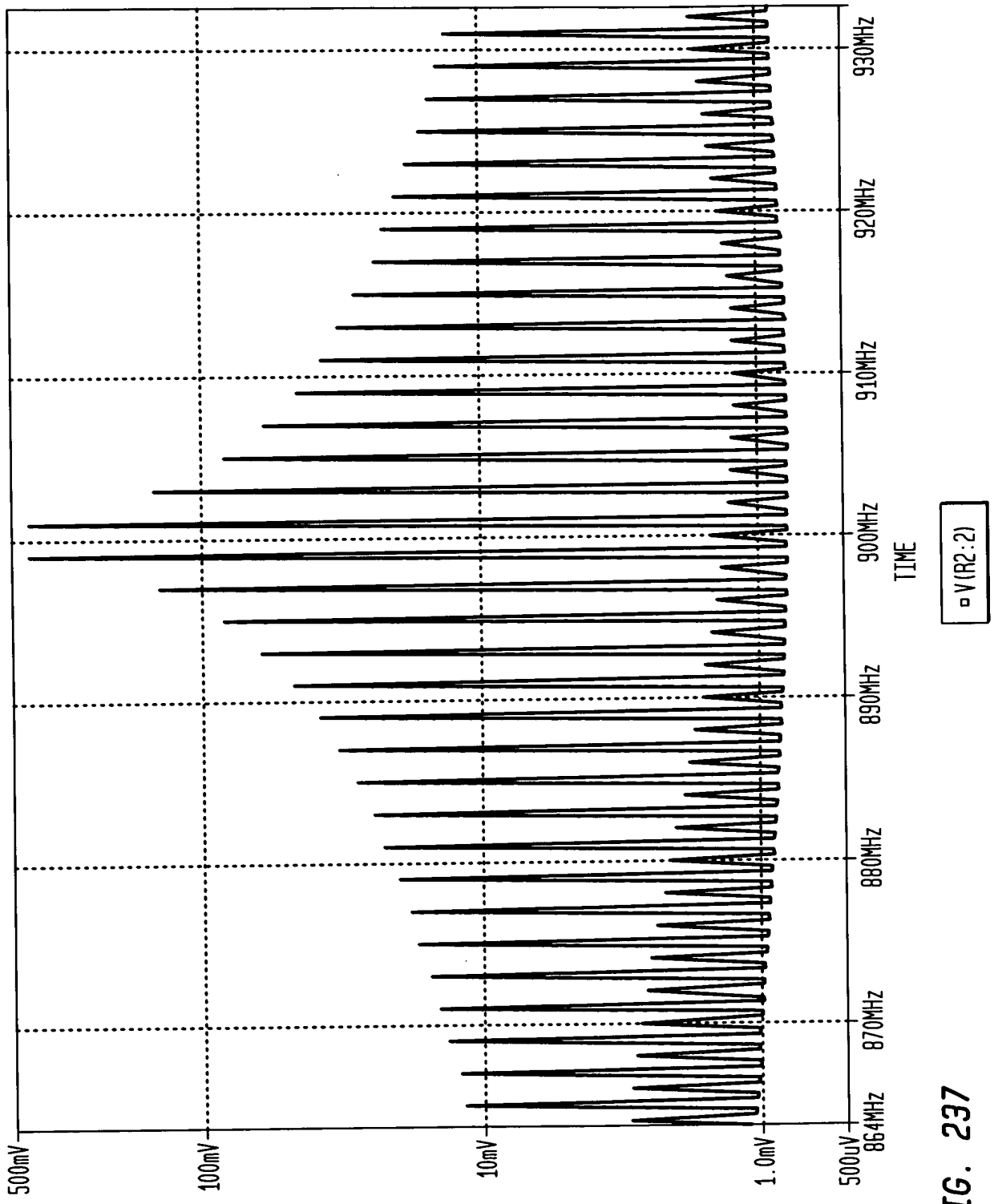

500mV
100mV
10mV
1.0mV
500uV
930MHz
920MHz
910MHz
900MHz
890MHz
880MHz
870MHz
864MHz
TIME
V(R2:2)

FIG. 237

FIG. 238

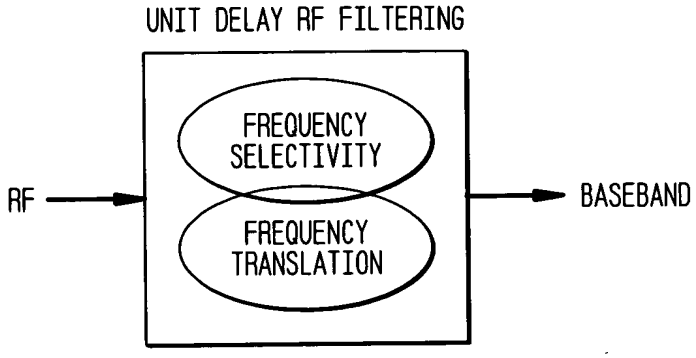



FIG. 239

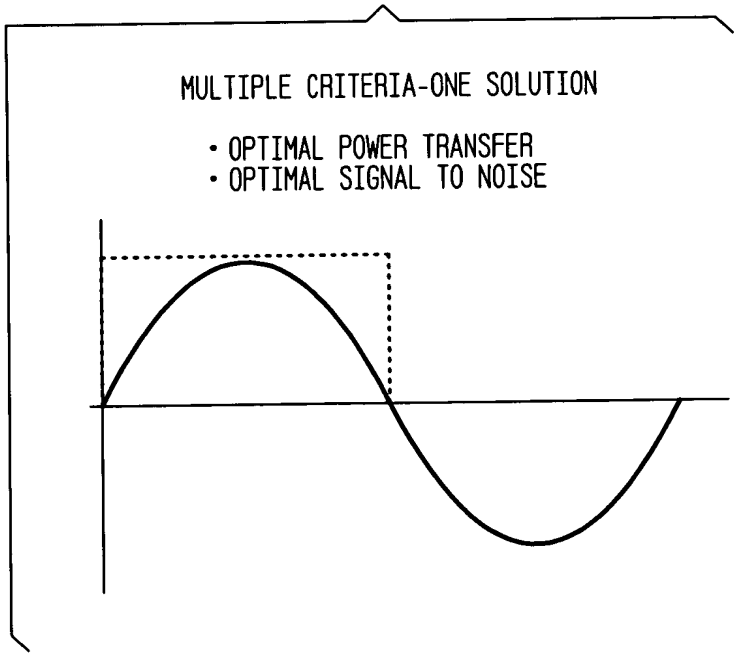


FIG. 240

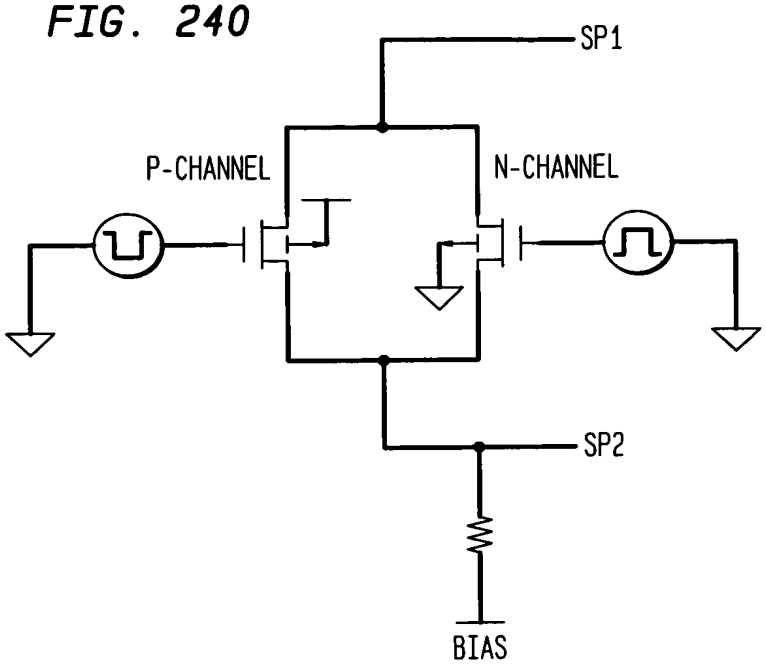



FIG. 241

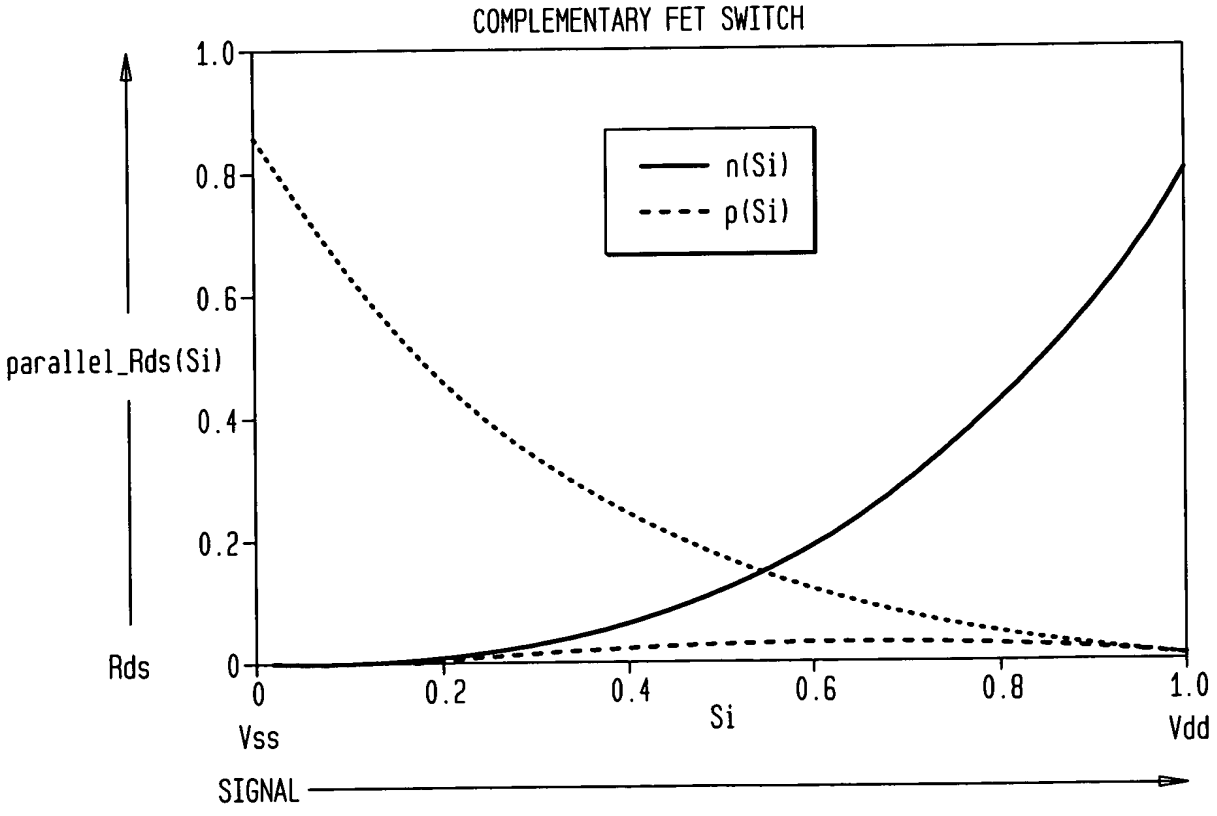
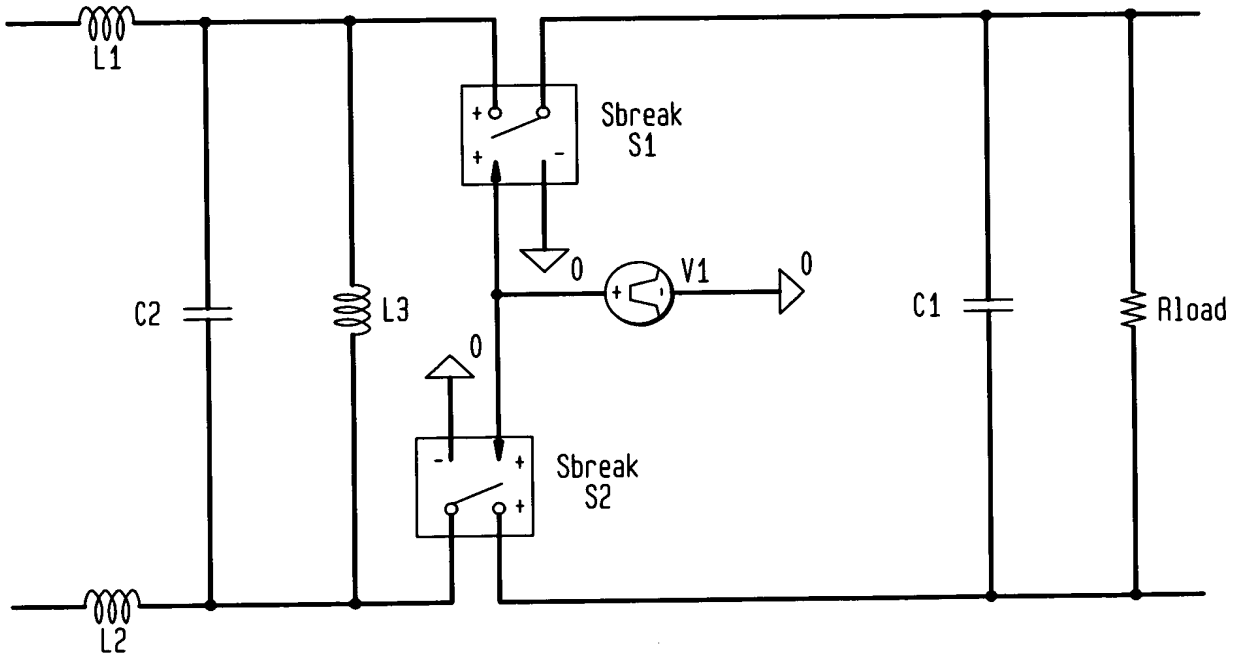


FIG. 242

DIFFERENTIAL CONFIGURATION



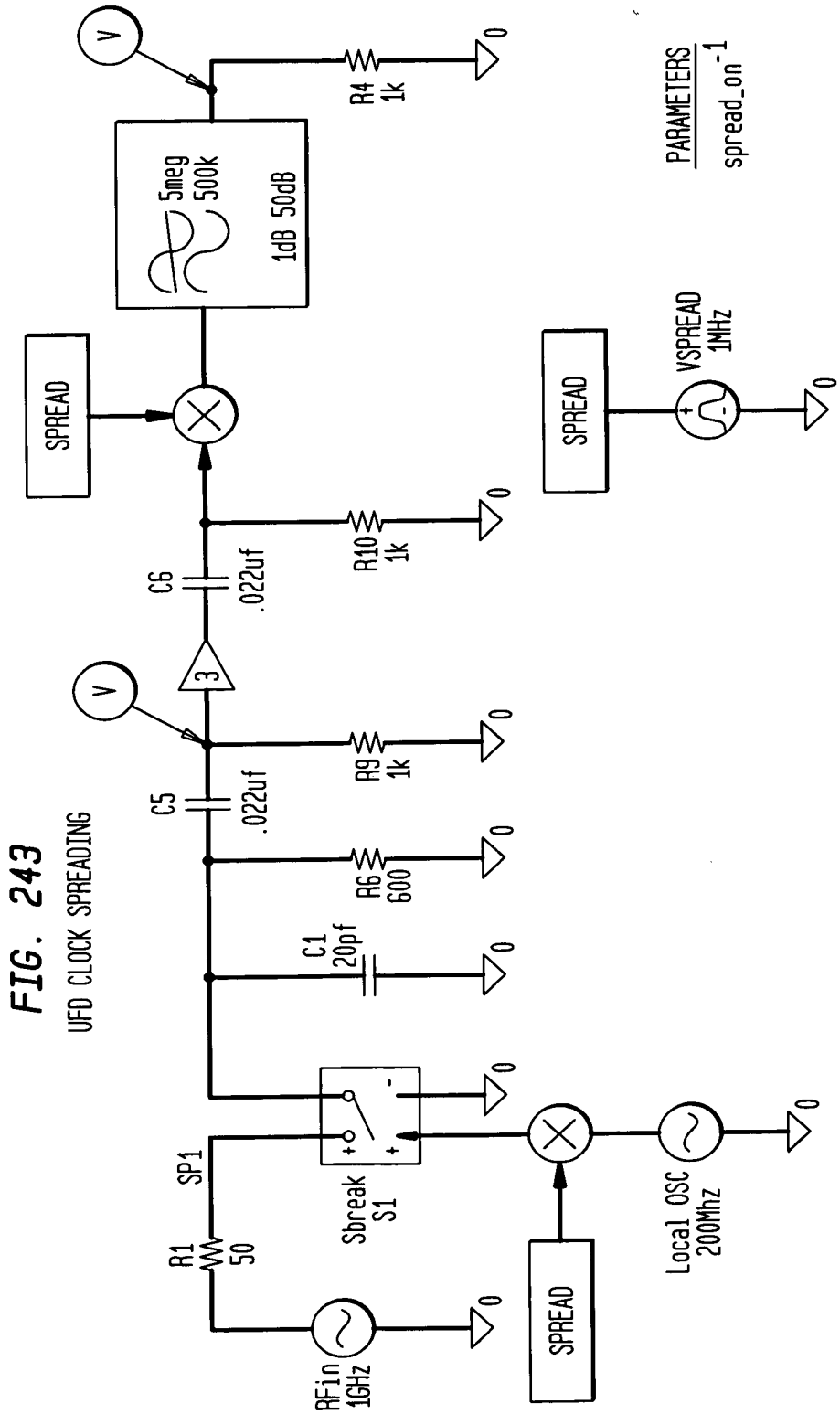



FIG. 243
UFD CLOCK SPREADING

FIG. 244

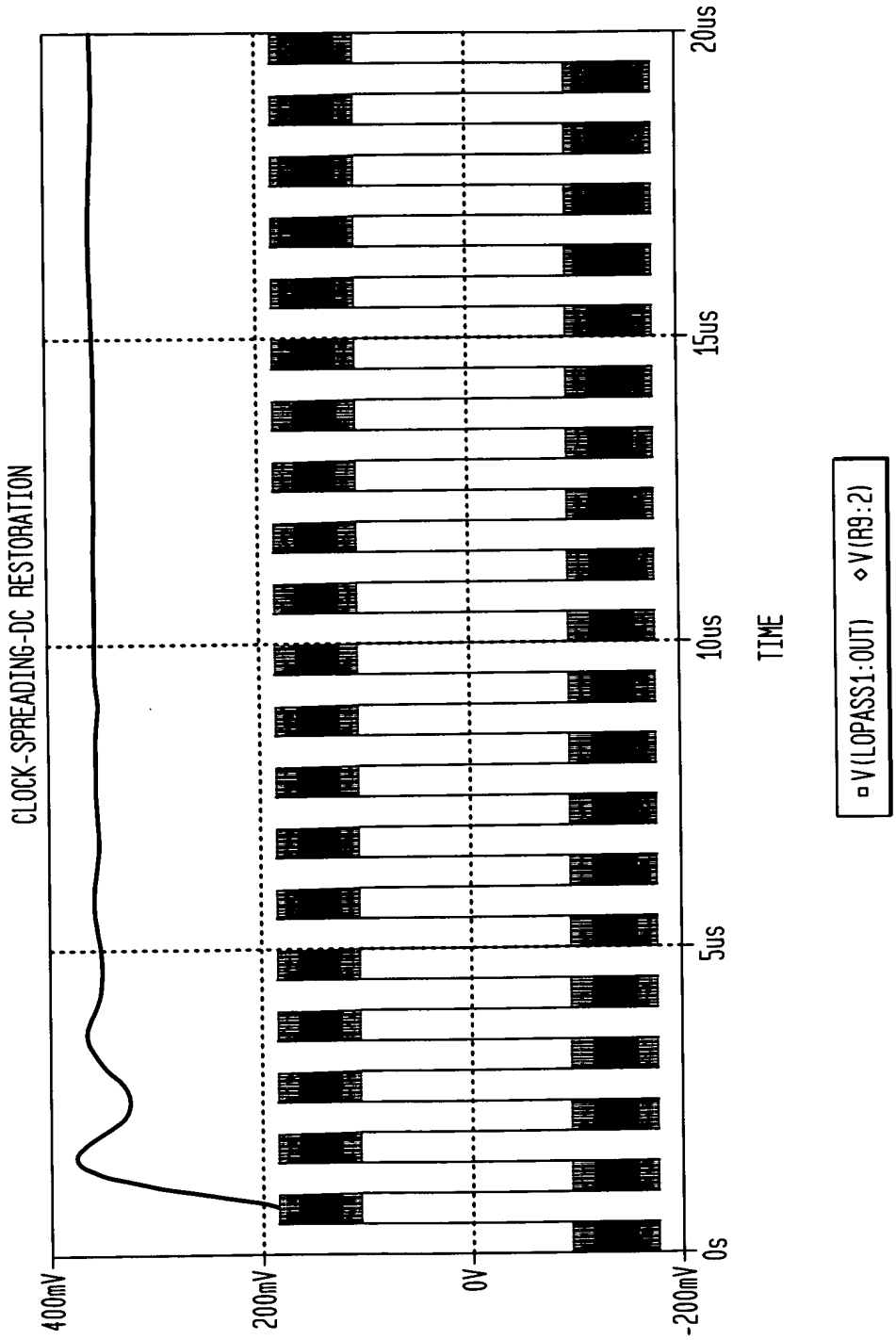

CLOCK-SPREADING-DC RESTORATION
400mV
200mV
0V
-200mV
0s
5us
10us
15us
20us
TIME
V(LOPASS1:OUT)
V(R9:2)

FIG. 245

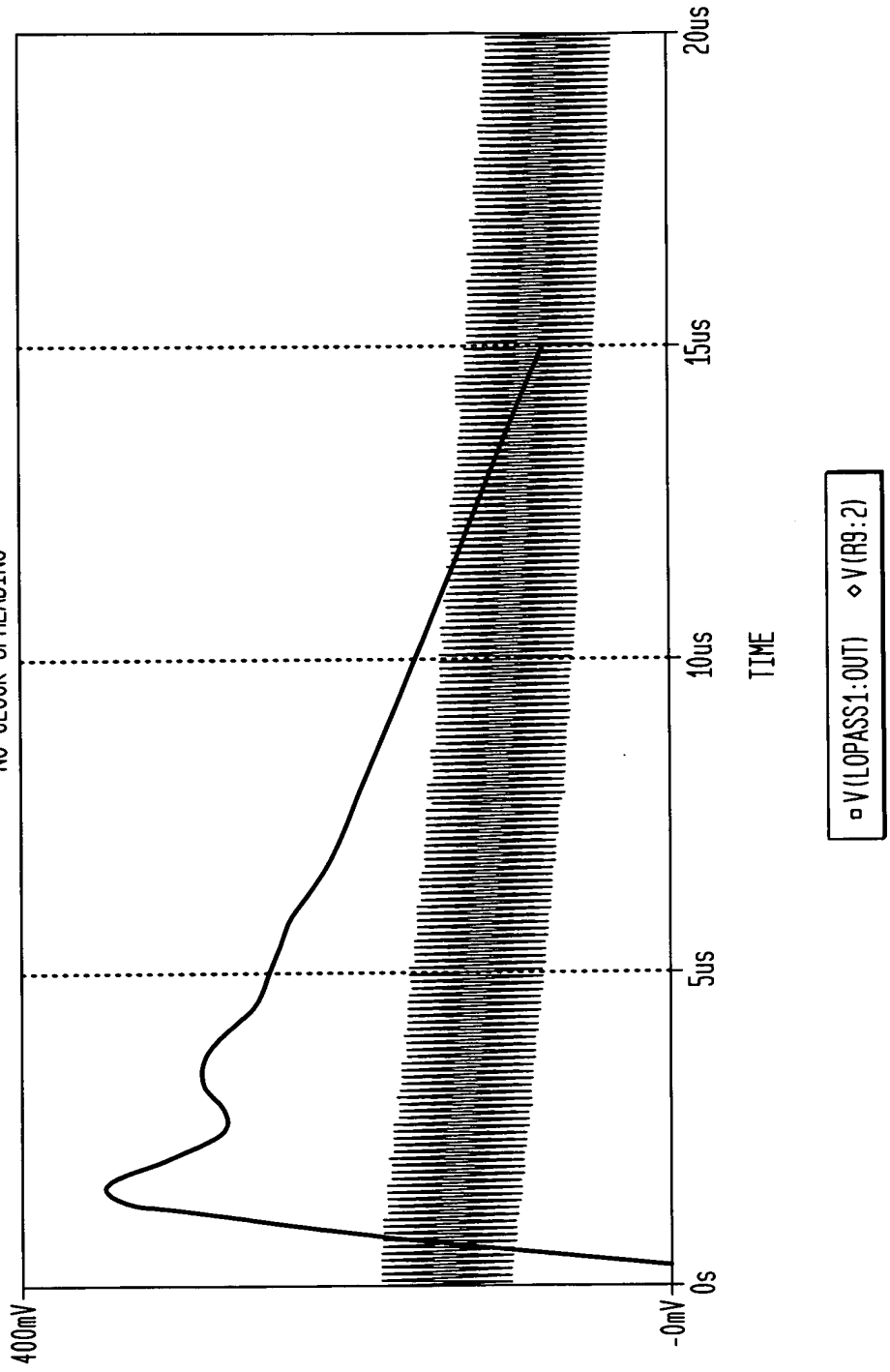

NO CLOCK SPREADING
400mV
-0mV
0s
5us
10us
15us
20us
TIME
V(LOPASS1:OUT)
V(R9:2)

FIG. 246

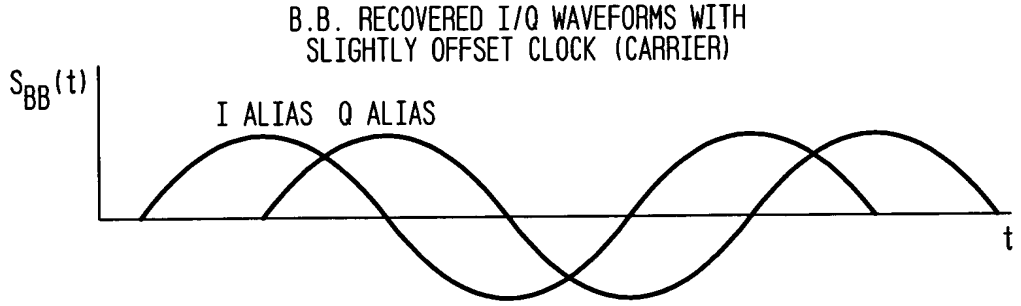



FIG. 247

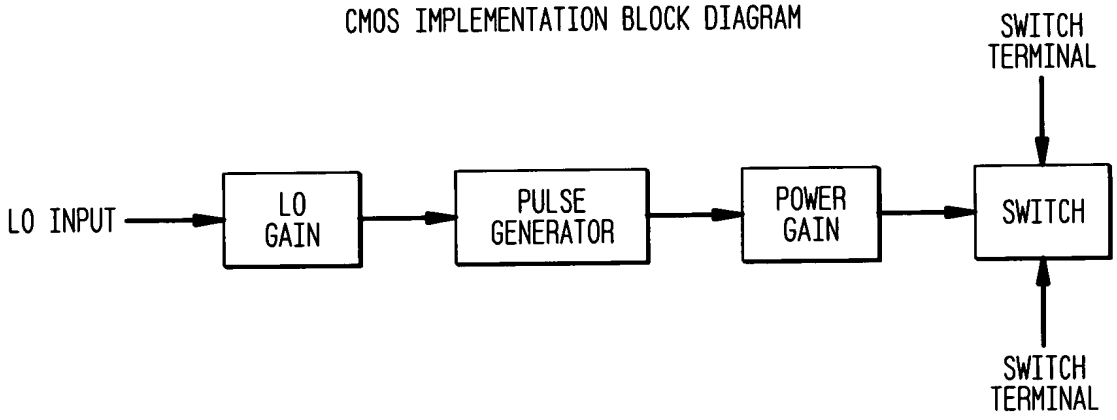



FIG. 248

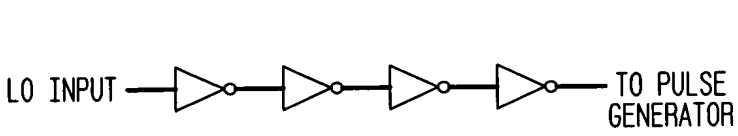


*FIG. 249*

LO GAIN BLOCK AT TRANSISTOR LEVEL

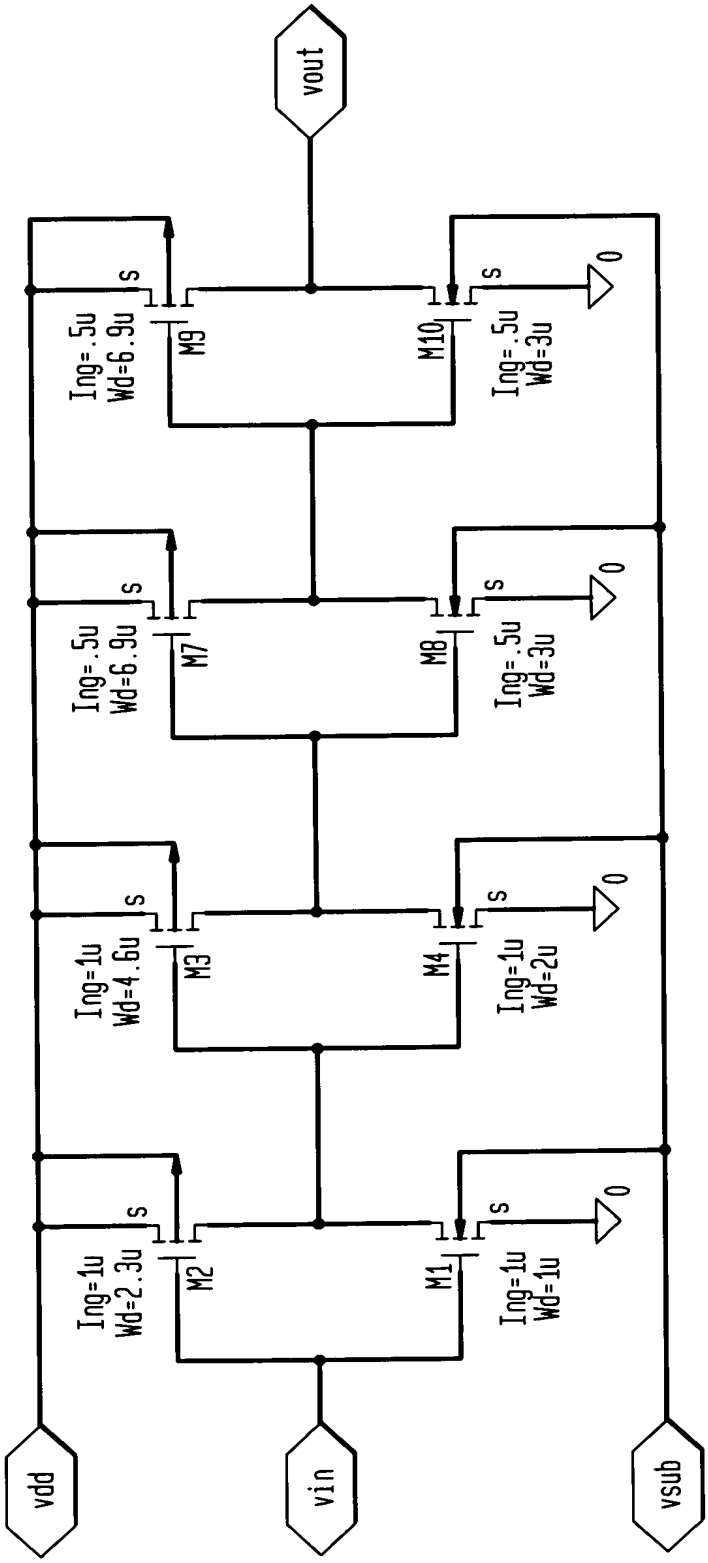


FIG. 250

PULSE GENERATOR#1 AT GATE LEVEL

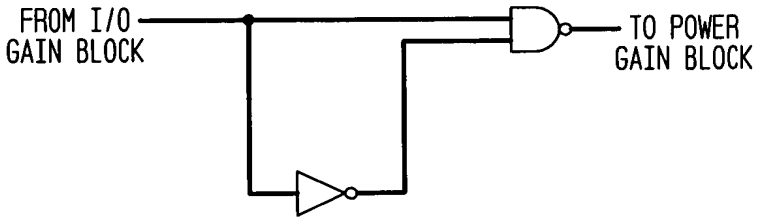



FIG. 251

PULSE GENERATOR#1 AT TRANSISTOR LEVEL

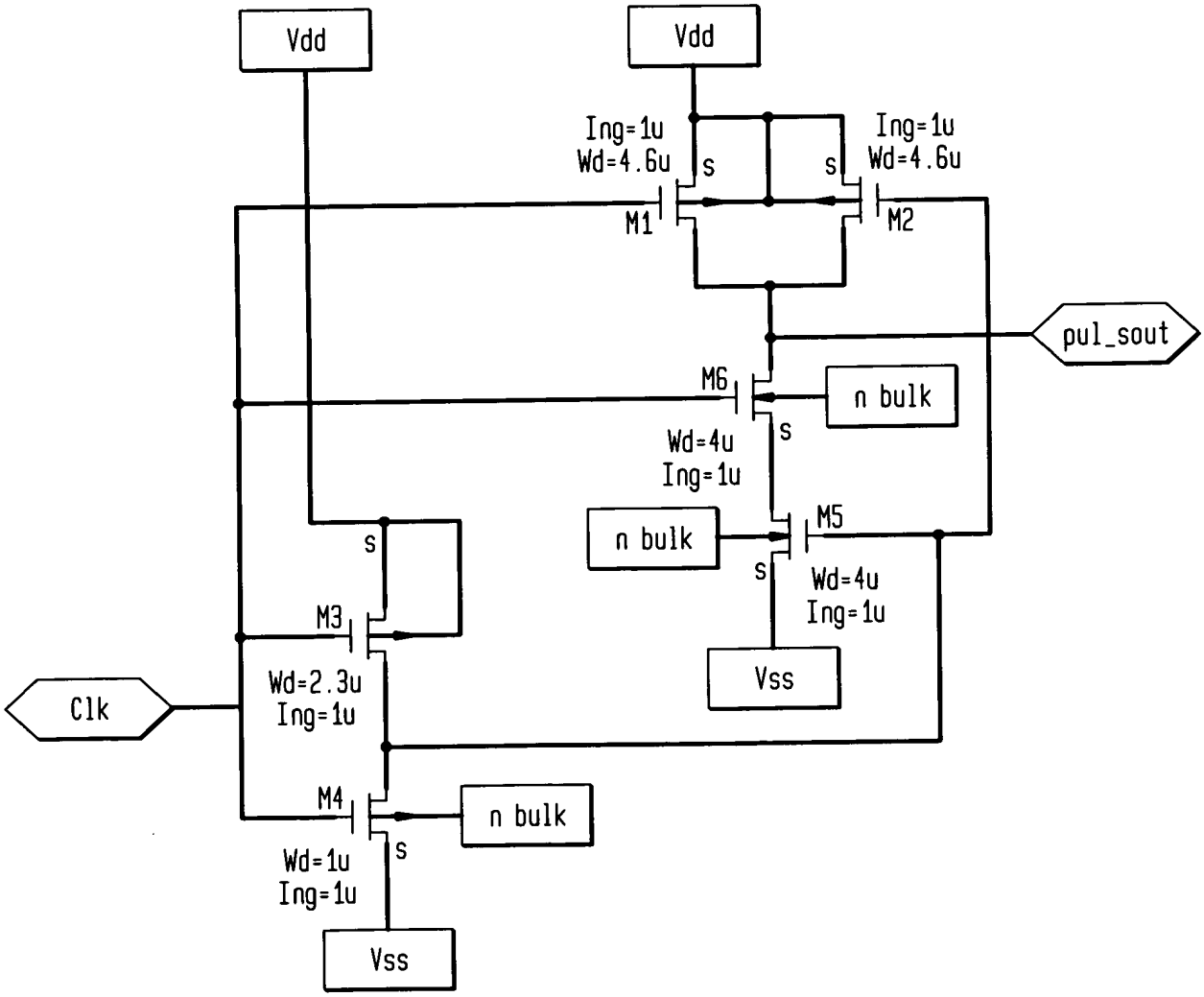
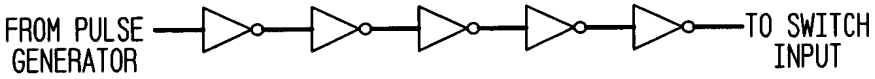


*FIG. 252*

POWER GAIN BLOCK AT GATE LEVEL



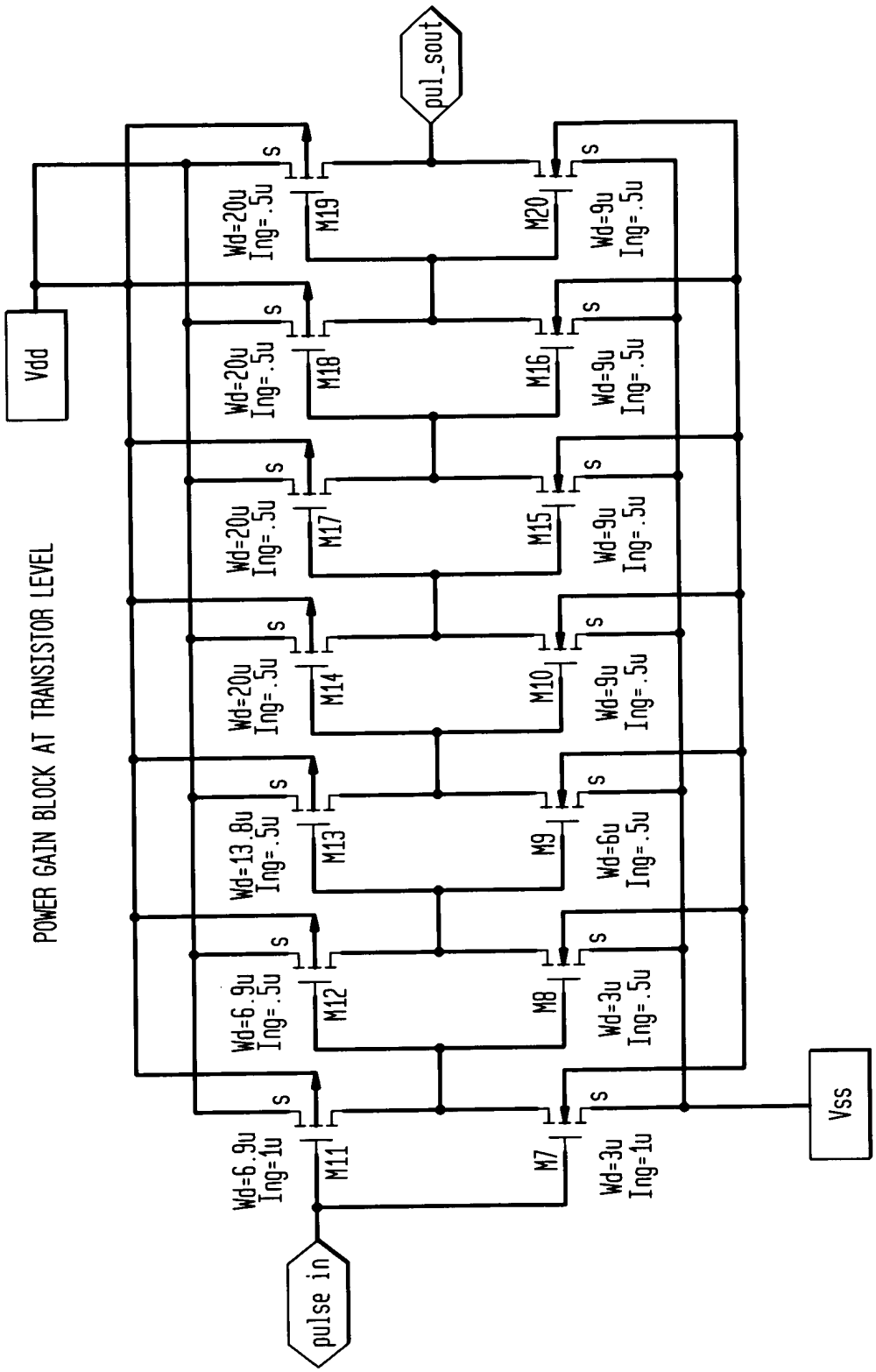



FIG. 253

POWER GAIN BLOCK AT TRANSISTOR LEVEL

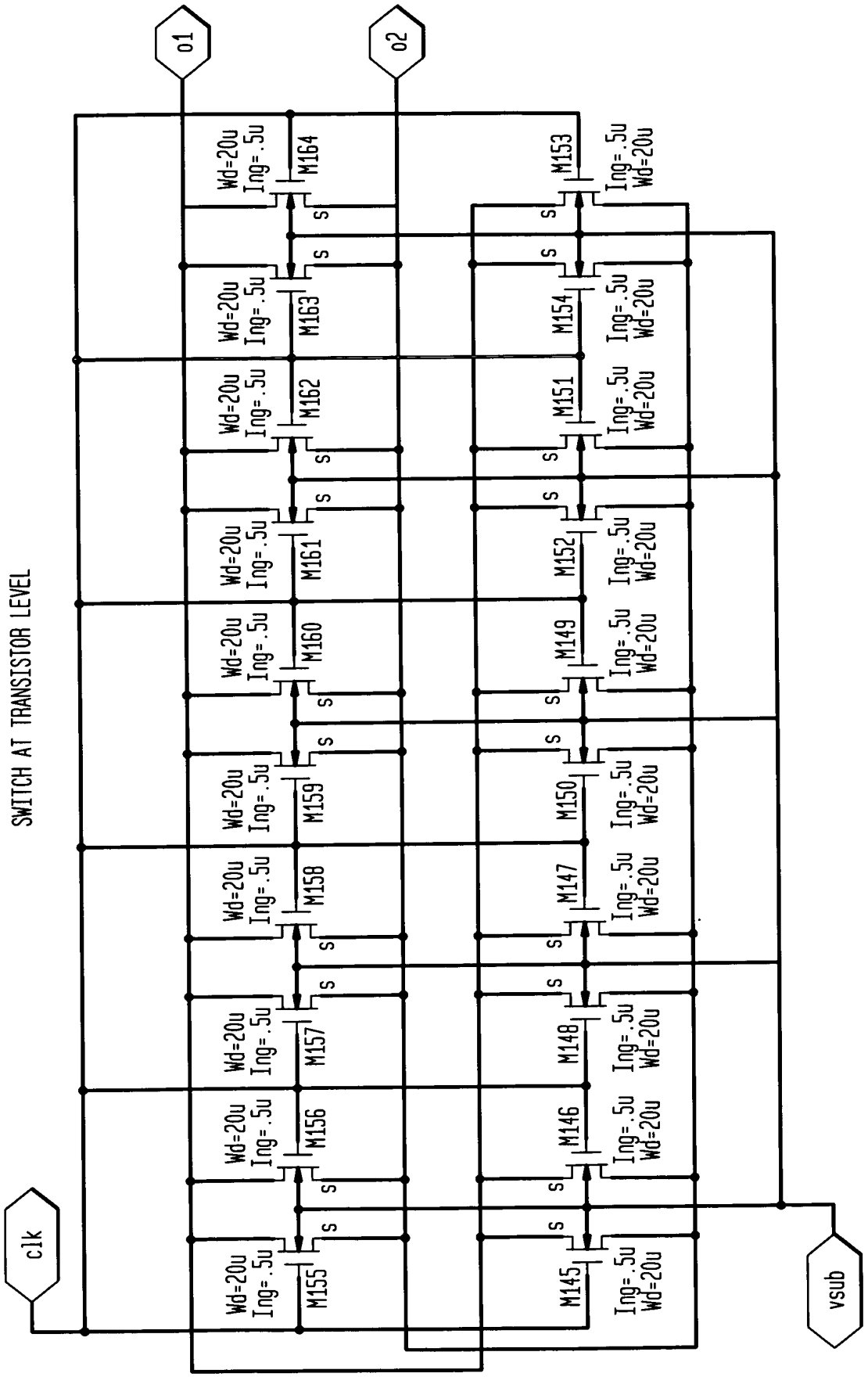



FIG. 254

SWITCH AT TRANSISTOR LEVEL

*FIG. 255*

CMOS "HOT CLOCK" BLOCK DIAGRAM

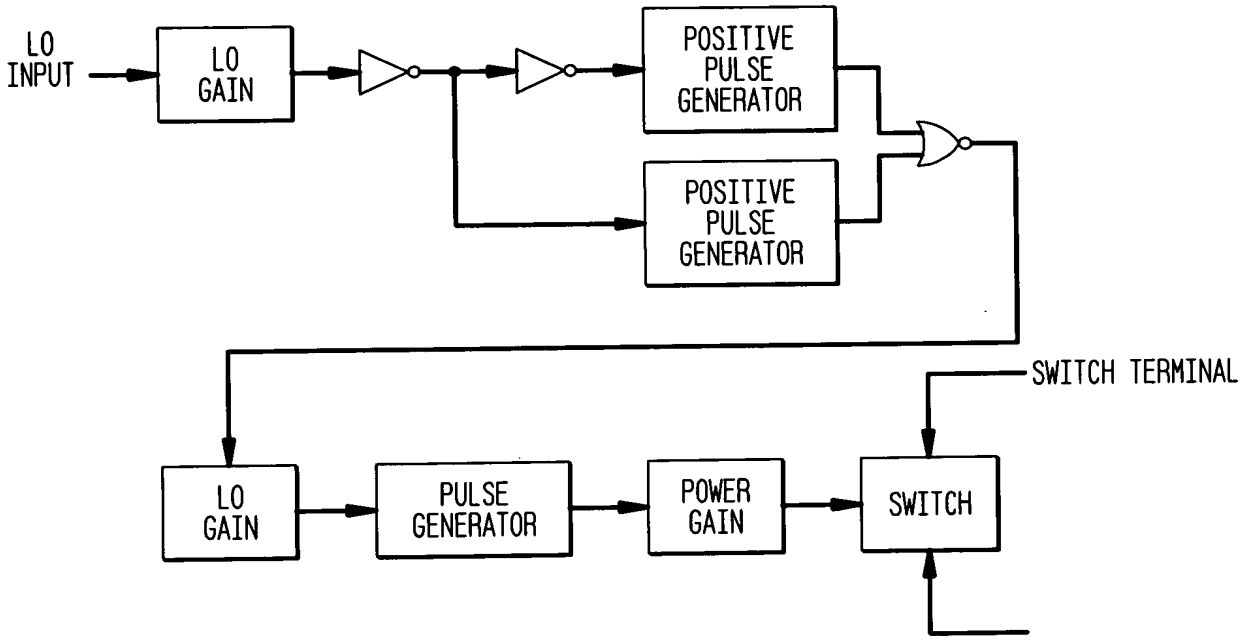
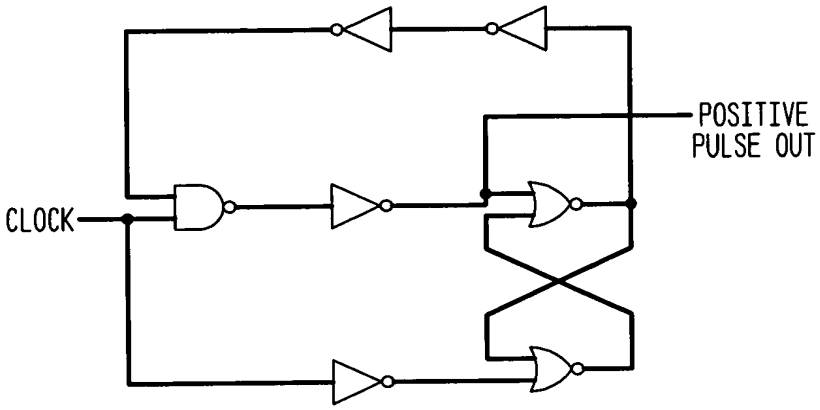


FIG. 256

POSITIVE PULSE GENERATOR AT GATE LEVEL



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Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 257
POSITIVE PULSER AT TRANSISTOR LEVEL

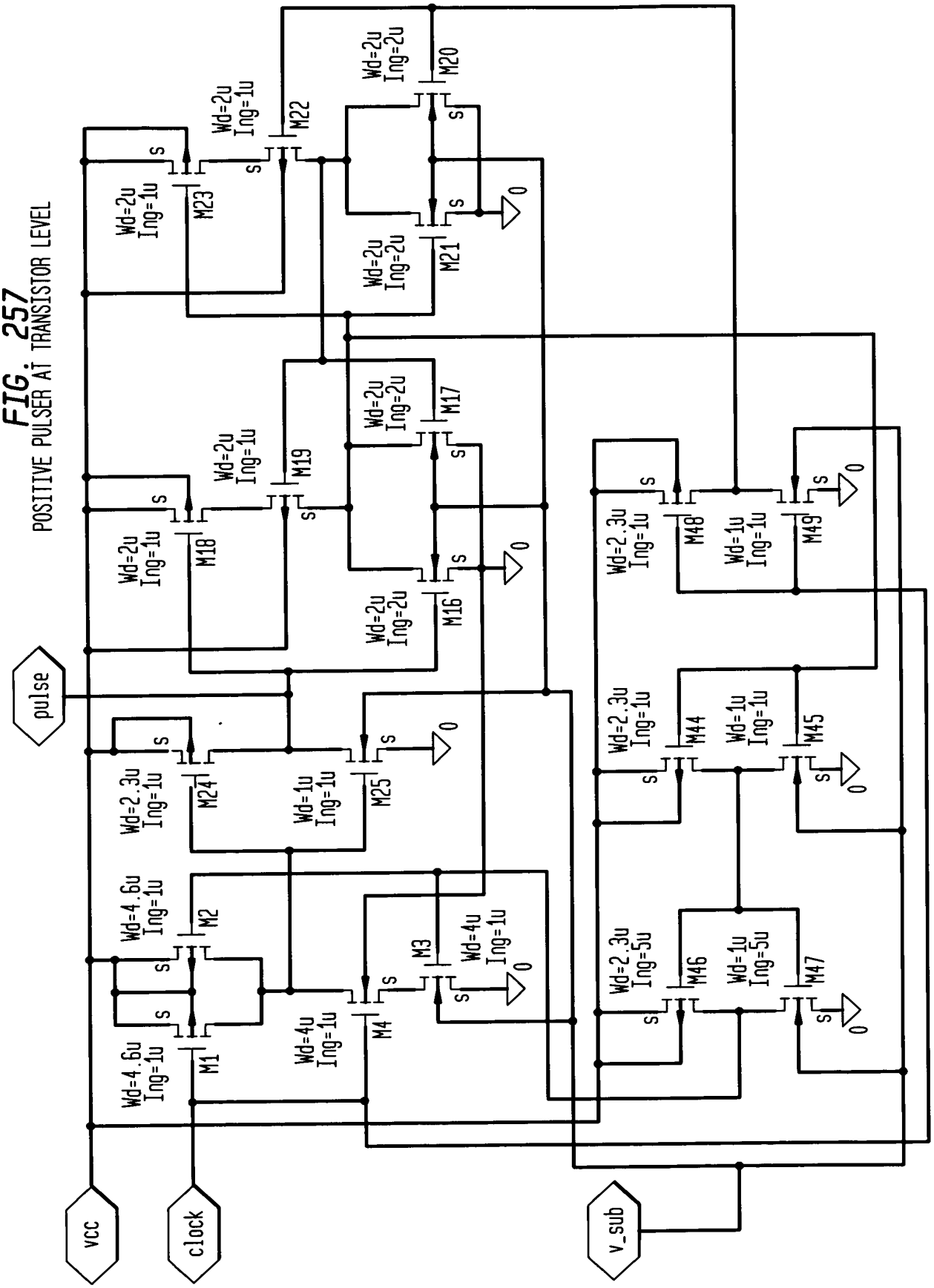
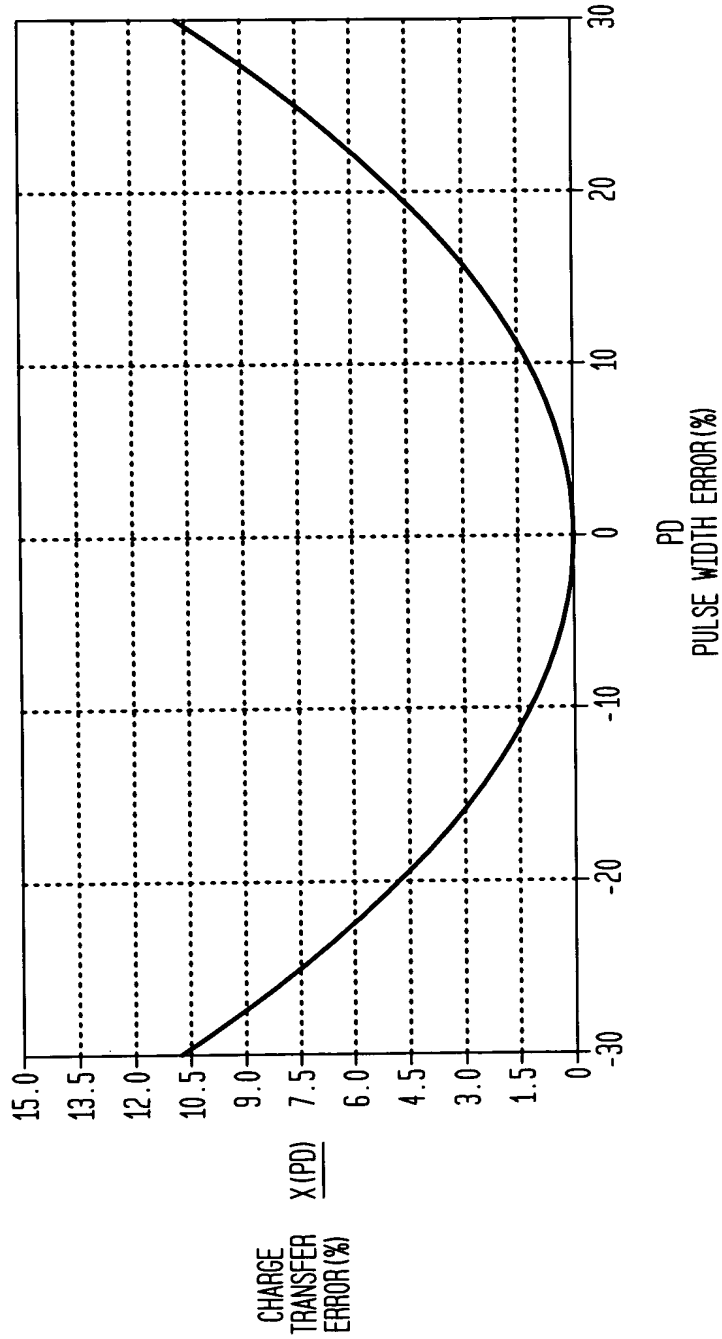


*FIG. 258*

PULSE WIDTH ERROR EFFECT FOR 1/2 CYCLE



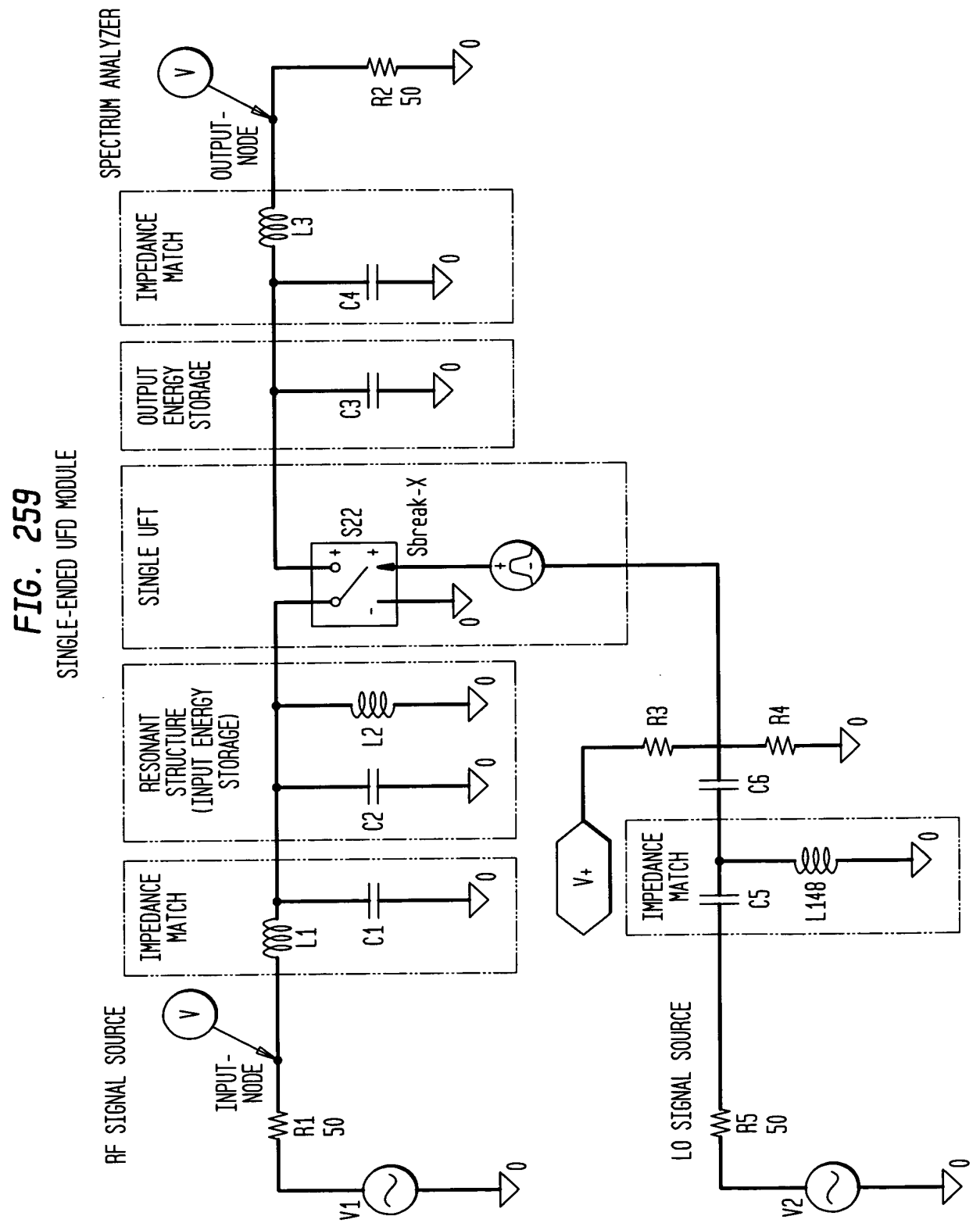



FIG. 259
SINGLE-ENDED UFD MODULE

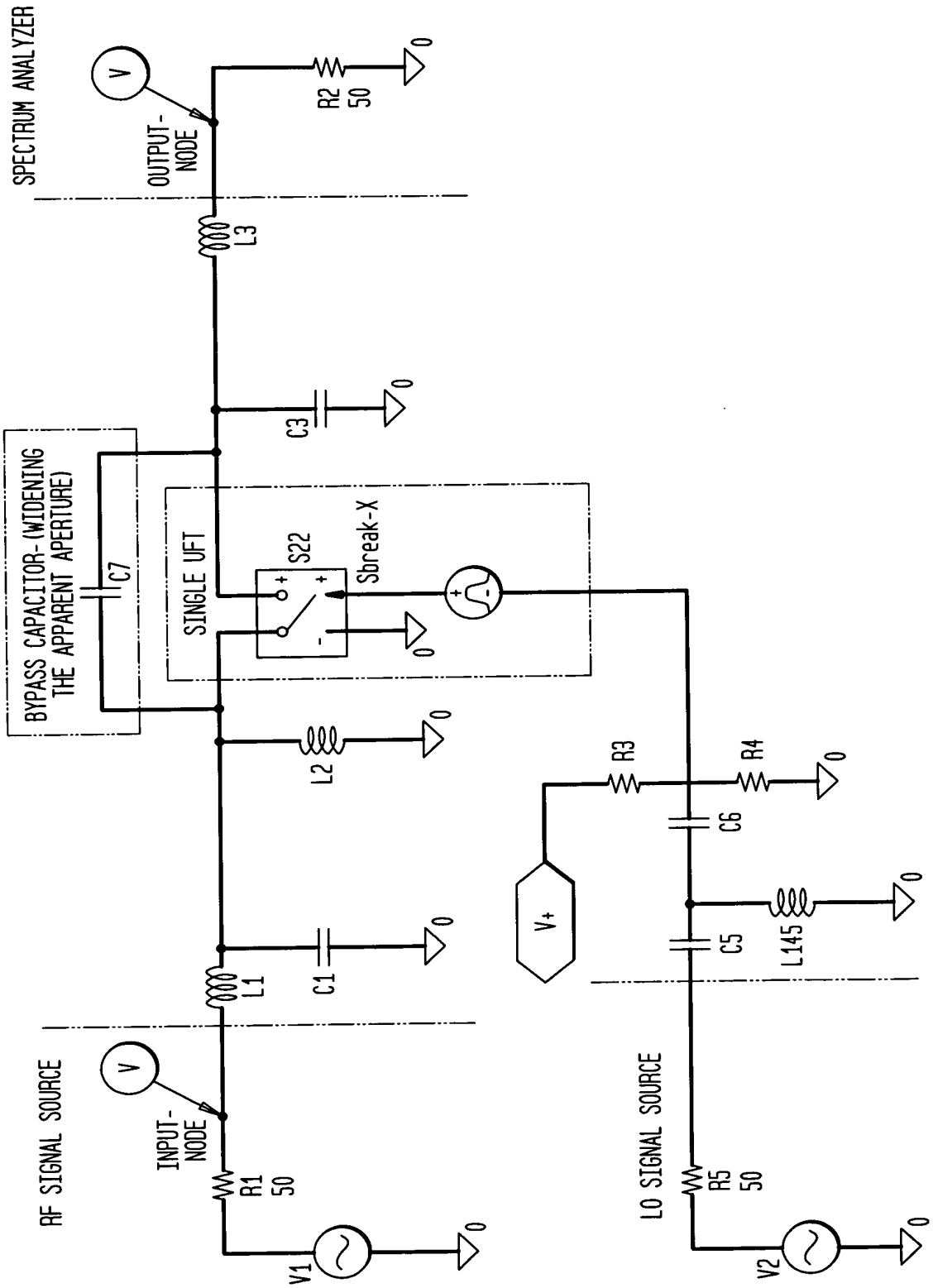



FIG. 260
SINGLE-ENDED UFD MODULE

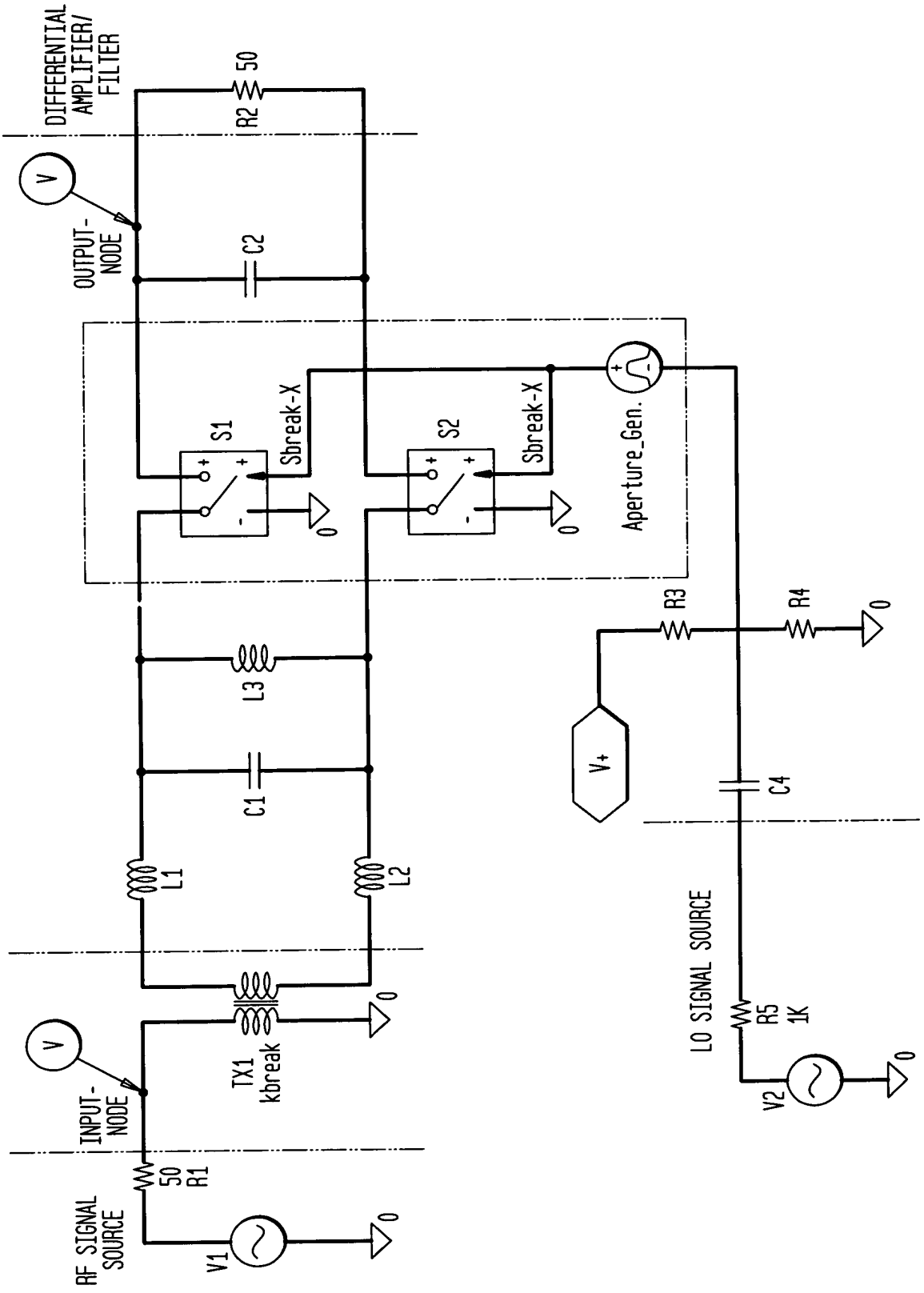



FIG. 261
FULL DIFFERENTIAL

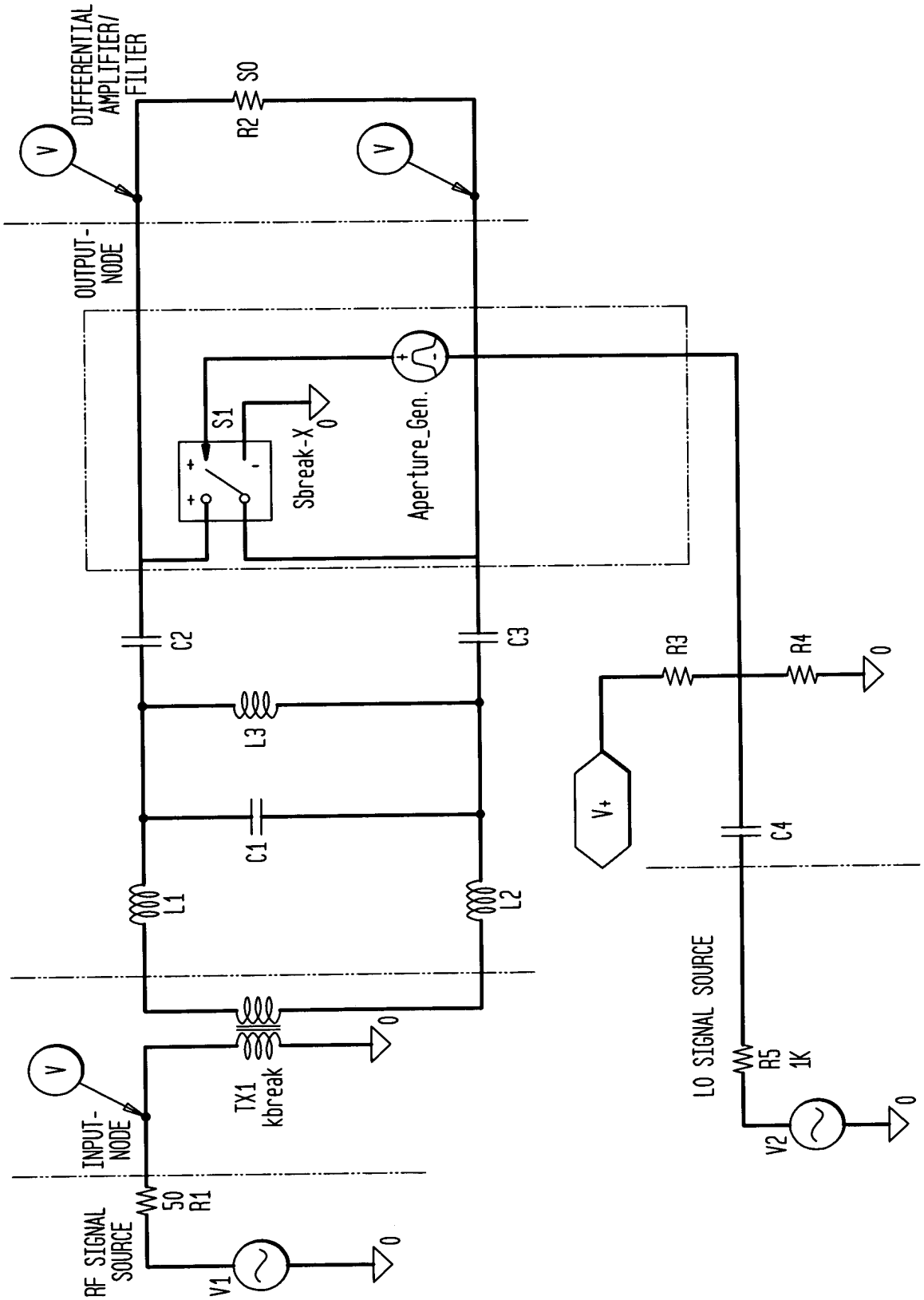



FIG. 262
FULL DIFFERENTIAL

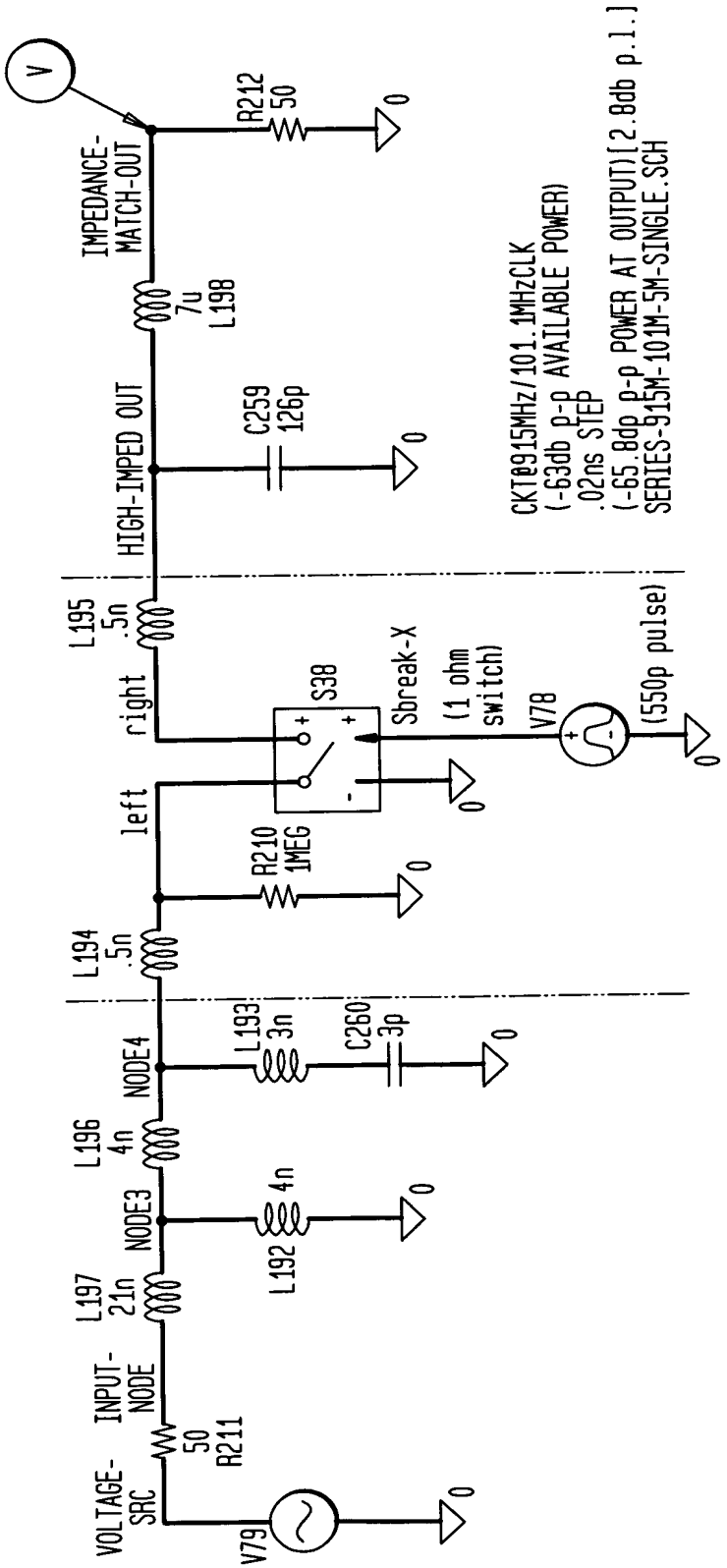



FIG. 263

SINGLE-ENDED, NEAR IDEAL SIMULATION

FIG. 264

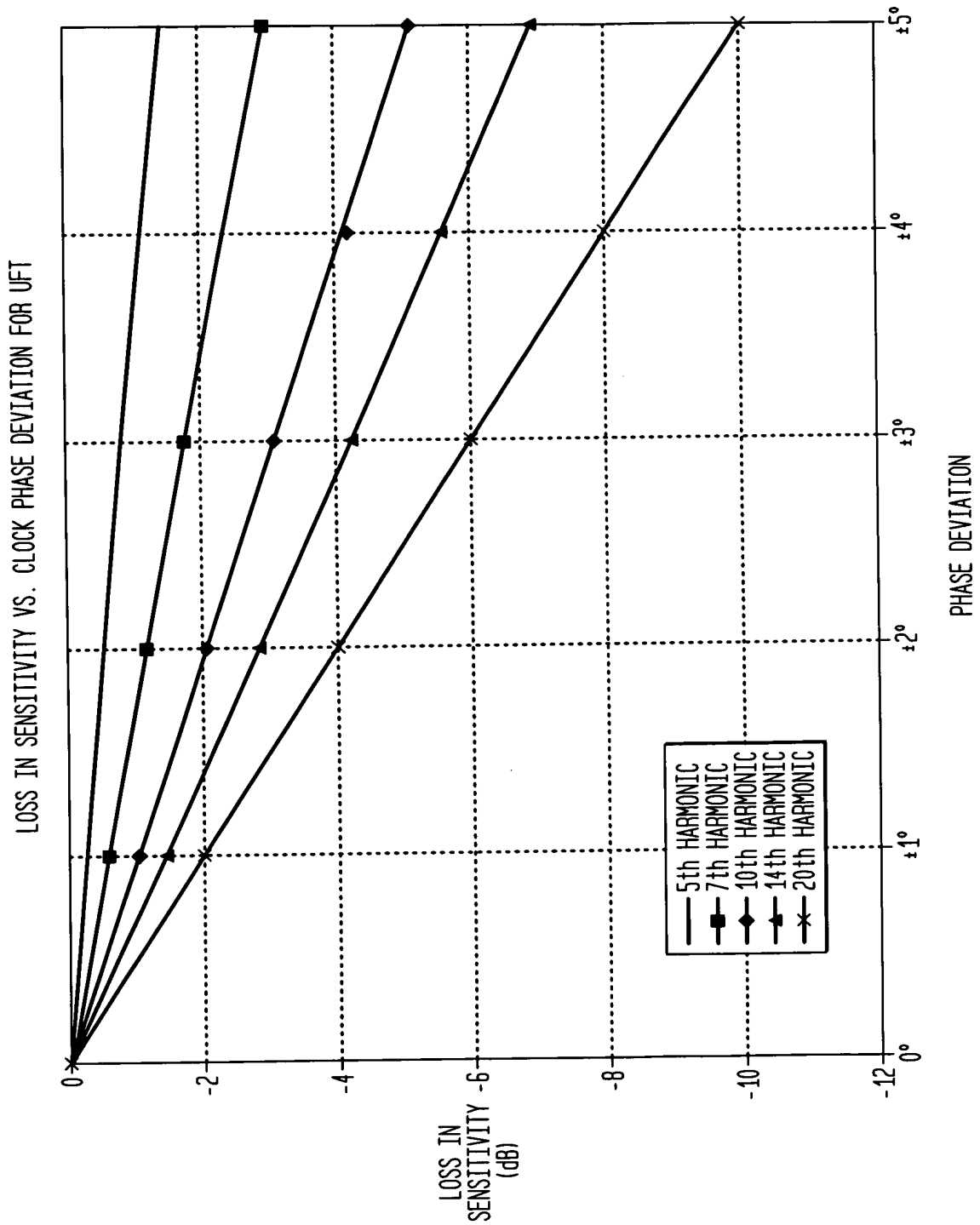
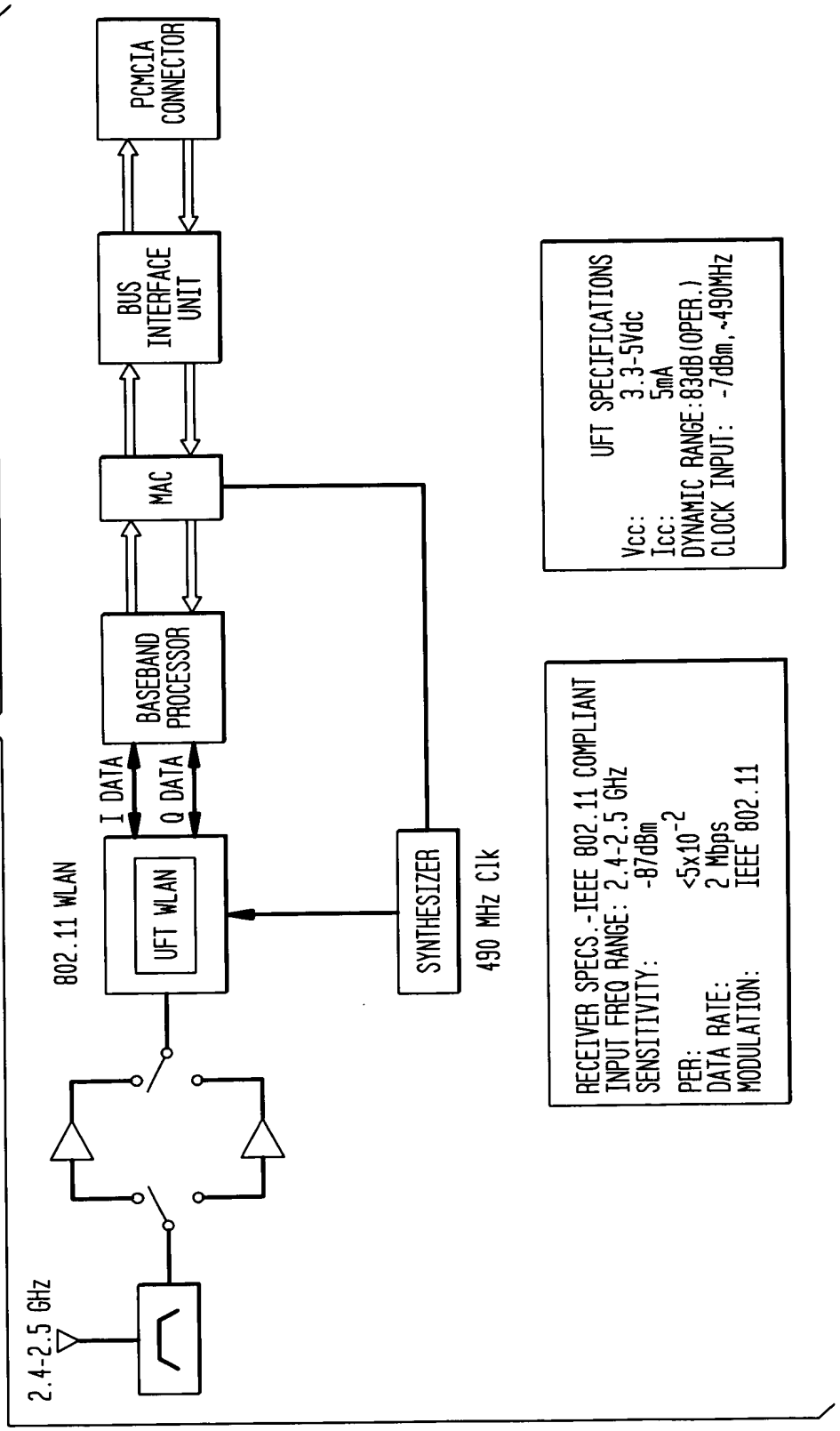

LOSS IN SENSITIVITY VS. CLOCK PHASE DEVIATION FOR UFT
LOSS IN SENSITIVITY (dB)
0
-2
-4
-6
-8
-10
-12
0°
±1°
±2°
±3°
±4°
±5°
PHASE DEVIATION
5th HARMONIC
7th HARMONIC
10th HARMONIC
14th HARMONIC
20th HARMONIC

FIG. 265


PCMCIA CONNECTOR
BUS INTERFACE UNIT
MAC
BASEBAND PROCESSOR
I DATA
Q DATA
802.11 WLAN
UFT WLAN
SYNTHESIZER
490 MHz Clk
2.4-2.5 GHz
UFT SPECIFICATIONS
Vcc: 3.3-5Vdc
Icc: 5mA
DYNAMIC RANGE: 83dB(OPER.)
CLOCK INPUT: -7dBm, ~490MHz
RECEIVER SPECS.-IEEE 802.11 COMPLIANT
INPUT FREQ RANGE: 2.4-2.5 GHz
SENSITIVITY: -87dBm
PER: $<5x10^{-2}$
DATA RATE: 2 Mbps
MODULATION: IEEE 802.11

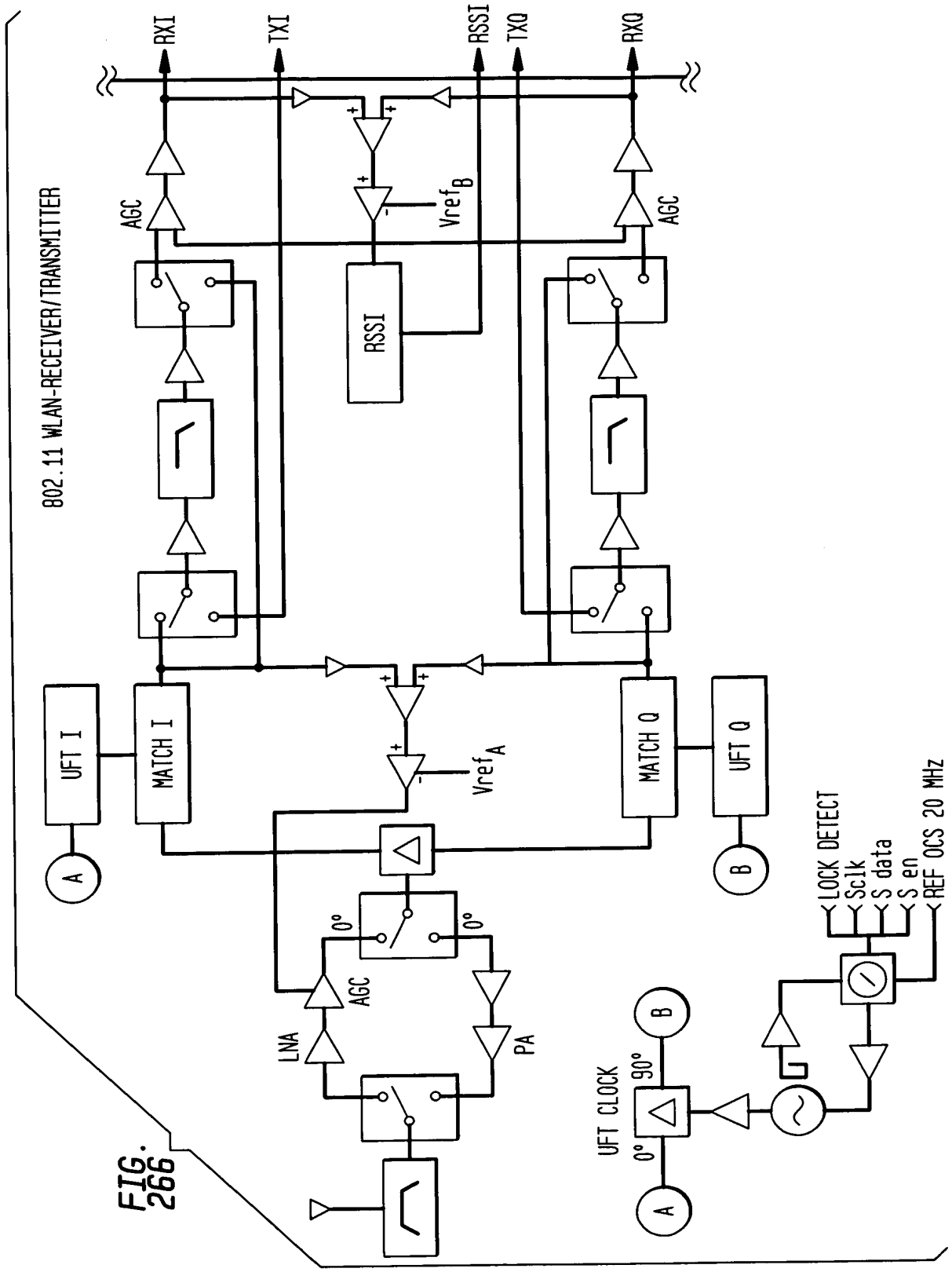

802.11 WLAN-RECEIVER/TRANSMITTER
RXI
TXI
RSSI
TXQ
RXQ
AGC
AGC
$Vref_B$
RSSI
UFT I
MATCH I
$Vref_A$
MATCH Q
UFT Q
A
B
0°
0°
AGC
LNA
PA
UFT CLOCK
90°
0°
B
A
LOCK DETECT
Sclk
S data
S en
REF OCS 20 MHz

FIG. 266

FIG. 267

| PARAMETER | 802.11 REQUIREMENT OR INDUSTRY PRACTICE | UFT MODULE BASED RX PERFORMANCE |
|---|---|---|
| OPERATING BAND | 2.4-2.5 GHz | 2.4-2.5 GHz |
| CHANNELS | 2.402 TO 2.495 IN 1 MHz STEPS<br>2.412 TO 2.484 GHz IN 5 MHz STEPS | 2.402 TO 2.495 IN 1 MHz STEPS<br>2.412 TO 2.484 GHz IN 5 MHz STEPS |
| MODULATION | BPSK,QPSK,(BARKER,CCK) | BPSK,QPSK |
| TX SPECTRAL MASK | FIRST SIDELOBE REJECT<-30,+15dBm<br>SECOND SIDELOBE REJECT<-50,+15dBm | -35 dBr,-55dBr |
| EYE OPENING | Verr<.35<br>FOR 1000 COMPLEX SAMPLES | <.3 |
| OPERATIONAL DYNAMIC RANGE | 76 dB (DERIVED) | 83 dB |
| MAX. INPUT, @, 8% PER | -4 dBm | -4 dBm |
| SENSITIVITY | -80 dBm @ <8% PER | -87 dBm @ <5% PER |
| ACQUISITION | 802.11 DSS AND FH | 802.11 DSS AND FH |
| IMAGE REJECTION | >80 dB | >80 dB |
| LO RERADIATION | < -50 dBm | < -50 dBm |
| ADJACENT CHANNEL REJECTION | > 35 dB @ 30 MHz OFFSET<br>PER <8% | > 35 dB @ 30 MHz OFFSET<br>PER <5% |
| POWER | 3.3,5V 1.5W (RX MODE) | 3.3,5V,700mW |

FIG. 268

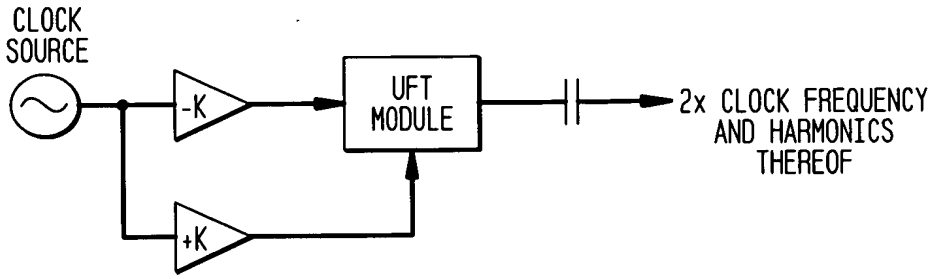



FIG. 269

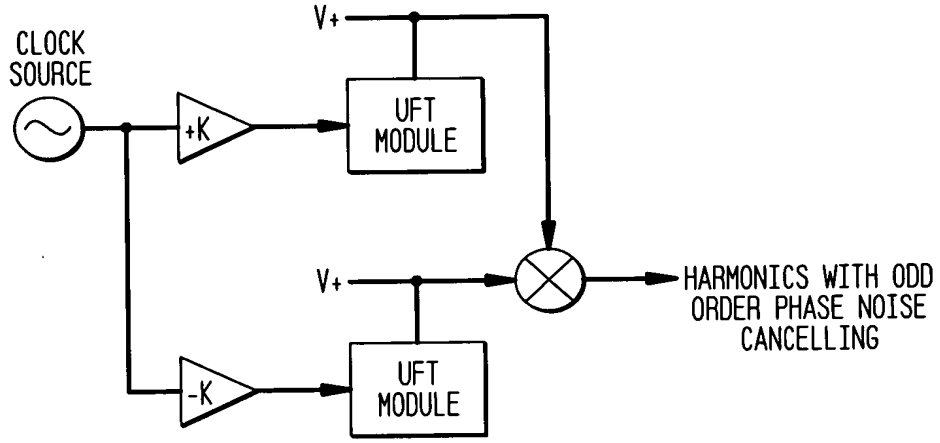



FIG. 270

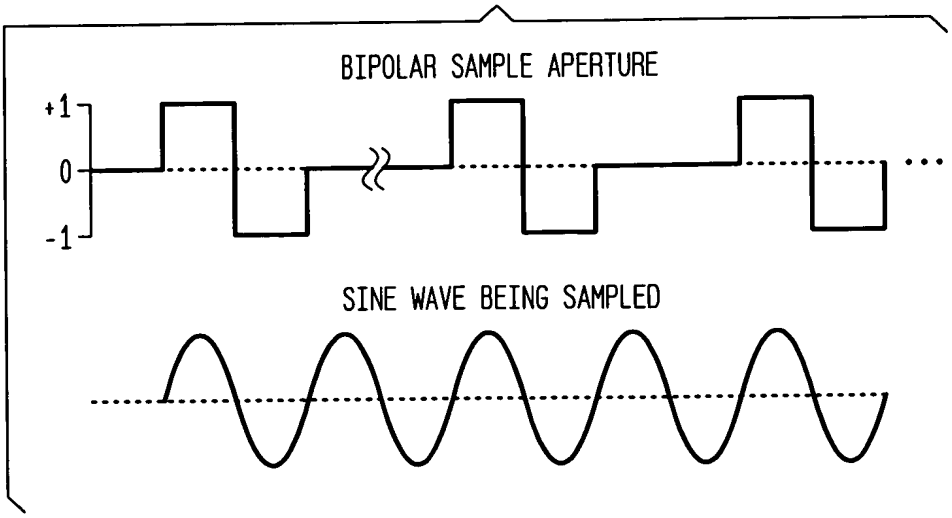


FIG. 271

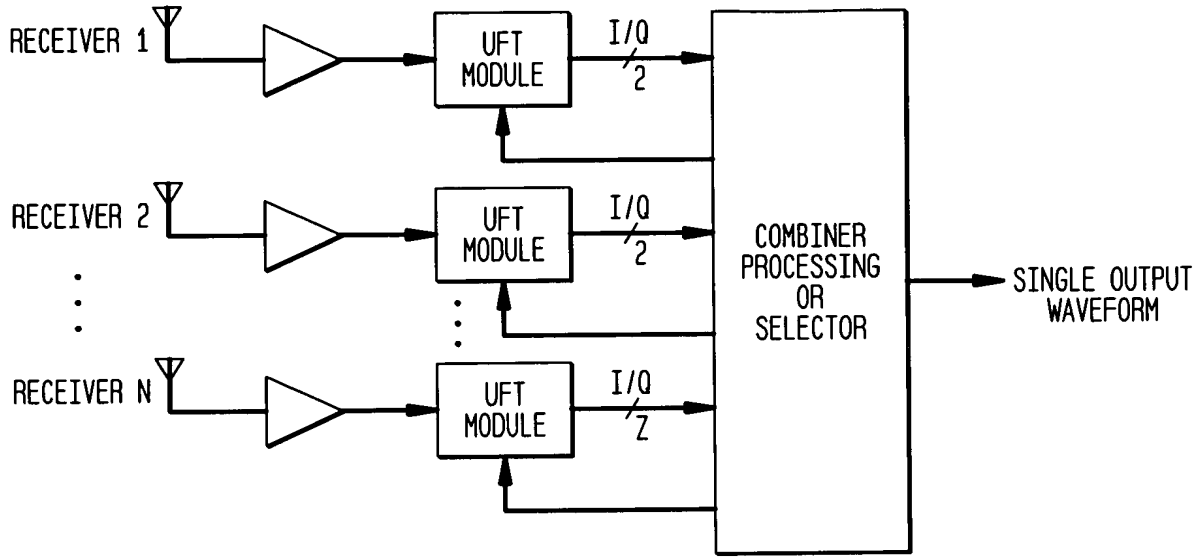
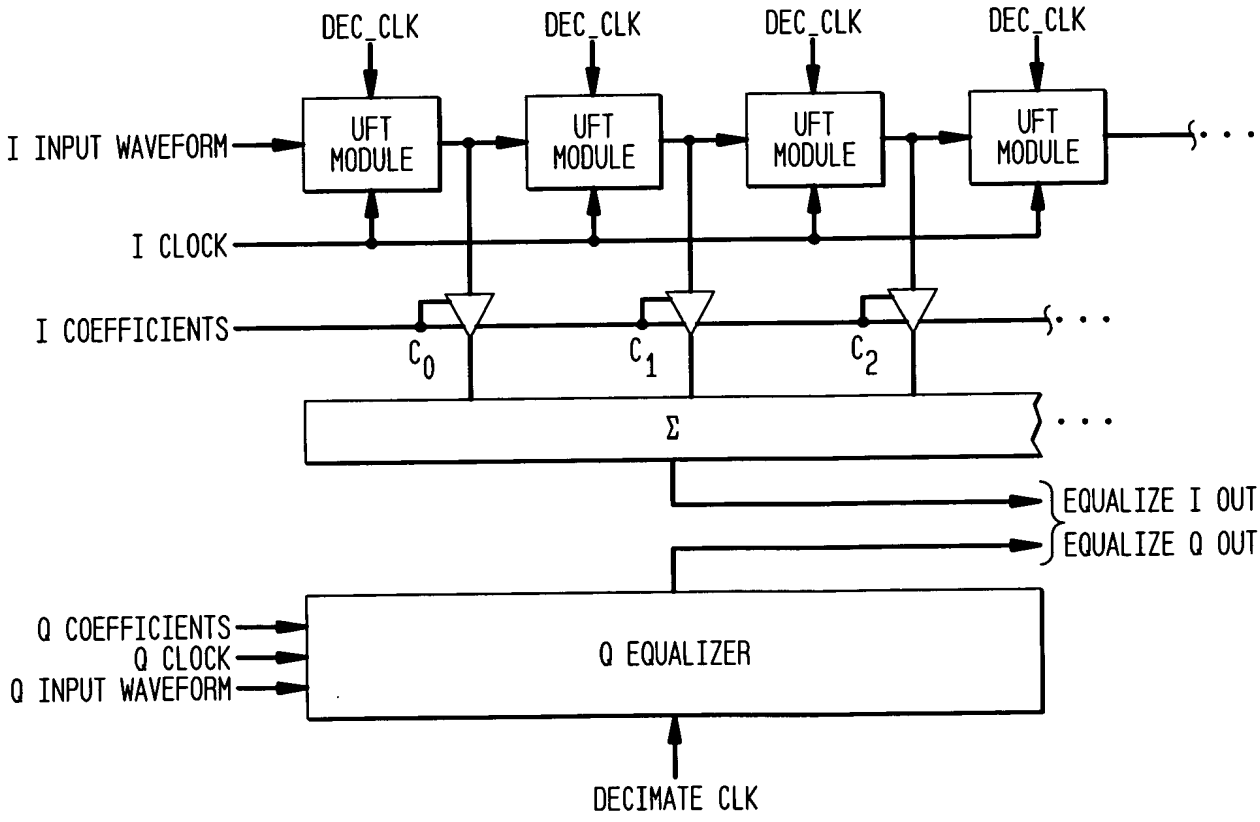



FIG. 272



Replacement Sheet
Sheet 274 of 284
Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 273

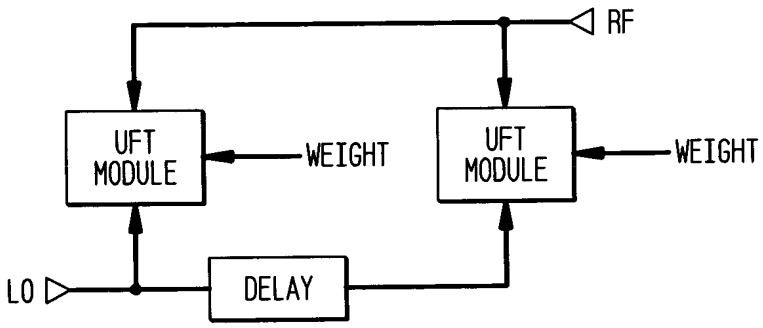



FIG. 274

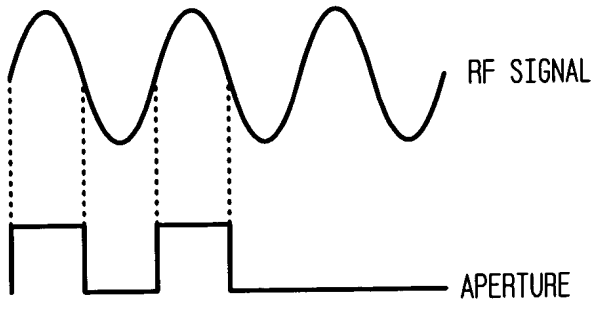


FIG. 275

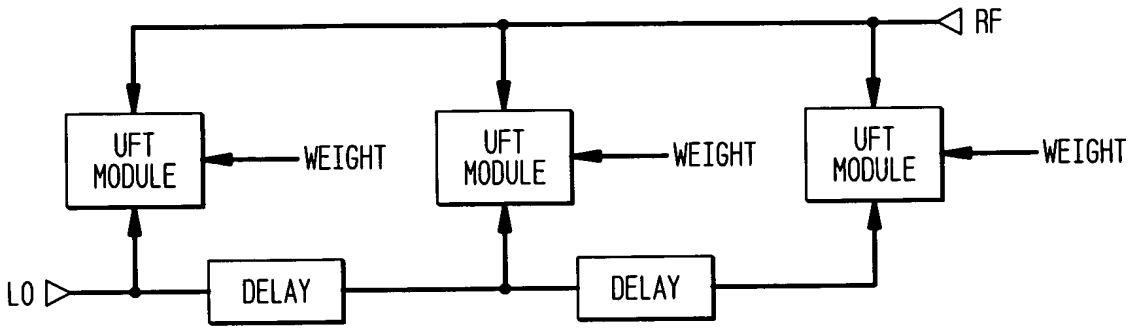



FIG. 276

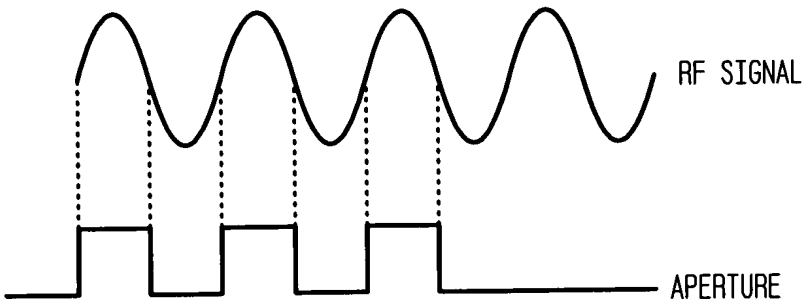


FIG. 277

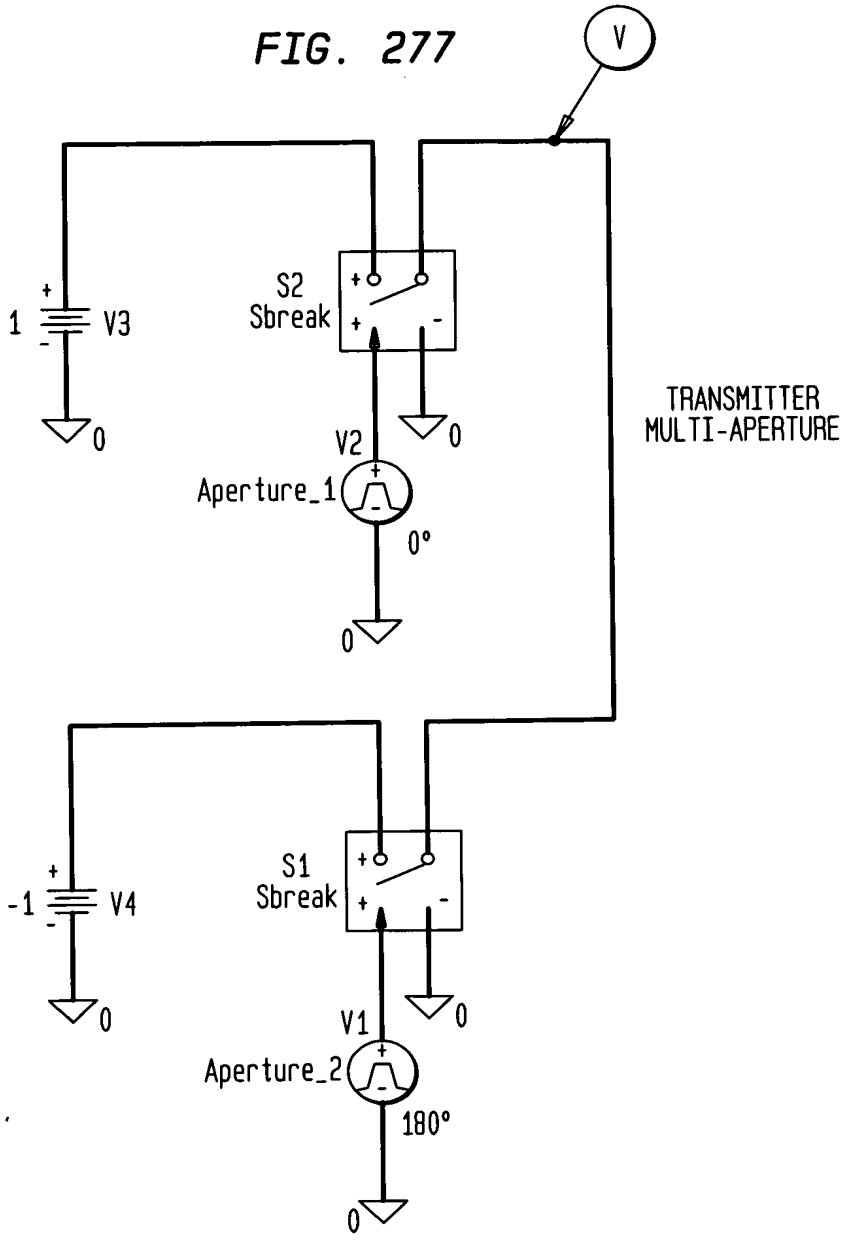
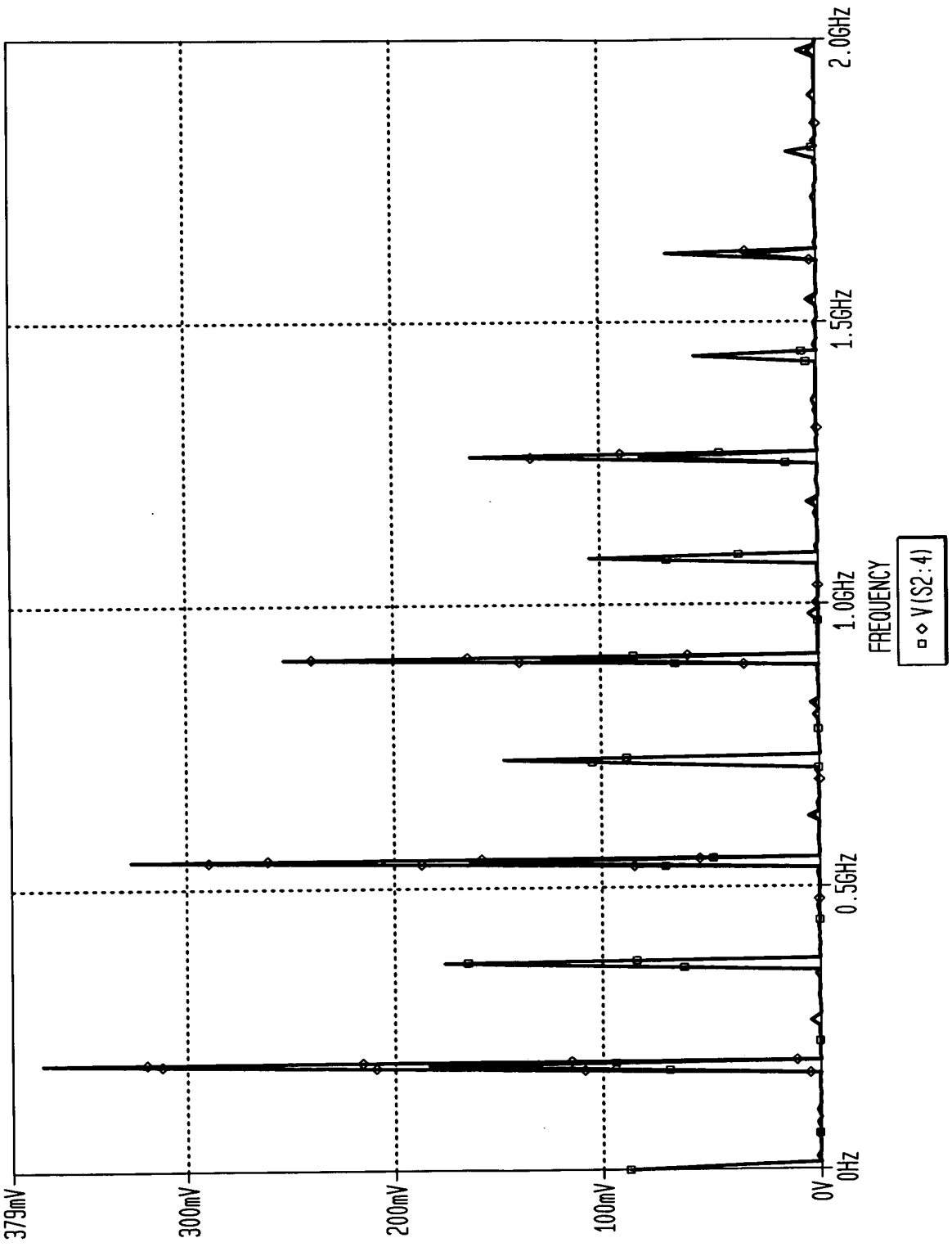
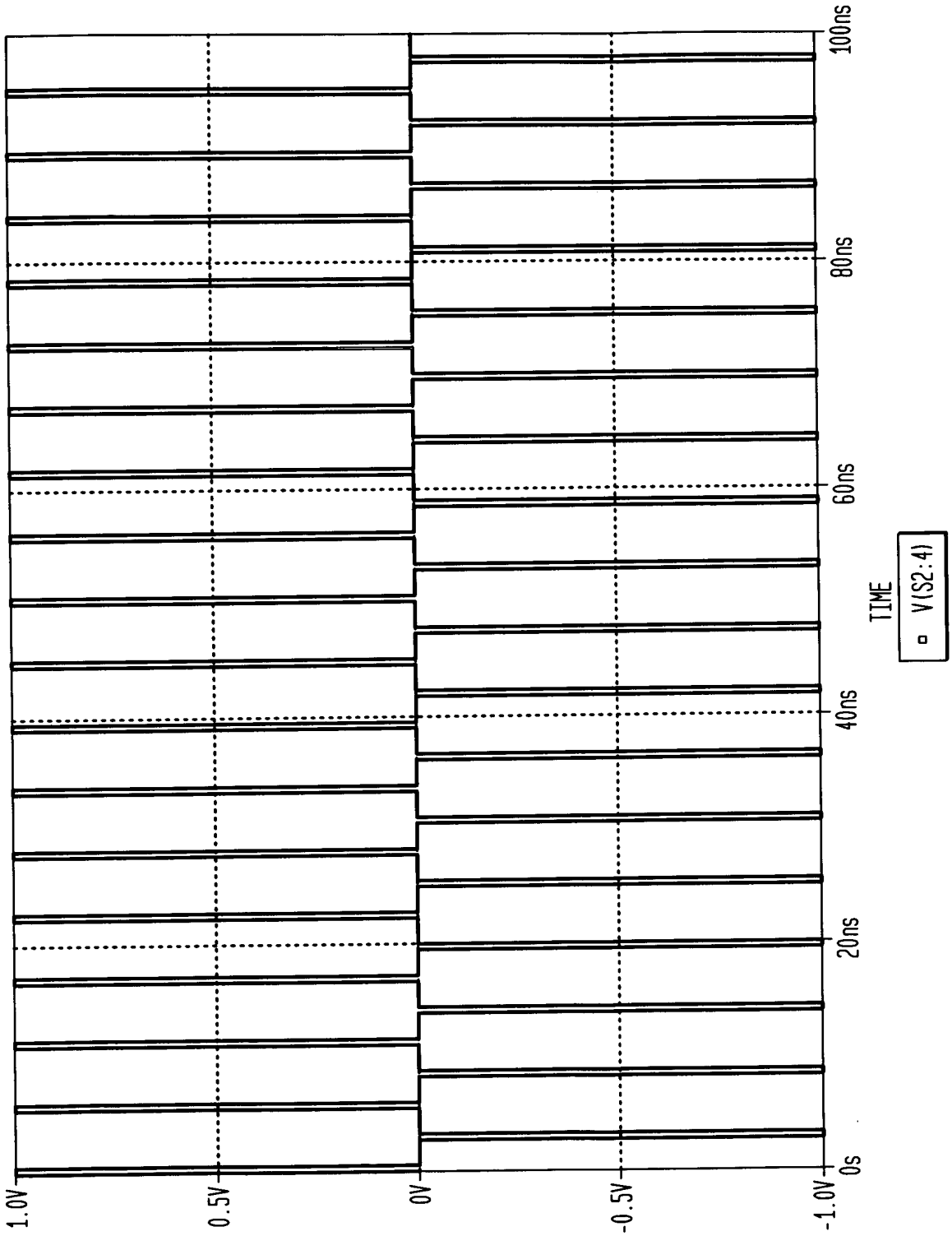

V
S2
Sbreak
1
V3
0
0
V2
Aperture_1
0°
0
TRANSMITTER
MULTI-APERTURE
S1
Sbreak
-1
V4
0
0
V1
Aperture_2
180°
0

FIG. 278


379mV
300mV
200mV
100mV
0V
0Hz
0.5GHz
1.0GHz
1.5GHz
2.0GHz
FREQUENCY
V(S2:4)

Replacement Sheet
Sheet 278 of 284
Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an
Electromagnetic Signal, and Transforms for Same

FIG. 279



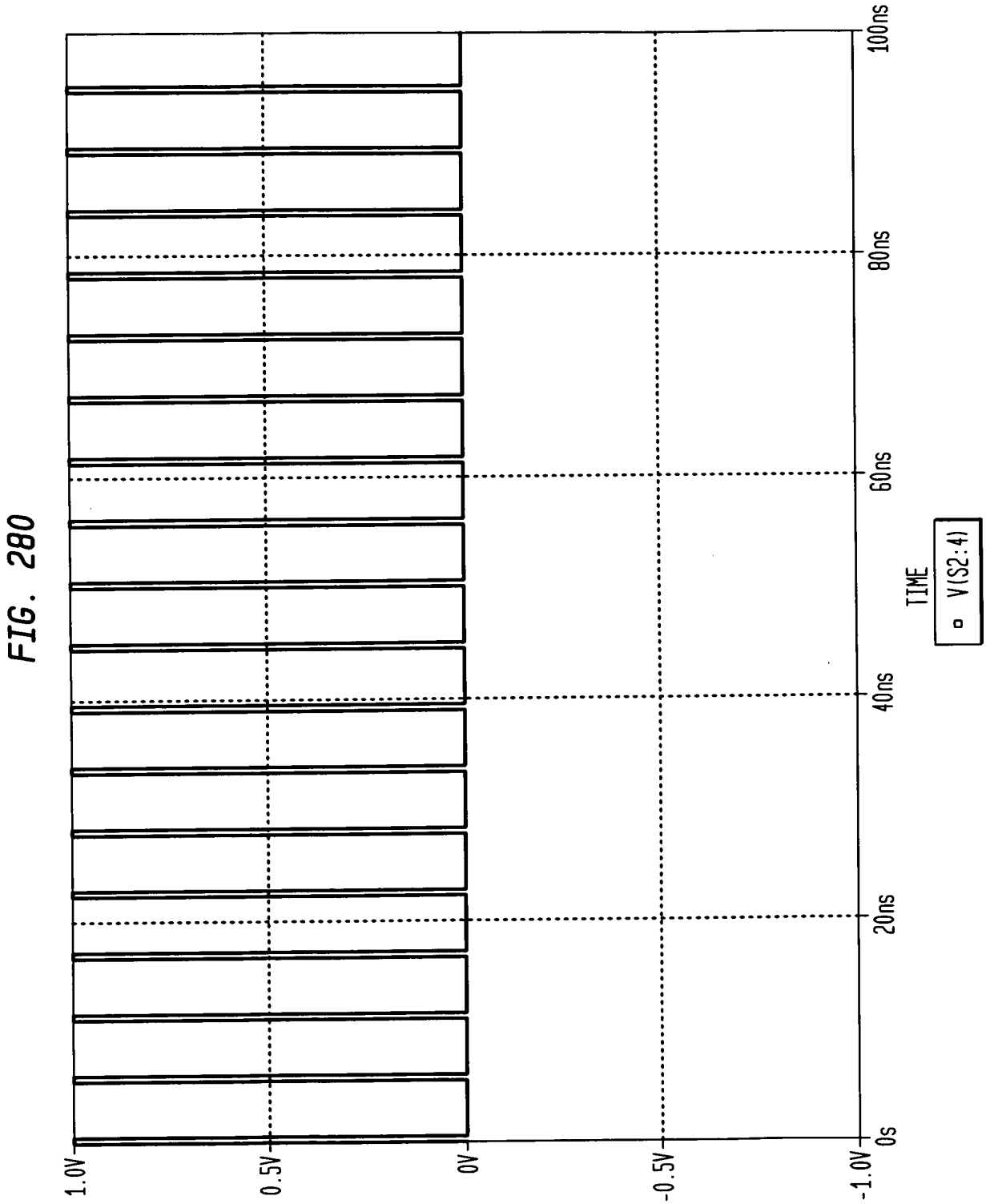
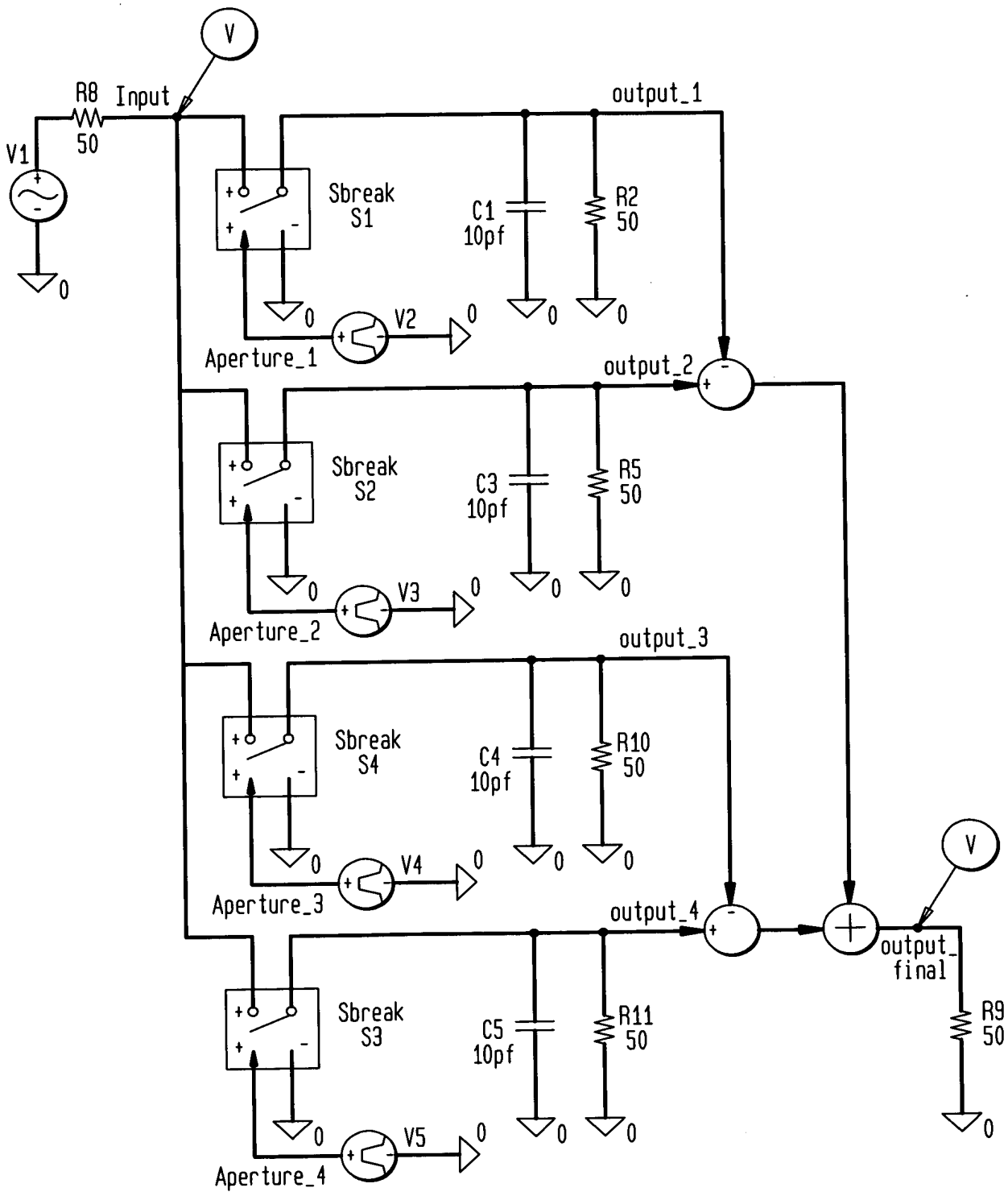



FIG. 280

# FIG. 281

MULTIPLE APERTURE RECEIVER IMPLEMENTATION



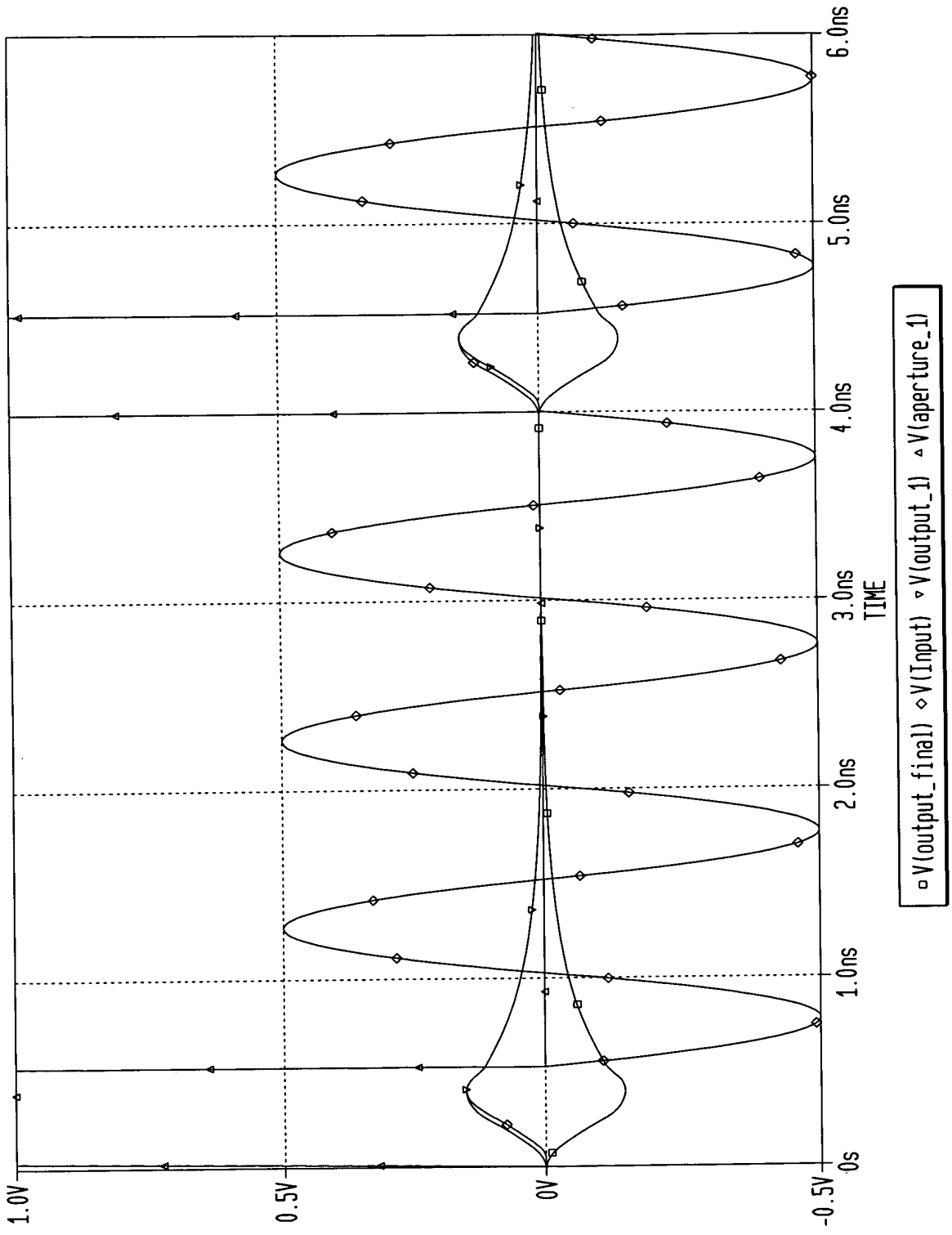

SINGLE APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final) V(Input) V(output_1) V(aperture_1)

FIG. 282

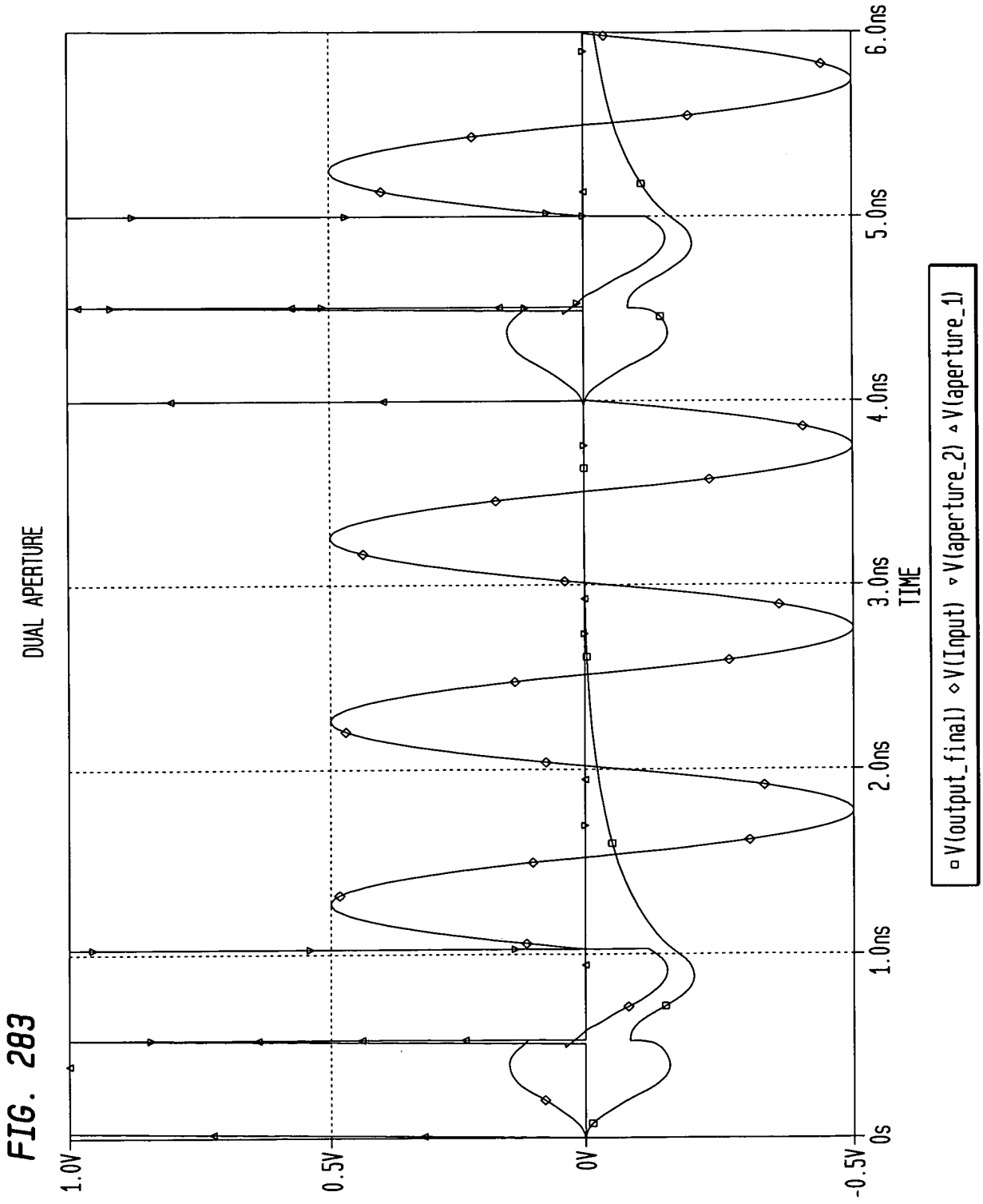

DUAL APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final) V(Input) V(aperture_2) V(aperture_1)

FIG. 283

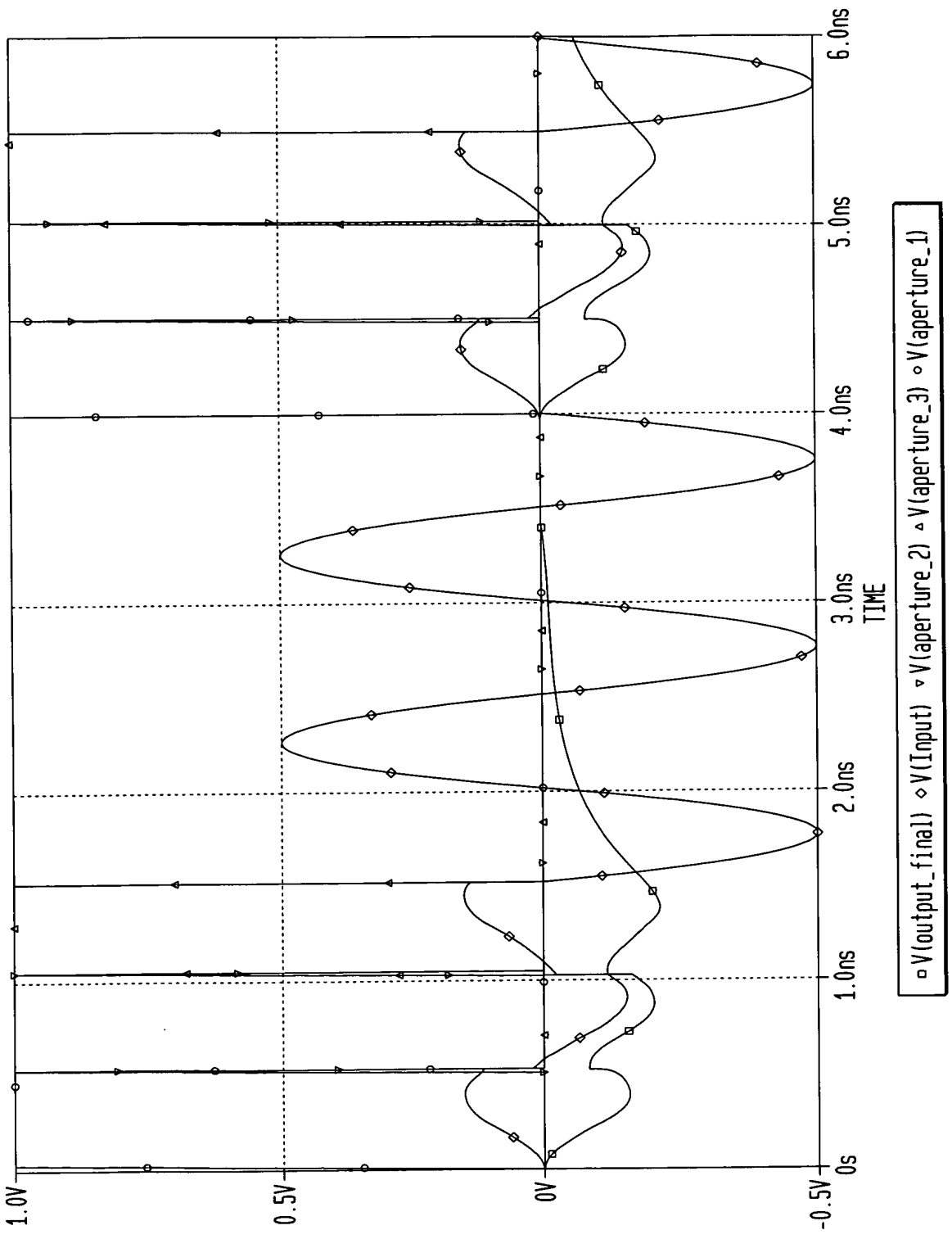

TRIPLE APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final) V(Input) V(aperture_2) V(aperture_3) V(aperture_1)

FIG. 284

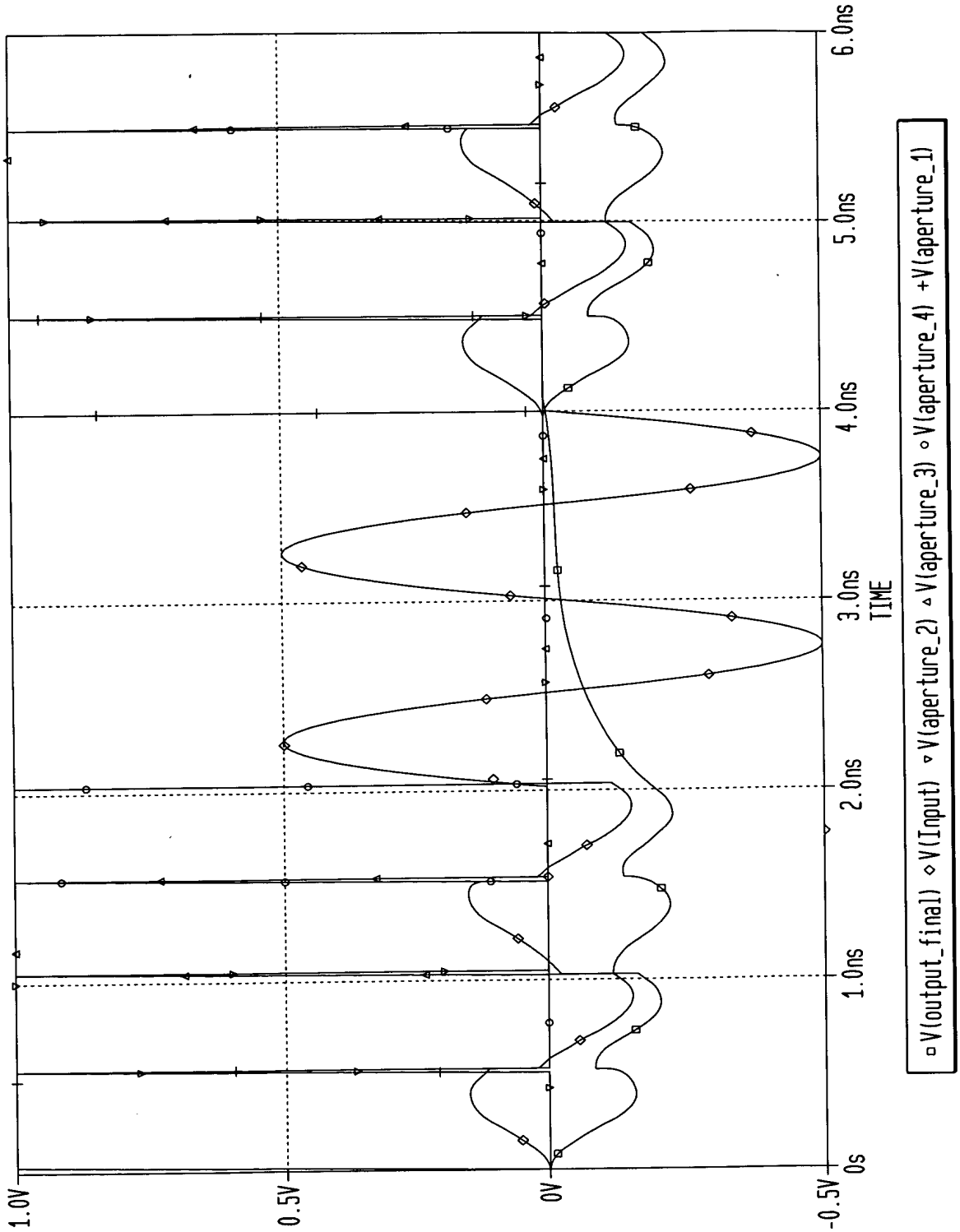

QUAD APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final) V(Input) V(aperture_2) V(aperture_3) V(aperture_4) +V(aperture_1)

FIG. 285